Article

Regression Model-Based AMS Circuit Optimization Technique Utilizing Parameterized Operating Condition

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Abstract: An analog and mixed-signal (AMS) circuit that draws on machine learning while using a regression model differs in terms of the design compared to more sophisticated circuit designs. Technology structures that are more advanced than conventional CMOS processes, specifically the fin field-effect transistor (FinFET) and silicon-on-insulator (SOI), have been proposed to provide the higher computation performance required to meet various design specifications. As a result, the latest research on AMS design optimization has enabled enormous resource savings in AMS design procedures but remains limited with regard to reflecting the intended operating conditions in the design parameters. Hereby, we propose what is termed a supervised learning artificial neural network (ANN) as a means by which to define an AMS regression model. This approach allows for rapid searches of complex design dimensions, including variations in performance metrics caused by process–voltage–temperature (PVT) changes. The method also reduces the considerable computation expense compared to that of simulation-program-with-integrated-circuit-emphasis (SPICE) simulations. Hence, the proposed AMS circuit design flow generates highly promising output to meet target requirements while showing an excellent ability to match the design target performance. To verify the potential and promise of our design flow, a successive approximation register analog-to-digital converter (SAR ADC) is designed with a 14 nm process design kit. In order to show the maximum single ADC performance (6-bit~8-bit resolution and few GS/s conversion speed), we have set three different ADC performance targets. Under all SS/TT/FF corners, $\pm 6.25\%$ supply voltage variation, and temperature variation from $-40\ ^\circ$C to $80\ ^\circ$C, the designed SAR ADC using our proposed AMS circuit optimization flow yields remarkable figure-of-merit energy efficiency (approximately 15 fJ/conversion step).

Keywords: machine learning; artificial neural network; AMS; FinFET; SOI process; PVT; SAR ADC

1. Introduction

Recent innovation in process technology has changed analog mixed-signal (AMS) circuits such that they now operate more digitally by incorporating increased transistor density levels and transistor operating speeds. Hence, design optimization of digital circuits has been actively conducted via an optimization loop based on a well-formed computer programming language, such as Verilog and VHDL. Digital circuit design optimization can easily be bound with both commercial and open-source optimization tools without extra effort [1]. On the other hand, analog circuit design is governed by human intervention, such as topology selection and the use of a full custom layout. For this reason, optimizing the designs of analog circuits often follows well-known design circuit architectures and focuses more on optimizing each sub-module [2–5] and on finding joint optimum points during the sub-module integration step [6–11]. Therefore, AMS circuit designs rely heavily

on the know-how and creativity of the designer and require considerable amounts of time to adjust the design parameters so as to ensure proper system target performance. In general, designers have to carefully check three different aspects when optimizing an AMS circuit sub-module and considering integration between modules: (1) the optimization flow should reflect the flexible designer's intention closely; (2) the execution time has to be quick as multiple iterative evaluations are required for resulting optimum output; and (3) the performance accuracy has to be guaranteed.

A number of studies have been proposed in an effort to meet these goals. These are equation-based, SPICE-based, and model (regression)-based methods. First, equation-based optimization techniques such as OPASYN [12], STAIC [13], OPTMAN [14], DON-ALD [15], DARWIN [16], and GPCAD [17] offer rapid execution performance as they rely on mathematical function-based operations. However, their use is limited when the circuit behavior cannot be expressed in an equation, and the accuracy is insufficient compared to the outcomes offered by other methods. Second, SPICE-based optimization techniques (DELIGHT.SPICE [18], ANACONDA [19], and GENOM [20]) are capable of excellent output accuracy with all AMS circuits, but they require the longest execution times among those discussed here. Last, in order to shorten the design execution time and improve the accuracy of the results, designs that use a model-based design flow have been applied to AMS design optimization. As the accuracy of the final circuit is proportional to that of the trained regression model, the support vector machine (SVM) [21] and neural network machine (NNM) [22], which have excellent regression model accuracy levels, are widely used in the AMS circuit design flow.

Although prior AMS optimization methods have evolved to fulfill certain key requirements (i.e., flexibility to accommodate the designer's intentions, rapid run times, and creditable accuracy of the output), operational sensitivity under wild operating environment changes was somewhat disregarded. Given that advanced technologies such as the fin field-effect transistor (FinFET) or silicon-on-insulator (SOI) have more process variations compared to conventional complementary metal–oxide–semiconductor (CMOS) processes, a sensitivity check step would be an essential procedure during the design optimization flow to ensure robust operation.

- We propose a new model-based design optimization technique that adaptively ensures the robust performance of AMS circuits and systems. Based on our prior research [22], we enhance the overall process by incorporating a sensitivity check step in order to offer customized operational environments as intended by the user.
- In practice, as there are demands to redesign circuits targeting different operating conditions with the same structure, this research contributes by greatly economizing the redesign effort while also increasing the production yield.
- We applied the overall design flow to an asynchronous SAR ADC architecture. The asynchronous SAR ADC design is suitable for verifying the performance of the AMS design algorithm because it is quite difficult to determine the optimal performance with respect to the key components of the ADC. Regarding the sensitivity performance, the design example covers the range of the supply voltage deviation of $\pm 6.25\%$, the temperature from $-40\,^{\circ}\text{C}$ to $80\,^{\circ}\text{C}$, and the process with SS/TT/FF corners. Finally, the figure-of-merit, which indicates the ADC power efficiency, is compared with the results when applying the SPICE-based design method.

The remainder of this paper is organized in the following manner: Section 2 introduces the detailed proposed AMS circuit optimization flow. Section 3 describes a design example employing the proposed design flow. Section 4 presents the simulated results of ADC final performance outcomes considering external condition changes. Section 5 discusses the proposed AMS circuit optimization technique, and Section 6 provides the conclusions.

2. Methods

The overall proposed AMS circuit optimization flow conducts four major steps, as illustrated in Figure 1. Before starting the design flow, the user has to clarify the target

circuit (i.e., filter, amplifier, ADC, etc.) and operating conditions. Assuming that the reference design library is well prepared, the main AMS circuit optimization flow performs from a given set of user-defined designs and system constraints. In particular, machine learning techniques (i.e., supervised learning) can be incorporated to identify the least sensitive and co-optimized output designs while building regression models as well as sub-module integration procedures. In the following subsections, four major steps are addressed in more detail.
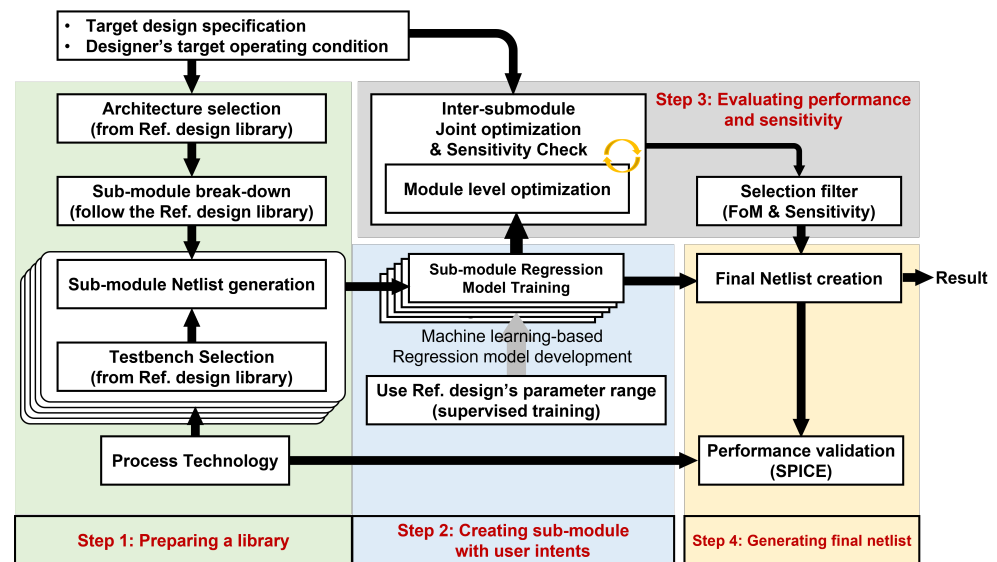

Figure 1. Top-level system diagram of the proposed AMS circuit optimization flow.

2.1. Step 1: Preparing a Library

This stage is an initial step for collecting appropriate reference designs for smaller stand-alone modules, such as a unit circuit for a parameterized library. First, each stand-alone module must be accurately evaluated using a fine SPICE simulator, after which it can be used for generating a regression model via a neural network training process. This step is important in terms of building a general-purpose library that can accommodate the various sub-modules that would compose the different target system. This step has to be performed precisely because, if the library is built with inaccurate simulation results, the accuracy of the final result deteriorates further due to the inaccuracy of the regression model.

2.2. Step 2: Creating Sub-Module with User Intent

Based on the system requirements defined by the user, this step divides the user requirements into module-level design constraints employing system design formulas and user preferences, such as those pertaining to occupation and energy efficiency. In this step, we perform supervised learning based on artificial neural networks (ANNs) [23–25] to characterize the regression model.

2.3. Step 3: Evaluating Performance and Sensitivity

To deliver reliable circuits, both the user-intended operation condition and the errors that occur during the manufacturing process must be considered. This step includes two main operations: searching for performance changes under the given conditions (e.g., process and temperature variations), and adaptively selecting the least sensitive results within the tolerance level set by the user. Because the cost and time for designing, simulating, and examining all possible operating conditions are limited, this step is challenging. However, given that the proposed design method can shorten the simulation time with its use of the regression model, it enables performance evaluations at a greater variety of operating points.

2.4. Step 4: Generating Final Netlist

Based on the prepared module library and user intents for each module, the selection filter [26] choses the proper modules for each function block, and the generation and validation of a final netlist are performed. Among the various design candidates correspondingly optimized at different operation environments, a top-level selection filter accordingly lists the possible candidates, allowing the user to sign off on the final netlist. As a result, the user-intended AMS circuit can be obtained while not only satisfying the performance matrix but also ensuring robust operation at the target environments.

3. Circuit Design

3.1. Topology Selection: Asynchronous SAR ADC

There are numerous types of AMS circuit topologies; among them, ADC is a viable option here given that it encompasses analog and digital considerations while also stipulating insight into high-speed circuits, such as clocking and high-frequency signaling circuits. When determining which ADC architecture to use, for proper support of the upcoming goal of medium resolutions with a GS/s target, the successive approximation register (SAR) ADC was found to be the best choice for the purposes of this study given its considerable energy efficiency and small footprint. The SAR ADC is primarily a digital type of architecture that therefore scales well in conjunction with feature-size scaling given the straightforward architecture it uses. Typically, the SAR ADC includes a front-end analog circuit with a switched-capacitor sampler (e.g., T/H), a comparator, along with a digital-to-analog converter (DAC) for the subsequent digital circuits.

3.2. Step 1: Preparing a Library

Partitioning the entire circuit architecture into multiple modules is the first step in the regression model-based AMS circuit optimization flow, allowing each module to be easily configured and simulated quickly (as mentioned in Section 2.1). A digital circuit typically consists of a SAR ADC architecture including a few analog blocks, such as a comparator, which is an appropriate candidate for a proof-of-concept, as shown in Figure 2. To evaluate the SAR ADC performance, the figure-of-merit (FoM) index is defined as follows:

$$\text{FoM} = \frac{\text{Power dissipation}}{2^{(SNDR-1.76)/6.02} \times F_{sample}}, \tag{1}$$

$$SNDR = 10 \cdot log_{10}\left(\frac{\text{P}_{\text{signal}}}{\text{P}_{\text{T/H}} + \text{P}_{\text{comparator}} + \text{P}_{\text{Quantization}}}\right). \tag{2}$$

In this work, the SAR ADC architecture is divided into T/H, timing controller, and comparator circuits, as shown in Figure 2. These three modules are then respectively parameterized to create a module library while covering the target design space. The module library can be simulated with different combinations of parameters to achieve the target performance.
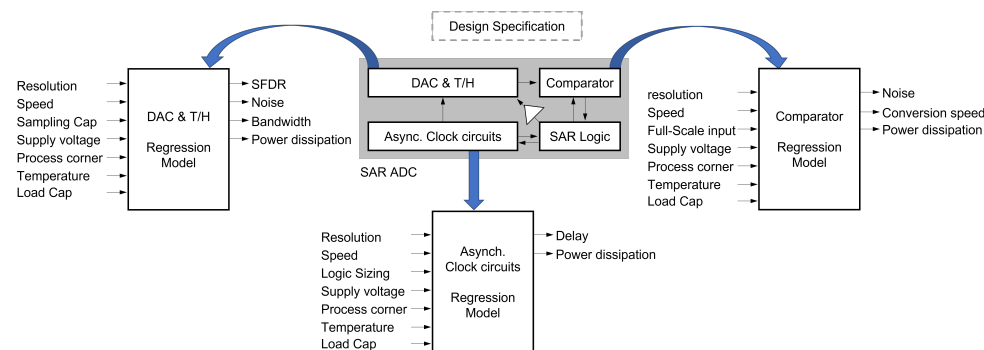

Figure 2. SAR ADC sub-module breakdown and regression models.

3.3. Step 2: Creating Sub-Module with User Intent

As elaborated in Section 2.2, in order to achieve the precisely desired system-level performance of the final assembly, accurate sub-module characterization is important for every sub-module composing the entire ADC. Each module is considered a 'black box' while having a relationship between 'parameters' and 'metrics'. Note that 'parameter' presents the group of design inputs, and 'metrics' presents the output performance. As the digital circuit can leverage the existing design optimization methods, only a module training process for the analog circuits has been applied. Regarding the given search space during a training process, a smart way to select a 'training' set is needed because the module training is not able to cover overall search space. In this work, randomly chosen training samples are used for module characterization, and the range of the training samples is provided by existing known good designs. Based on the 1500 training samples uniformly and randomly selected from the given search space, we created the parameterized module library and collected their output performance metrics using SPICE simulations.

In this work, a neural network comprising multiple hidden layers [27,28] is developed by using the aforementioned training dataset. Moreover, the constructed module library expands the search space of each module for predicting non-present module configurations to compensate for an insufficient training dataset. Depending on the input parameters, multiple input neurons and 30 neurons in the hidden layers are arranged. The number of output neurons is followed by the number of output performance metrics. Consequently, 90% of the dataset was used for the neural network training, and the remaining 10% was used for accuracy validation.

3.3.1. Track-and-Hold Circuit

A transmission gate with a sampling capacitor (C_S) forms a simple top-plate track-and-hold (T/H) circuit. Since the T/H is a fundamental switched capacitor element, it is an appropriate candidate to which to apply the proposed design methodology. Figure 3a illustrates the non-linear transfer function of the T/H. The linearity performance of the T/H can be enhanced by a properly chosen transmission gate sizing, which results in the highest linearity performance with the reduced non-linear capacitance, as shown in Figure 3b. As a result, the properly selected input parameter with well-defined target output performance metrics enabled us to create the regression model of the T/H circuit. As summarized in Tables 1 and 2, as input parameters, we defined the ranges of input signal frequency, sampling speed, supply voltage, input signal swing, sampling capacitor, load capacitor, aspect ratio of the transmission gate, process corner, and temperature. The harmonic distortion, the effective number of bits (ENOB), the noise power, and the bandwidth are defined as performance output metrics.
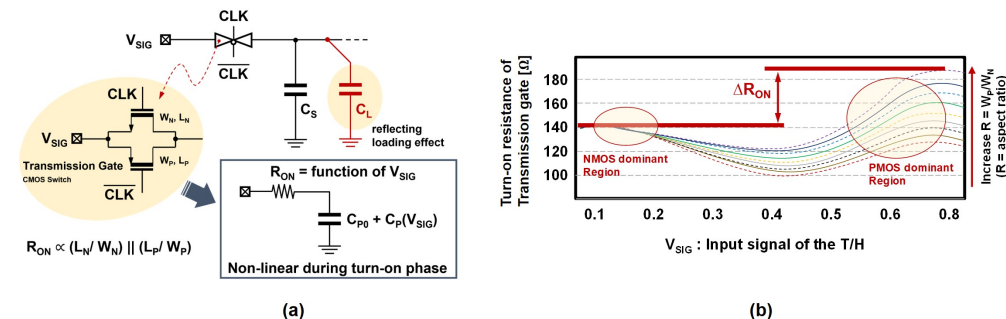

Figure 3. (**a**) Schematic of sampling network (T/H) and (**b**) turn-on resistance of transmission gate with different transistor aspect ratios; data from [22].

Table 1. Design input parameters of the T/H module.

Input Parameter	Variable Range	Unit
Max[input signal frequency]	0.75~1.2	GHz
Sampling speed	1.5~2.5	GHz
Supply voltage	0.75~0.85	V
Max[input signal swing]	1.4	Vpp
Sampling capacitor	2.0~30	fF
Load capacitor	2~10	fF
Aspect ratio[Sampling switch]	0.25~4.0	V
Process corner	SS, TT, FF	-
Temperature	−40~120	°C

Table 2. Performance output matrix of the T/H module.

Output Matrix	Unit
Harmonic Distortion	dBc
ENOB	bit
Noise Power	V^2
Bandwidth	GHz

The input signal sampling bandwidth is one of the most important performance indexes in the T/H circuit. The turn-on resistance (R_{ON}) values of the transmission gate and attached capacitor C_S are dominantly determined by the given input signal bandwidth specification. As the C_S size is generally defined by the required thermal noise level (i.e., kT/C), the turn-on resistance property associated with the practical parasitic determines the dynamic performance of the T/H. According to the operational principle of the T/H, the transfer function in the s-domain ($H_{T/H}$) can be expressed as follows:

$$H_{T/H}(s) = \frac{1}{1 + s \cdot R(V_{SIG}) \cdot [C_S + C_L + C_{PO} + C_P(V_{SIG})]} \tag{3}$$

where the non-linear resistance (R) and parasitic capacitance (C_P) are changed by the magnitude of an input signal V_{SIG}. In this example, there exists a controversial relationship between the non-linear components R and C_P. In order to reduce one of non-linear portions, the other portions will grow until an optimum size at which to realize maximum linearity is reached. However, considering process variations, it is difficult to select a sampling switch size that satisfies all the corner conditions. Here, we defined seven input parameters—in this case, the process corners (SS, TT, FF), a supply voltage variation, the input signal common mode voltage, the transmission gate sizes (PMOS, NMOS), the sampling capacitor size (C_S), and the output load (C_L). Six output parameters of SFDR and ENOB for all three corners are defined.

Table 3 shows evaluated errors in percentile after different numbers (500, 1000, 1500, and 2000) of training sets of the ANN are used. Here, we used 90% of 4096 randomly generated training references from the SPICE simulation, with the remaining 10% of references used to verify the accuracy. In this sub-module, two hidden layers with ten neurons for each layer and an ELU function [29] as an activation function are applied. The target performance of the T/H circuit is >8 ENOB at all process corners. As shown in Figure 4, even when the other parameters—in this case, the sampling and load capacitance, input common mode level, and supply voltage—are varied, the aspect ratio of 2.75 for the sampling switch mainly contributes to the achievement of peak dynamic performance. Considering the SFDR and ENOB at the optimum points, the T/H performances were not constrained by harmonic distortion.

Table 3. ANN regression accuracy of the T/H module (ENOB).

Number of Epoch		Error		Unit
500	4.9	%
1000	3.1	%
1500	2.6	%
2000	1.7	%

(a)

(b)
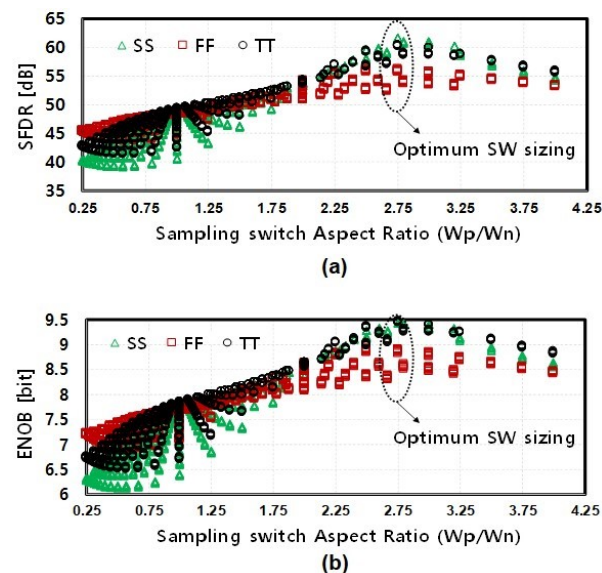
Figure 4. (**a**) T/H circuit's linearity performance (SFDR) and (**b**) resolution (ENOB) performance.

3.3.2. Comparator

The comparator converts the input voltage into a digital code. Here, the input signal is provided by the front-end T/H circuit or a reference switch network during the SAR charge redistribution procedure. In order to minimize both the active area and power dissipation, a regenerative strong-arm comparator topology is widely used, as shown in Figure 5a. The clocked comparator initially stays in a reset mode ($\overline{\text{ENV}}_{\text{comp}}$ is off) and then resolves the differential output using a built-in regenerative latch circuit ($\overline{\text{ENV}}_{\text{comp}}$ is on). Furthermore, we can divide the latter resolving phase into sampling and regeneration phases. The sampling phase begins with the comparator-enabled signal and ends with an established output voltage, which turns on the back-to-back placed regenerative latch. Afterward, the comparator causes the differential output to be fully stretched; thus, one of the comparator outputs is equal to the supply voltage (VDD) but the other decreases to the ground at the end of the regeneration time, as illustrated in Figure 5b. During the regeneration time, the stretched down signal causes the ready signal (RDY) to be flagged; thus, we can measure the comparator resolving time or speed.

Here, we define certain input parameters, including the process corners (SS, TT, FF), a supply voltage variation, grouped and scaled comparator transistor sizes (input, regenerative cross-coupled pairs, and reset switch), load capacitor, and temperature, as summarized in Table 4. Here, the regenerative cross-coupled pairs' size increases the regeneration strength, and the reset switch is partially related to the noise power level. Moreover, we set the performance output metrics of the comparator (Table 5), the noise power, the power dissipation, and the conversion speed. In comparator design, we can ignore the linearity performance as we are only interested in the polarity against the input signal, and the unit transistor size for the comparator core circuit is selected by an empirical design reference to reduce the search space during the development of the regression model.
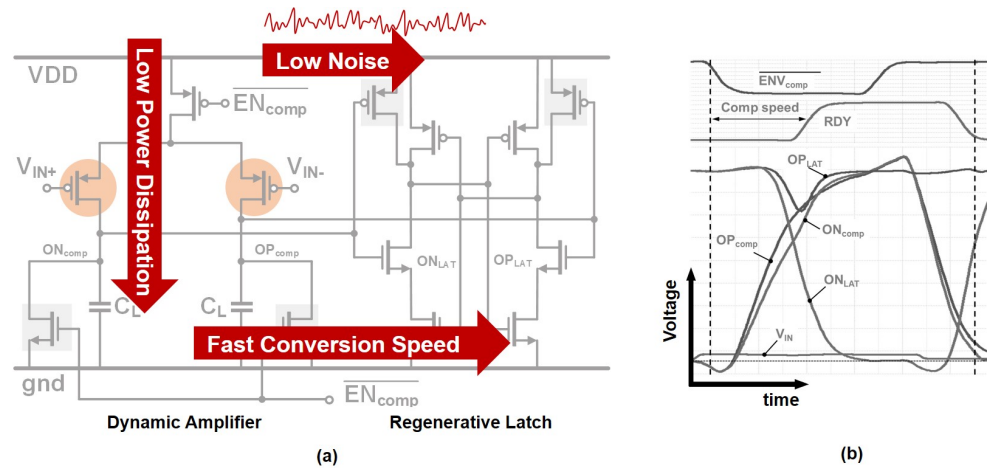
Figure 5. (**a**) Schematic of comparator and (**b**) waveform.

Table 4. Design input parameters of the comparator module.

Input Parameter	Variable Range	Unit
Operating speed	50~150	psec
Supply voltage	0.75~0.85	V
Input transistor size	1~8	scale
Regeneration strength	1~8	scale
Reset switch size	1~4	scale
Load capacitor size	2~10	fF
Process corner	SS, TT, FF	-
Temperature	−40~120	°C

Table 5. Performance output metrics of the comparator module.

Output Metrics	Unit
Noise power	V^2
Poser dissipation	W
Speed	psec

Regarding the comparator noise and conversion speed evaluations, we measured the entire circuit noise at different target speeds. According to an analysis of the comparator noise ($P_{CMP,noise}$) and operating speed (τ_{CMP}), we found that there is a trade-off relationship between these two output metrics, as follows:

$$\tau_{CMP} \propto \alpha_1 \frac{g_m V_{th}}{I_{CMP}} + \alpha_2 \frac{C_L}{g_m} + \alpha_3 ln\left(\frac{VDD}{G_{CMP}V_{IN}}\right) \tag{4}$$

$$P_{CMP,noise} \propto \beta_1 \frac{8kTI_{CMP}}{g_m C_{IN} V_{th}} + \beta_2 \frac{2kT}{C_{IN}G_{CMP}^2} \tag{5}$$

where $g_m, C_{IN}, C_L, V_{th}, VDD, I_{CMP}, G_{CMP}$, k, and T are correspondingly the transconductance, input and output capacitance, threshold voltage of regenerative pair devices, supply voltage, drain current, comparator voltage gain during the sampling phase, Boltzmann constant, and temperature. The α and β coefficients are topology-dependent scaling constants.

To develop an ANN regression model with the comparator input parameters and output metrics, we trained it more than 2000 times with uniformly and randomly selected training references from the SPICE simulation results. Here, four hidden layers with 16 neurons for each layer and the ELU function activation function are employed due to the increased circuit complexity in comparison with the above T/H example. The target

performance of the comparator is a speed of 2 to 2.5 GS/s with more than eight ENOBs at all process corners. Figure 6 shows the ANN regression accuracy of the regenerative strong-arm comparator in terms of the conversion speed (resolving time), power dissipation, and noise power in the CDF expressions. It shows challenges in the areas of the comparator noise model rather than the power dissipation or speed metrics.
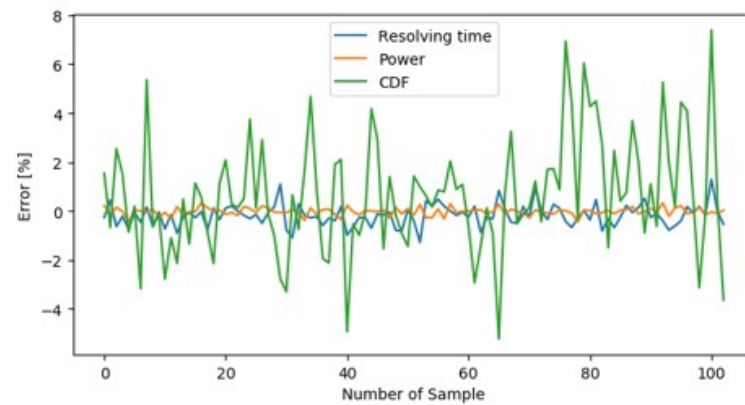

Figure 6. ANN regression accuracy of the comparator.

3.3.3. SAR ADC Timing Controller

A schematic of an SAR ADC timing controller consisting of variable delay cells is shown in Figure 7. In order to implement an asynchronous SAR operation, the delay cell creates voltage-dependent delayed pulses associated with the supporting digital circuits. The conversion time for a typical *N*-bit resolution SAR ADC is calculated by adding an input signal tracking-or-sampling time ($T_{T/H}$), a charge redistribution time in capacitive DAC (C-DAC) during the comparator reset period (T_{RS}), resolving time of the comparator (T_{CMP}), and logic delay time (T_{Logic}). A single period of the ADC operation (T_{Period}) can be calculated as follows:

$$T_{Period} = T_{T/H} + \sum_{i=1}^{i=N} \left(T_{CMP}[i] + T_{RS} + T_{Logic} \right) \tag{6}$$

T_{CMP} is already covered by the comparator, and T_{Logic} is generally determined once the technology has been decided. Therefore, the remaining T_{RS} must be optimized by selecting the proper size of the delay cell. In contrast with the former circuits, the timing controller behaves as a digital circuit and is relatively simpler in terms of performance predictions. We defined several input parameters, including the process corners (SS, TT, FF), supply voltage variation, scaled logic gate size, load capacitor, and temperature (Table 6). Since the SAR ADC timing controller includes both analog and digital circuits, such as mixed-mode circuits, we can set the aspect ratio (i.e., ratio between width and length of the transistor) and leverage the scaling factor as denoted in a unit of a logic gate size. In addition, the power dissipation, scaled active area, and conversion speed were set as the performance output metrics of the SAR ADC timing controller, as summarized in Table 7. Note that the digital circuit prioritizes the silicon occupation factor since it can be normalized.

Table 6. Design input parameters of the asynchronous clock control module.

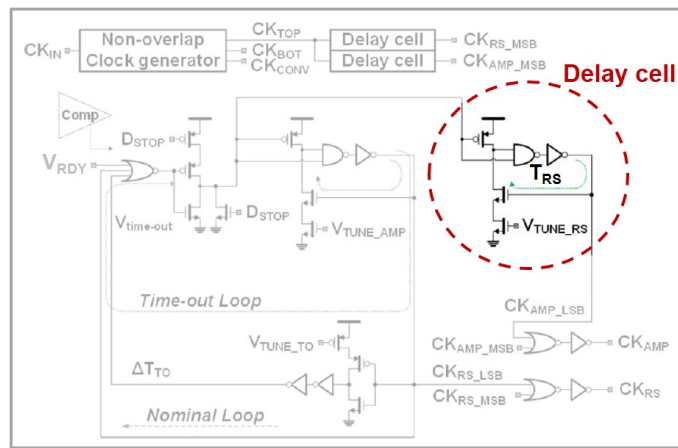| Input Parameter	Variable Range	Unit
Supply voltage	0.7~0.9	V
Logic gate size	1~25	scale
Load capacitor size	2~10	fF
Process corner	SS, TT, FF	-
Temperature	−40~120	°C

Figure 7. Schematic of SAR ADC timing controller consisting of variable delay cells.

Table 7. Performance output metrics of the asynchronous clock control module.

Output Metrics	Unit
Power dissipation	W
Area	scale
Speed	psec

The performance of the SAR ADC timing controller is evaluated in terms of its ability to predict the active area, power dissipation, and load condition trade-off, as shown in Figure 8. According to the results shown in Figure 8a, the overall power consumption is increased by larger device size, which would increase the loading capacitor on a driving circuit. Figure 8b shows measured delay variations at ±100 mV supply voltage change. Although the higher supply voltage would lead to a wide range of controllable delay in time, it requires more power dissipation and undesired delay variations. According to the logic gate size, a duty cycle of the control pulse was evaluated, as shown in Figure 8c. An increasing logic gate size can reduce the pulse duty cycle variation, and an optimum logic gate size can be defined by the first-order derivative of the logic gate size versus the duty cycle variation range relationship.

After the generation of the regression model for the SAR ADC timing controller is complete, delay and duty cycle variations are checked in comparison with the SPICE simulation results. Since an energy-efficient delay controller design eventually saves a large portion of dynamic power dissipation of the entire SAR ADC, a reliable SAR ADC timing controller design with low-power consumption is critical. Therefore, the proper logic gate sizing would be executed by the target user-defined specifications.
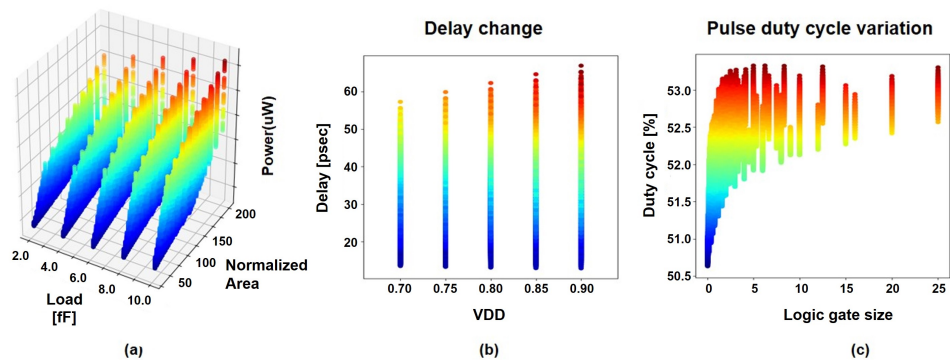

Figure 8. (**a**) Evaluated area/power dissipation/load (parasitic) relationship of the SAR ADC timing controller, (**b**) delay change, and (**c**) pulse duty cycle variation.

3.4. Step 3 and 4: Evaluating Performance and Sensitivity and Generating Final Netlist

In this work, we aim to build a regression model-based circuit design flow. Based on the user intent submitted to the system, the desired design flow automatically selects corresponding modules for the target application. Given the user intents, such as the desired ENOB, the conversion rate, and the required input signal bandwidth, all the module specifications are calculated from the high-level design analysis; thus, the module library can find each candidate in the asynchronous SAR ADC design, as shown in Figure 9. Compatibility is checked through appropriate boundary conditions (i.e., searching for applicable input and output load conditions). Therefore, we follow a design flow to attain the best candidate, using a variety of selection criteria and priorities with respect to the required high-level specifications that users provide. Based on the sensitivity check procedure (mentioned in Section 2.3), a system-level performance variation chart is devised as a result of weight parameter expansion and perturbation. Consequently, the user can choose the desired final netlist (related to Section 2.4). The circuit optimization flow is finally validated against a set of designs by conducting individual performance evaluations.
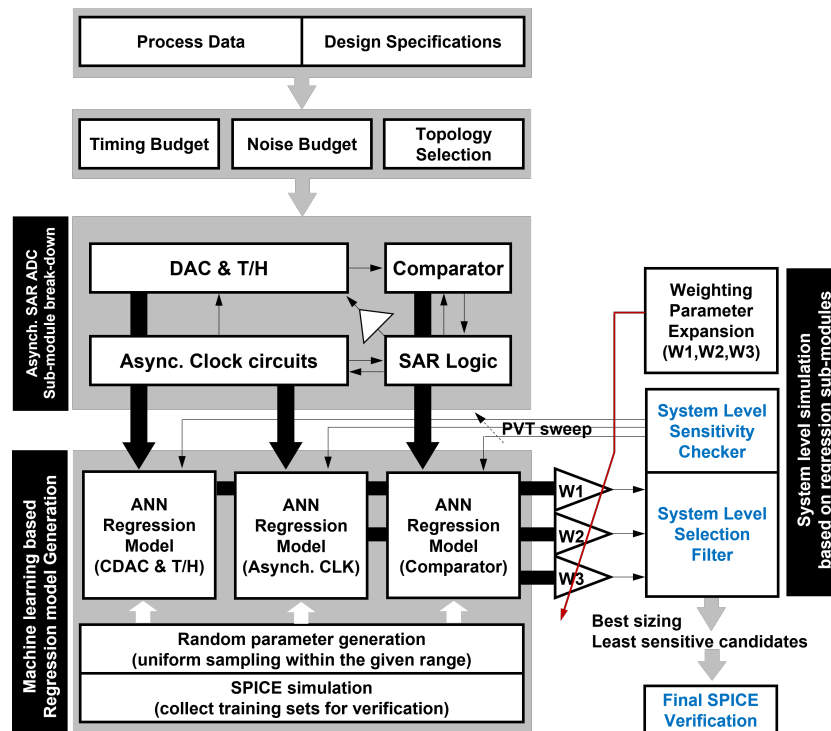

Figure 9. Regression model (ANN)-based asynchronous SAR ADC design flow.

4. Simulation Results

Figure 10 shows a performance plot from the final verification step in our AMS design flow. The target specification is 8-bit 2-GS/s; thus, the Nyquist input signal bandwidth is 1 GHz. Although the final performance at the Nyquist input frequency is slightly lower than that of the target ENOB, we achieved remarkable energy efficiency (<15 fJ/conversion step), as defined by the figure-of-merit (FoM). Moreover, the final result of the sensitivity check was determined under PVT variations, as shown in Figure 11. According to the process and temperature sweep test to confirm our design flow step 3 and 4 (refer to Section 3.4), the result proves the robust operation of the proposed design given the absence of remarkable performance degradation. However, the supply voltage sweep clearly shows a performance drop at a supply voltage of 0.75 V. This is mainly caused by deterioration of the speed and linearity of the transistor in the front-end T/H circuit, which occurs when the power supply voltage is reduced. Although the achieved ENOB is lower than the target level, the

ADC energy efficiency indicates that it has been optimized to perform best in any given situation.

In addition, we prepared three ADC specifications with different ADC resolutions, conversion speeds, and process conditions in order to check whether the proposed optimization method works well for different requirements. Table 8 summarizes and compares the SAR ADC performance of the proposed optimization method with the SPICE simulation results at the different target operating conditions, respectively. Here, the SPICE simulation results (in Table 8) are gold-standard references to evaluate our achieved SAR ADC performance. In essence, the error percentage (in Table 8) represents the accuracy loss in our approach. The proposed AMS optimization technique achieved excellent ADC performance and showed acceptably creditable accuracy. In the comparison of the proposed AMS circuit optimization method and SPICE-based approach, errors of 17.2% and 12.8% can be ignored considering that the ADC FoM generally stays around 15~20 fF/conversion step in an 8-bit 1.5-GS/s SAR ADC. Other than these errors, the overall accuracy of our proposed approach results is 90% or more.
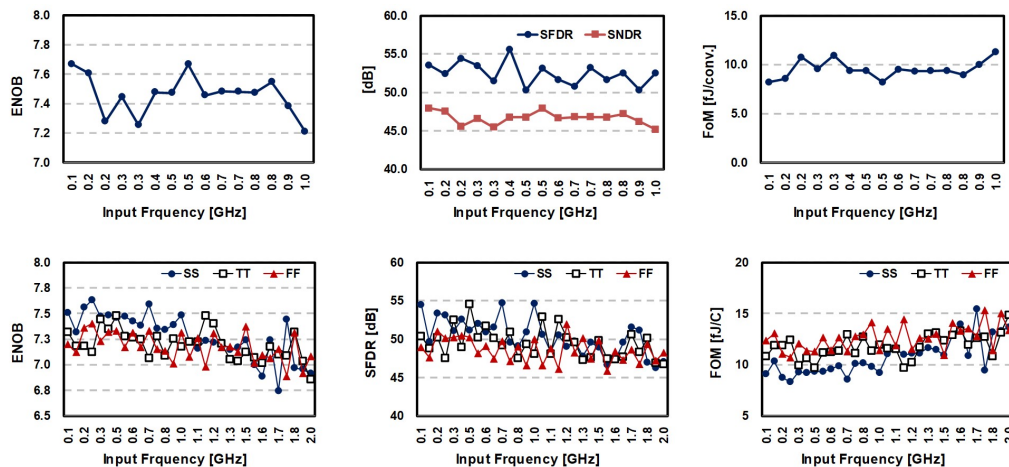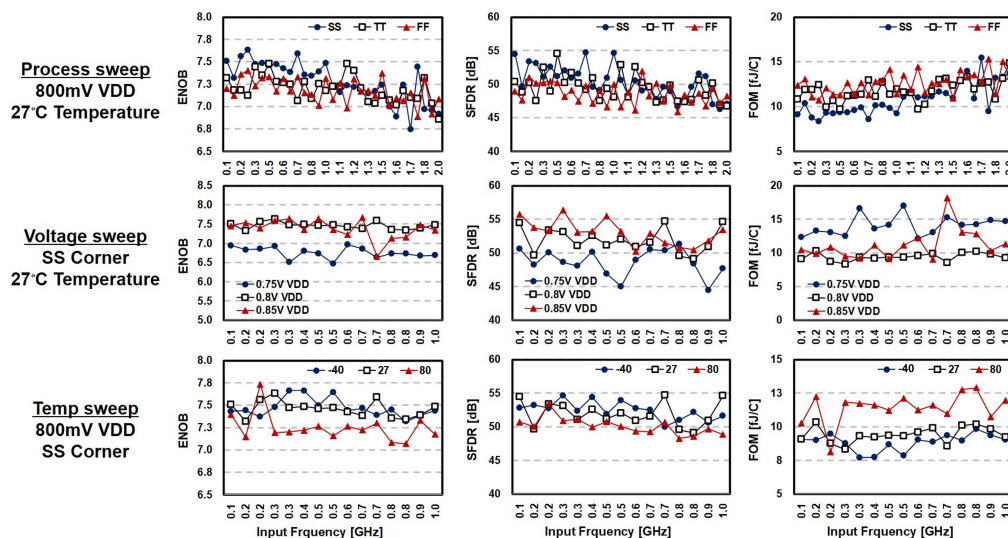

Figure 10. Performance plots.

Figure 11. Sensitivity check over PVT variations.

Table 8. Figure-of-merit comparisons at each target ADC specification; data from [22].

Spec.	Corner	SPICE Sim. FoM(fJ/c.s)	AMS Sim. FoM(fJ/c.s)	Error %
8-bit 1.5-GS/s	SS	6.8	5.8	17.2
	TT	6.0	5.5	9.1
	FF	5.3	4.7	12.8
8-bit 2.0-GS/s	SS	12.5	11.9	5.04
	TT	9.8	9.1	7.7
	FF	11.8	9.9	7.7
6-bit 2.5-GS/s	SS	12.2	11.8	3.4
	TT	10.0	9.2	8.7
	FF	8.5	7.7	10.4

5. Discussion and Future Research Orientations

By adopting a regression-model-based AMS design flow instead of an expensive SPICE simulator from the initial design phase, the circuit design time can be effectively reduced. However, ambiguities exist when determining the appropriate number of reference samples, especially during the development of known good design-based libraries. Because the performance of an ANN model depends on the number of reference samples, deriving an appropriate number of samples through an empirical study or selecting an effective sampling method can be an important factor in this method. Moreover, uniform input sampling over a given range can degrade the accuracy of the regressor because more training samples are required to approximate a sudden sharp surface. In this work, a manually defined range of input parameters with uniform sampling was inevitably applied to focus more on our AMS design flow. Hence, in order to resolve this limitation, we plan to study the design and application of an adaptive input data sampling algorithm as a future study. In addition, employing a higher-level transfer learning technique would enable our regression-model based optimization flow to be more generalized [30–32]; thus, it is expected to create technological synergy, such as dramatically preventing human error.

6. Conclusions

In this research, we propose a regression model-based AMS circuit design optimization flow utilizing parameterized operating conditions. For proof of concept, an asynchronous SAR ADC considering practical environment changes has been successfully evaluated. First, parameterized module library preparation for characterizing module-level operation is performed to apply the scheme to the enlarged design space. Subsequently, a regression model based on an ANN is trained to extract the representative features of modules for the target design space. Afterward, the performance sensitivity is assessed to ensure that the system can meet the user-intended PVT variation target. Lastly, a final performance evaluation at both the module level and the overall system level is done to validate the effectiveness of the proposed AMS design flow. To reflect the design complexity, an advanced technology 14 nm predicted process design kit is used. Given the skewed PVT conditions, the design output successfully shows robust operation of the asynchronous SAR ADC without instances of abrupt performance degradation.

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