A Low-Power Class-C Voltage-Controlled Oscillator with Robust Start-Up and Compact High-Q Capacitor Array

Young-Kyun Cho, *Member, IEEE*, Jae-Won Nam, and Sang-Won Lee

***Abstract*—This brief presents a class-C voltage-controlled oscillator (VCO) that ensures a robust start-up with low phase noise and high power efficiency. The proposed start-up scheme, which uses a voltage converter that operates according to the output state, relieves the start-up difficulty by supplying a time-varying bias voltage to the core transistors and allows the VCO to operate in an optimal state. The start-up circuitry is enabled only during initial operation, so power efficiency is improved without phase noise degradation. Furthermore, a capacitor array with a high quality factor is implemented by a direct capacitor connection that exhibits low series resistance. Fabricated with a 65-nm CMOS, the VCO demonstrates a frequency tuning range of 13.1% from 19.3 to 22.0 GHz. The measured minimum phase noise at a 1-MHz offset is –106.33 dBc/Hz at an oscillation frequency of 19.7 GHz, while dissipating 3.8-mW of power from a 1.0-V supply. The VCO occupies an active area of 0.064 mm^2. It reveals a figure-of-merit and figure-of-merit with area of –186.4 and –198.3 dBc/Hz, respectively.**

***Index Terms*—Millimeter-wave oscillator, class-C voltage-controlled oscillator, start-up, quality factor, capacitor array.**

I. Introduction

THE millimeter wave (mm-wave) bands are considered to improve the capability of high data rate wireless communication owing to their widely available bandwidths. In particular, the explosive increase in on-board Internet connectivity in high-speed mobile environments, including buses, trains, and subways, is accelerating the development of high-performance transceivers within this frequency band [1]. Voltage-controlled oscillators (VCOs) are a fundamental building block in wireless transceivers that provide a local oscillation signal for frequency conversion. In general, the system performance is affected by the phase noise (PN) and frequency tuning range (FTR) of VCOs.

Several approaches to improve the PN of VCOs have been reported in the literature [2]–[8]. Among them, class-C VCOs show better PN characteristics than those of conventional LC VCOs by using biasing cross-coupled transistors under a class-C operating condition and by shaping the drain current into an impulse-like waveform with a tail capacitor. However, class-C VCOs exhibit inevitable start-up problems owing to low-gate bias voltage, which causes the transconductance of the cross-coupled differential pair to be too small. The hybrid architecture in [5] addresses this issue by using a class-B input pair placed in parallel with the class-C core. The negative-feedback loop presented in [7] and [8] also optimizes start-up reliability by adaptively adjusting the bias voltage of the core transistors. Although the resulting circuits achieve a powerful start-up even with a fairly low gate bias, the VCO tank is loaded with additional circuitry, which affects both the tank quality factor (Q) and the FTR. Moreover, the additional circuits have to operate continually in a steady-state condition, thereby degrading the PN performance and power efficiency of the VCOs.

A wide tuning range can be obtained for VCOs by employing a parallel combination of MOS varactors and switched capacitors [4], [9]. When the operational frequency increases to the mm-wave band, the quality factor, and therefore the PN performance of the VCO, degrade significantly owing to the lossy silicon substrate and control switches. Extensive efforts have been invested to improve quality factor by adjusting the ON/OFF resistance of the transistor switches, but such attempts inevitably increase the parasitic capacitance, further limiting the FTR [4], [10].

In this brief, we present a class-C VCO using a voltage converter that adaptively adjusts the bias voltage of an input transistor pair to achieve robust start-up and improved PN performance. This start-up scheme relieves start-up difficulty, allowing the VCO to operate in an optimal state. In addition, a simple method to improve the quality factor of the capacitor array is proposed. We organize the remainder of this brief as follows: The proposed VCO structure is described in Section II. The implementation details of the circuits are presented in Section III. The experimental results are presented in Section IV. Finally, the conclusions are discussed in Section V.

II. Proposed VCO Structure

A simplified topology for the proposed oscillator, derived

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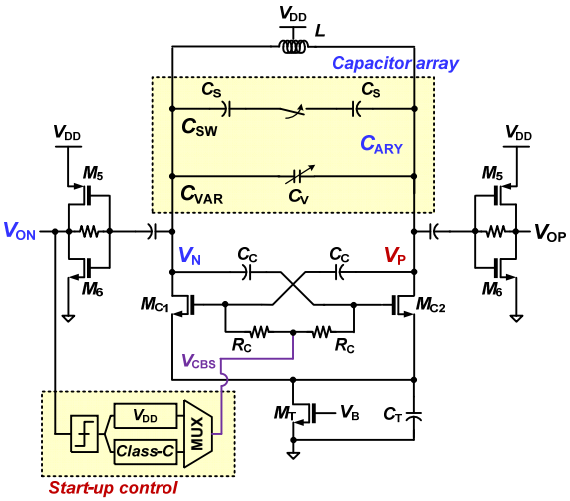

Fig. 1. Proposed voltage-controlled oscillator with start-up control.

from that of traditional class-C oscillators, is shown in Fig. 1. The inductance is optimized for the lowest achievable PN. A small single-turn 275-pH inductor L is used, and the center tap of the inductor is connected to a supply voltage V_{DD} of 1V. The simulated quality factor of the designed inductor is approximately 19.5 at 20.5 GHz. A combination of a switched capacitor bank, C_{SW}, and a varactor, C_{VAR}, is employed as a capacitor array, C_{ARY}, to tune the oscillation frequency band from 19 to 22 GHz. The cross-coupled NMOS transistors (M_{C1} and M_{C2}) form a positive feedback loop that induces negative transconductance to maintain the oscillation. The tail transistor M_T comprises a VCO bias circuit, which is a digitally controlled current source that helps obtain the desired control of power consumption and PN. The common source capacitance C_T enforces full class-C operation by shaping the drain current into tall and narrow pulses and filters out high frequency noise from M_T. An ac-coupled self-biased inverter is used as a buffer to change the output common-mode level from 1 to 0.5 V. To guarantee safe start-up, the bias voltage of the NMOS transistors, V_{CBS}, is initially set to V_{DD}; this allows M_T to be in the saturation regime, enabling vibrant start-up. When the VCO begins to oscillate, a low gate bias voltage for class-C operation is applied to V_{CBS}. The detailed operation of the proposed start-up control scheme is discussed in the next section.

III. Circuit Implementations

A. Start-Up Circuit

The proposed automatic start-up circuit is shown in Fig. 2(a). The loop comprises a voltage converter, oscillation detector [11], and simple digital logic. Fig. 2(b) presents a simulated waveform to illustrate the operation of the start-up procedure.

During the initial stage (0 < T <50 ns), dc power is supplied to the circuits, and the VCO does not oscillate. The output of the self-bias buffer V_{ON} in Fig. 1 reaches a value between the two reference voltages V_H and V_L of the hysteresis comparator, the comparators output LOW, and the oscillation detector output OS_{EN} becomes HIGH. As OS_{EN} drives the switch M_4 of the voltage converter, the input V_I and output V_O of the inverter become GND and V_{DD}, respectively. Therefore, V_{DD} is used as the initial value for the gate of cross-coupled transistors,

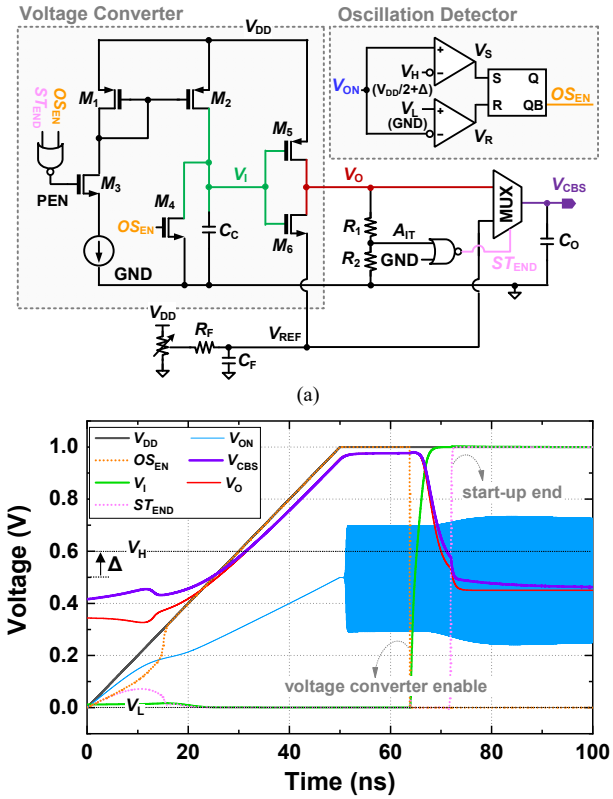

Fig. 2. Start-up circuit. (a) Schematic diagram. (b) Simulated waveform.

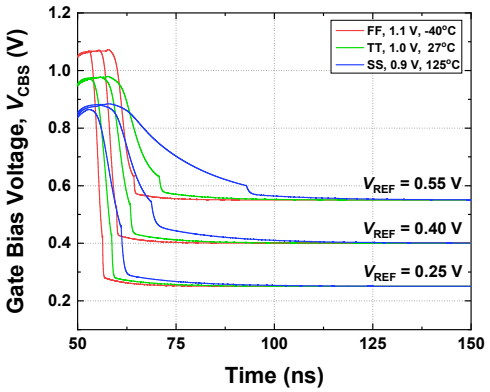

Fig. 3. Start-up characteristic for PVT variations.

enabling a safe and swift start-up (T ~ 52 ns). After start-up (52 ns < T < 71 ns), V_{ON} exceeds V_H, the high-side comparator outputs HIGH, and OS_{EN} becomes LOW; then, the voltage converter is enabled. The capacitor C_C starts to charge and the voltage across it finally increases to V_{DD}. As V_I increases, V_O falls to the externally applied reference voltage V_{REF}. Hence, the output voltage of the start-up V_{CBS} follows V_{REF}. Note that the source terminal of M_6 is connected to V_{REF} instead of GND; therefore, when the voltage converter is charged, its output becomes V_{REF}, which drives the input switching pair of the VCO to operate under class-C conditions. At the end of the transient state (T > 71 ns), the start-up circuit enforces V_{CBS} ~ V_{REF} to produce the required V_{CBS} in a steady-state for class-C operation. It can be seen that when V_{CBS} is decreased, the amplitude of the VCO output increases due to the reduction of

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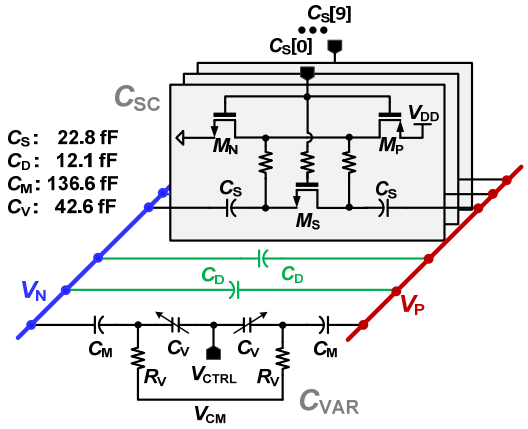

Fig. 4. Proposed capacitor array with additional small capacitor C_D.

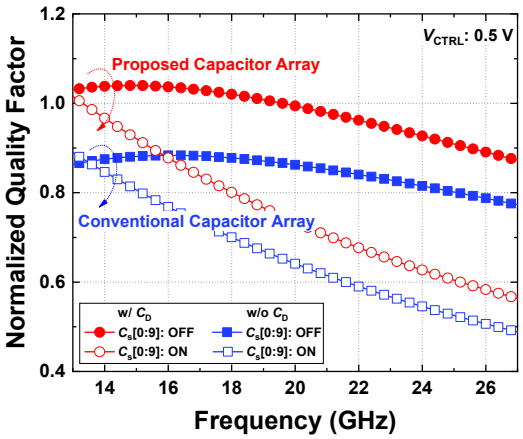

Fig. 5. Effect of C_D on simulated capacitor-array quality factor.

gate-drain parasitic capacitance of input transistors [12]. To switch V_{CBS} from V_O to V_{REF}, V_O is applied to the NOR gate via a resistor divider to ensure an exact LOW state. Then a multiplexer control signal ST_{END} is generated, and the start-up operation is terminated. With ST_{END}, the voltage converter and oscillation detector are disabled, and V_{CBS} is maintained at a constant setting. As a result, the output of the start-up is dynamically adjusted and is provided as a bias voltage for input transistors. V_{REF} should be adjusted according to process-voltage-temperature (PVT) variations to optimize PN. V_{REF} is controlled externally with variable resistor and low-pass filter (LPF) as shown in Fig. 2(a). The LPF filters out potential noise from the external voltage source. It is worth noting that although this scheme easily produces a stable V_{REF}, its supply should be carefully considered because the phase noise is highly dependent on it. Fig. 3 shows the start-up characteristics of gate bias for several values of V_{REF}. The proposed start-up loop can stably generate V_{CBS} when V_{REF} ranges from 0.25 to 0.55 V regardless of PVT variations.

This start-up scheme has several advantages when compared with conventional techniques. First, it is simple to design and does not have complicated feedback circuitry, such as a peak detector, operational amplifier, or various digital blocks [6]–[8]. Both the start-up transient and PN can be affected by the non-linearity and complexity of the feedback; hence, a simpler circuit can lead to improved results. Second, it is possible to reduce the loading of the VCO resonator, which affects the tank quality factor and the tuning range by detecting oscillation through a self-biased buffer. Moreover, the input transistors can be sized to provide only sufficient transconductance to ensure start-up, further reducing parasitic capacitance and current consumption. Finally, the proposed approach does not require constant current consumption by the start-up circuit, and it leads to very low noise, because all active components are disabled after start-up.

B. Capacitor Array

Generally, a VCO capacitor array consists of a parallel combination of varactors, C_{VAR}, and of switched capacitors, C_{SC}, for a wide FTR [9]. At mm-wave frequency bands, the quality factor of capacitor array Q_C is significantly reduced because of the low Q of the varactors and switched capacitors. The quality factor of the capacitor array can be obtained from

$$\frac{1}{Q_C} = \frac{1}{Q_{C,VAR}} + \frac{1}{Q_{C,SC}} = \omega R_{S,VAR} C_{VAR} + \omega R_{S,SC} C_{SC}, \quad (1)$$

where $Q_{C,VAR}$ and $Q_{C,SC}$ are the quality factors of varactors and switched capacitors, respectively, and $R_{S,VAR}$ and $R_{S,SC}$ are the series resistances of varactors and switched capacitors, respectively.

In order to improve Q_C, it is essential to reduce the series resistance of the varactors and switched capacitors. The value of $R_{S,VAR}$ can be improved by reducing the varactor size. The value of $R_{S,SC}$, which is dominated by the switch channel resistance, can be reduced by increasing the width of the switch transistor [10]. However, these methods inevitably increase the ratio of the parasitic capacitance, which decreases the achievable tuning range.

To mitigate this problem, an additional small capacitor, C_D, is added to the capacitor array to enhance the quality factor, as shown in Fig 4. Metal-oxide-metal (MoM) capacitors are chosen for C_D as well as the C_M and C_S of the varactor and switched capacitor, because these capacitors formed with multiple metal layers have a capacitance density comparable to that of MOS capacitors and show improved linearity owing to their lower leakage current [13]. C_D is composed of metal 5, 6, and 7 as parallel conductors with a finger width and space of 100 nm and a number of horizontal and vertical fingers of 10 and 22, respectively. It has a capacitance of 12.1 fF and a series resistance of 2.1Ω at 20.5 GHz, exhibiting a high quality factor. Because this capacitor is connected in parallel with C_{VAR} and C_{SC}, which have relatively high series resistances ($R_{S,VAR}$ and $R_{S,SC}$), the total series resistance of the capacitor array can be reduced. Although C_D increases the total capacitance of the capacitor array, it can improve Q_C by drastically reducing the series resistance. Moreover, thanks to the similarity between C_D and C_S in device configuration, the same amount of parameter change is expected from PVT variations. This indicates that Q_C can be preserved by the relative matching property of the MoM device, rather than by implementing C_D in different ways.

Fig. 5 shows the simulated quality factor of the capacitor array with and without C_D. When a capacitor with a small series resistance is directly connected between the output nodes V_P and V_N, the quality factor is improved by more than 15% at all

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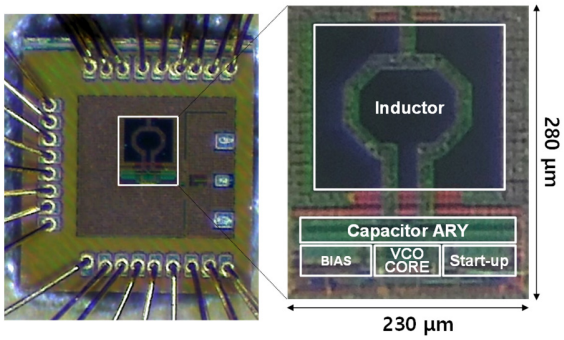

Fig. 6. Die micrograph.

Fig. 7. Transient waveform of the start-up procedure.

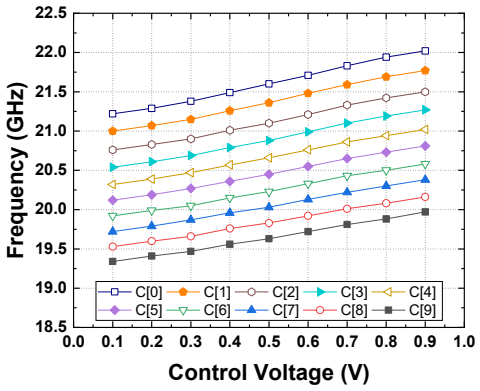

Fig. 8. Measured frequency tuning range.

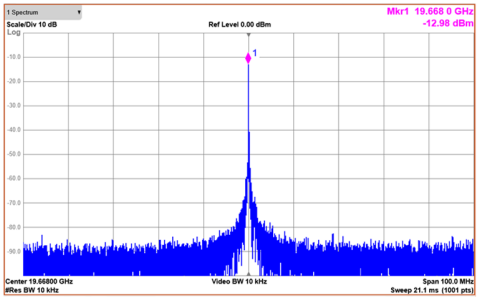

Fig. 9. Measured frequency spectrum at 19.7 GHz.

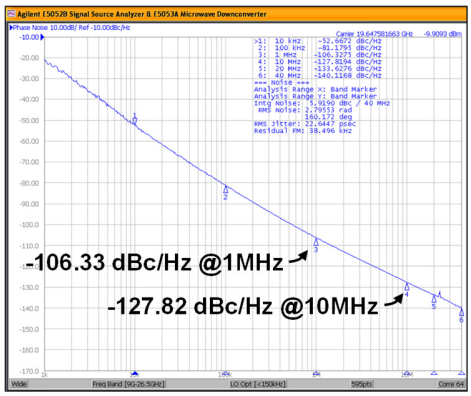

Fig. 10. Measured phase noise characteristic at 19.7 GHz.

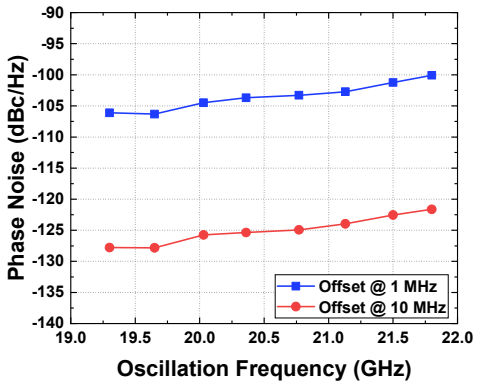

Fig. 11. Measured PN at 1- and 10-MHz offsets against oscillation frequency.

operating frequencies, albeit at the expense of a slight penalty in total capacitance.

IV. Measurement Results

The proposed class-C VCO was implemented using a 65 nm CMOS; a die photograph of it is shown in Fig. 6. The active area was 0.064 mm^2. As shown in Fig. 6, only one of the differential channel ports was connected to the output pad. The VCO was measured using a Cascade 40 GHz ground-signal-ground probe via on-wafer probing with a corresponding radio frequency cable. This cable was connected to a Keysight EXR054A oscilloscope for transient waveform characterization, to an Agilent N9000A spectrum analyzer for oscillation frequency measurement, and to an Agilent E5052B signal source analyzer with an Agilent E5053A microwave downconverter for PN evaluation. The total power consumption was 3.8 mW from a 1.0-V supply voltage, when the 19.7-GHz output frequency was generated. It was experimentally confirmed that the V_{REF} optimizing PN was in the range of 0.4 to 0.45 V.

The start-up procedure can be verified by measuring the time domain waveform through an oscilloscope, as shown in Fig. 7. Because V_{OUT} was generated thorough multiple-stage buffers configured with self-biased inverters, was loaded by parasitic capacitances, and was captured using a bandwidth-limited oscilloscope, it could not show an output waveform similar to that in Fig. 2(b). However, it may be indirectly inferred that the proposed start-up circuit operated properly.

The measured frequency tuning characteristics of the oscillator are plotted in Fig. 8. The VCO can tune 10 output frequency states, C[0], C[1], …, C[9] with an appropriately set bit status of the switched capacitors. When the controlled voltage was swept from 0.1 to 0.9 V, the oscillation frequency of the VCO varied from 19.3 to 22.0 GHz, thereby exhibiting an FTR of 2.7 GHz; this corresponds to 13.1% of the center

TABLE I
PERFORMANCE COMPARISON TO PRIOR STUDIES

References	This Work	[4]	[5]	[14]	[15]
Frequency (GHz)	19.7	25	19.5	24.25	20.1
FTR (%)	13.1	26	12.7	9.5	4
PN@1MHz (dBc/Hz)	–106.33	–110	–112	–100.79	–105.4
V_{DD} (V)	1	0.95	0.9	1	0.6
Power (mW)	3.8	16	20.7	8	1.4
Area (mm^2)	0.064	0.1	0.07	0.19	0.6
FoM (dBc/Hz)	–186.4	–185.9	–184.6	–179.5	–190.0
FoM_T(dBc/Hz)	–188.8	–194.2	–186.7	–179.0	–182.0
FoM_A (dBc/Hz)	–198.3	–195.9	–196.2	–186.7	–192.2
Process (nm)	65	40	28	65	90
Topology	Class-C	Class-B quadcore	Class-C	Class-C	Transf. feedback

FoM_T = FoM-20log(FTR/10%), FoM_A = FoM +10log(Area/mm^2)

frequency. The oscillation frequencies of adjacent bands sufficiently overlap.

Fig. 9 shows the measured output spectrum of the VCO at a frequency of 19.7 GHz, where the resolution and video bandwidths were both 10 kHz. A measured single-end output power of –12.9 dBm was achieved without de-embedding the cable loss. The measured output spectrum demonstrates low PN and high spectrum purity within the specified frequency span.

The PN curve of the VCO at a carrier frequency of 19.7 GHz is shown in Fig. 10. The PN was –106.33 and –127.82 dBc/Hz at offset frequencies of 1 and 10 MHz, respectively. The measured PN values at offsets of 1 and 10 MHz versus the carrier frequency are plotted in Fig. 11. At the offset frequency of 1 MHz, the best and worst PN values were –106.33 and –100.1 dBc/Hz, respectively. Note that the PN at the offset of 10 MHz degraded by approximately 6.1 dB. These degradations were due to quality factor reduction from an integrated inductor.

Table I compares the performance of the proposed class-C oscillator with that of existing state-of-the-art oscillators [4], [5], [14], [15]. A well-recognized figure-of-merit (FoM) for evaluating a VCO is given in [16]:

$$\text{FoM} = \text{L}\{\Delta f\} - 20log\left(\frac{f_0}{\Delta f}\right) + 10log\left(\frac{P_{DC}}{1mW}\right), \qquad (2)$$

where $\text{L}\{\Delta f\}$ is the PN measured at offset Δf from the carrier frequency f_0, and P_{DC} is the dc power consumption. The FoM of the fabricated VCO was –186.4 dBc/Hz. Furthermore, to adopt more VCO parameters, two additional FoM values, the FoM_T [17] and FoM_A [18], were given as –188.8 and –198.3 dBc/Hz, respectively. The proposed VCO with a robust start-up and high quality factor capacitor array achieves a comparable PN and FTR without using complicated circuitry, resulting in high FoMs.

V. CONCLUSIONS

A low-power class-C VCO was demonstrated using a 65-nm CMOS. Using a proposed start-up circuit with a time-varying bias technique and deactivation function, the required dc power for sustaining VCO oscillations could be effectively minimized without PN degradation. A quality factor enhanced capacitor array also contributed to improving the PN performance. The proposed VCO with robust start-up achieved a PN and FTR comparable to those of existing state-of-the-art oscillators without using complicated functional blocks, and had a competitive FoM and FoM_A. Therefore, the proposed VCO may offer a potentially significant contribution to low-power mm-wave signal generator applications.

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