Four-Bits-Per-Cell Operation in an HfO_2-Based Resistive Switching Device

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The quadruple-level cell technology is demonstrated in an $Au/Al_2O_3/HfO_2/TiN$ resistance switching memory device using the industry-standard incremental step pulse programming (ISPP) and error checking/correction (ECC) methods. With the highly optimistic properties of the tested device, such as self-compliance and gradual set-switching behaviors, the device shows 6σ reliability up to 16 states with a state current gap value of 400 nA for the total allowable programmed current range from 2 to 11 μA. It is demonstrated that the conventional ISPP/ECC can be applied to such resistance switching memory, which may greatly contribute to the commercialization of the device, especially competitively with NAND flash. A relatively minor improvement in the material and circuitry may enable even a five-bits-per-cell technology, which can hardly be imagined in NAND flash, whose state-of-the-art multiple-cell technology is only at three-level (eight states) to this day.

The importance of the high-density nonvolatile memory (NVM) is ever increasing in modern information technology,[1–9] and its most appealing contender is the vertically integrated NAND (v-NAND) flash memory. Memory cell area scaling had been the method of choice for increasing the memory cell density until 2015 (planar NAND or p-NAND), but such strategy has become less competitive compared with vertical integration since then.[10–14] Aside from area scaling or vertical integration, storing multiple data bits in a single cell has been a critical ingredient for the NAND flash,

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which is called "multilevel cell (MLC) technology".[15–18] In the flash memory community, MLC refers to two bits per cell (four memory states), and the triple-level cell (TLC) does three bits per cell (eight memory states). MLC or TLC in a flash memory cell can be acquired by storing different numbers of electrons in the floating gate or charge trap layer, which alters the threshold voltage (V_{th}) of the memory transistor. As the number of data state increases, the margin between the neighboring states becomes smaller because the allowed overall V_{th} range is limited to only several volts, making reliable operation quite challenging. To mitigate such problem, the incremental step pulse programming (ISPP) method is adopted in conjunction with the error checking/correction (ECC) technique,[19,20] although it takes a longer time and higher energy to write a data bit when using such method. Due to the inherent limitation of varying the V_{th} within the allowable overall V_{th} range; however, TLC has been the upper-bound commercial NAND flash, which might not be the case for the resistance switching random-access memory (ReRAM), as shown in this work.

ReRAM, especially in the vertically integrated crossbar array format (v-CBA), has been suggested as the ultimate storage memory device.[21–25] As with the case of v-NAND, however, MLC, TLC, or even quadruple-level cell (QLC) would be necessary for the v-CBA ReRAM to be competitive with the v-NAND device. While the inherent randomness of oxide-based ReRAM memory states mainly due to the defect-related resistance switching mechanism such as the valence change mechanism is a critical drawback of ReRAM compared with the transistor-based flash memory device, the current-sensing mode of ReRAM can provide the unprecedented merit of multiple data storage in a single cell. There have been many reports on the multiple level resistance values (both in the low resistance state (LRS) and the high resistance state (HRS)) in different types of ReRAMs.[26–30] However, if the resistance values vary in log scale, their usefulness is severely limited because the common current-sensing amplifiers detect current in linear scale.[21] Therefore, the available current range for multiple data storage for ReRAM is also limited from the point of view of the circuit. On the other hand, a certain ReRAM material may have a limited resistance (or current) range in which the different levels can be defined, which requires a highly tight control of the resistance (or current) value of each level. In these senses, the adoption of the ISPP and ECC methods is inevitable for implementing TLC or even QLC to ReRAM. The authors searched several different types of ReRAM materials that are suitable for such purposes and discovered that Au/Al_2O_3/HfO_2/TiN devices possess the desirable properties and could demonstrate feasible QLC performance. QLC required 16 different resistance values with a sufficiently narrow distribution for a given state and a sufficiently distinct gap between the states. In NVM, the criteria for stable multiple levels are generally defined as 6σ, and the σ is defined as:

$$\sigma = (m_1 - m_2)/(\sigma_1 + \sigma_2) \quad (1)$$

where m_1, m_2, σ_1, and σ_2 are the mean values of neighboring states 1 and 2 and their standard deviations when the distribution of the data within a state has a normal Gaussian form. 6σ corresponds to an error rate of 1 part per billion, so only one cell malfunctions in the 1 Gb density memory or a given cell fails once during 10^9 operation times. The Au/Al_2O_3/HfO_2/TiN device fulfilled this stringent criterion for QLC, which has not yet been reported from any other ReRAM material to the authors' knowledge.

Figure 1 shows the resistance switching (RS) current–voltage (I–V) curves of the CBA-type Au/Al_2O_3/HfO_2/TiN device, with a junction area of 10 × 10 μm^2 patterned via photolithography and followed wet-etching or lift-off technique. The thicknesses of top electrode (TE) Au, Al_2O_3, HfO_2, and the bottom electrode (BE) TiN were 150, 2, 6, and 100 nm, respectively, whose detailed microstructure properties can be identified from Section SI in the Supporting Information. The TiN BE was reactively sputter deposited

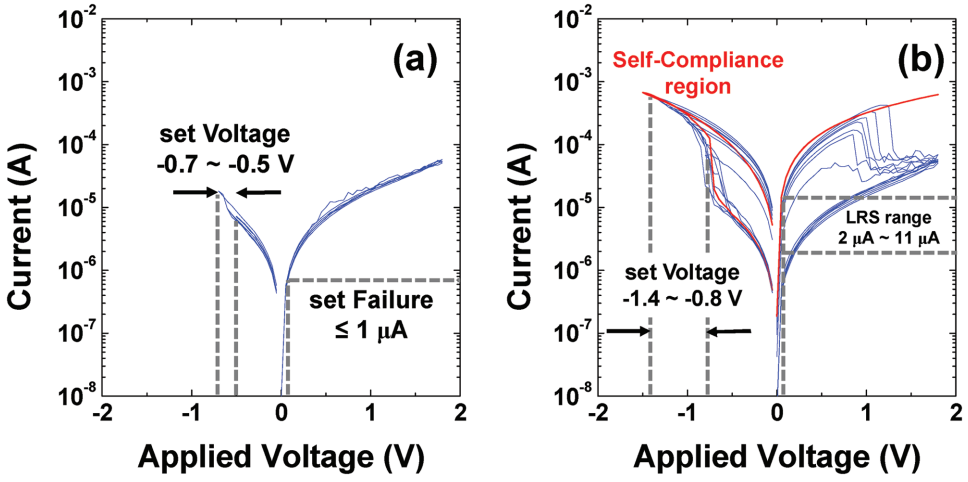

Figure 1. Voltage-bias-dependent RS hysteresis behavior. a) In the –0.5 to –0.7 V set voltage range, significant resistance change was not observed. b) In the –0.8 to –1.4 V set voltage range, obvious gradual resistance change was observed, originating from the self-compliance characteristic. The application of the –1.5 V set voltage increased the HRS, which could bring about the malfunction of the RS device. Overall, it was confirmed that the achievable current range for MLC operation of the given RS device is 2–11 μA.

on the SiO_2/Si wafer and patterned by photolithography and wet-etching process for CBA-type BE. Then, 6 nm thick HfO_2 and 2 nm thick Al_2O_3 were deposited sequentially via atomic layer deposition (ALD) technique. The detailed device fabrication processes were provided in the Experimental Section. The device showed the typical valence change type switching behavior, where the negative bias (applied to Au TE, while TiN BE was grounded) sets (switching from HRS to LRS) and positive bias resets (switching from LRS to HRS) the device after the electroforming at –4.5 V. One of the critical merits of this device is its self-compliance behavior. That is, even without applying external current compliance, the device was not broken down within the stable operation voltage range (–1.4 to +1.8 V), which may be ascribed to the appropriately involved internal resistance (perhaps from the TiN BE).[31–34] There could be a slight oxidation of the TiN BE forming the thin TiO_xN_y interfacial layer during ALD of oxide layers on top. However, TiO_xN_y has a much higher electrical conductivity than those of the ALD oxide layers in this work,[35] so its adverse effect on RS must be minimal. On the other hand, this layer may provide the device with an internal resistance which is essential for the self-compliance characteristic of the given device. As ISPP/ECC must be performed with pulse voltages, current compliance functionalities can hardly be adopted. The other, and the most critical for MLC operation using the ISPP/ECC, is the gradual set-switching behavior shown in the –0.8 to –1.4 V region. If this set switching has been abrupt, the ISPP/ECC will not work very well because the device will easily reach a state where the resistance will already be outside the desired range (see Section SII, Supporting Information, for more details about the ISPP/ECC failure cases).

In this work, when the set voltage was higher than –0.7 V, the set switching was not sufficiently acquired, and the reading current (read at +0.1 V) was lower than 1 μA (Figure 1a), which was almost indistinguishable from the HRS current. Therefore, the upper limit of the set voltage was –0.8 V. When the set voltage was as low as –1.5 V, the device failed to reset in the positive-bias region (as shown by the red curve in Figure 1b), and as such, the lower limit of the set voltage was –1.4 V. Within the allowed set voltage (or programming voltage) range, the achievable reading current (also read at +0.1 V) ranges from 2 to 11 μA. Using these preliminary data on the device performance, multiple-level operation in the ISPP/ECC mode was attempted, as shown in **Figure 2**. It should be noted that the absolute values of the achievable reading current (2–11 μA) are highly favorable for the rapid reading (Johnson–Nyquist limit of reading current)[36,37] and energy saving operation of the device. In fact, the tested device in this work has been selected from many other candidate devices which also have shown gradual switching and self-compliance behavior, considering this appropriate, achievable current range. Another example with higher current range and even higher number of states is explained in the Supporting Information.

For ISPP/ECC, several parameters should be appropriately selected from the preliminary data. ISPP was acquired by adopting a pulse generator while ECC was conducted by a semiconductor parameter analyzer (SPA). They include the state current gap (SCG), which is the difference between the minimum and maximum current values of the neighboring states; the state current width (SCW), which is the allowed difference between the minimum and maximum current values within a state; the incremental-step voltage and duration, which were fixed at 5 mV and 100 ns, respectively, from several preliminary tests; and finally, the program start voltage for ISPP, which must also be determined experimentally using a preliminary test. Before each programming operation, the device was always erased (switched to HRS) using a 100 ns long +2.5 V pulse (see Section SIII, Supporting Information, for the reset operation parameters). For QLC, the achievable current range (2–11 μA) was divided into 15 LRSs, and individual current range (for one state) was 600 nA which is the summation of SCG and SCW (SCG + SCW = 600 nA). In this work, the SCG ratio (SCG/(SCG + SCW)) was the main experimental parameter that was used to determine the state overlap probability. A larger value of SCG/(SCG + SCW) will help achieve more reliable states, but it simultaneously increases the malfunction rate of ECC. In Figure 2, the ISPP/ECC test results when the SCG/(SCG + SCW) was set to be 33.3%, 50.0%, 66.6%, and 83.3%, respectively, are shown from the top to the bottom panels. Here, the erased state current was commonly less than 100 nA, which was not achieved by ISPP/ECC, but by only single-reset pulse application. For each programmed state, 100 programming was repeated for statistical accuracy, and one ISPP/ECC took a typical pulse number of ≈20 (10 pulses each for ISPP and ECC). Thus, the total number of pulse application/reading for one SCG/(SCG + SCW) condition in Figure 2 was $\approx 3 \times 10^4$ (20 pulses and 100 cycles, and a total of 15 levels). As can be seen in the figure, all the desired states can be well achieved, which is understandable from the adopted switching protocol of ISPP/ECC. Nevertheless, the σ value for each case must be different, which must decrease for a smaller SCG/(SCG + SCW). A more detailed analysis of this important problem is shown in **Figure 3**.

Figure 3a shows the distribution plots of the current values of each state for a given SCG/(SCG + SCW), which is another presentation of the data shown in Figure 2. As can be readily anticipated, the current distribution of each state showed a typical Gaussian shape, and as such, the standard error estimation given by Equation (1) above can be applied. The averaged σ values which were calculated from the corresponding individual σ values are plotted in Figure 3b as a function of SCG/(SCG + SCW). Both figures clearly show that 6σ can be guaranteed down to the SCG/(SCG + SCW) value of 66.6%. When the SCG/(SCG + SCW) value decreased to 50.0%, the error rate increased to ≈0.003%, which was too high to be corrected even with redundancy cells. In fact, more states can be programmed if the allowable current range is increased. As shown in Figure S4 of Section SIV in the Supporting Information, 100 × 100 μm^2 area of Au/HfO_2/TiN capacitor-like ReRAM device which has no interfacial Al_2O_3 layer showed 100 ~ 500 μA of allowable current range. From several preliminary tests, it was confirmed that measurement condition of SCW 5 μA and SCG 15 μA exhibited 21 states (20 LRSs and 1 HRS) with 6.5σ of state overlap probability. Although the allowable current range of Au/HfO_2/TiN

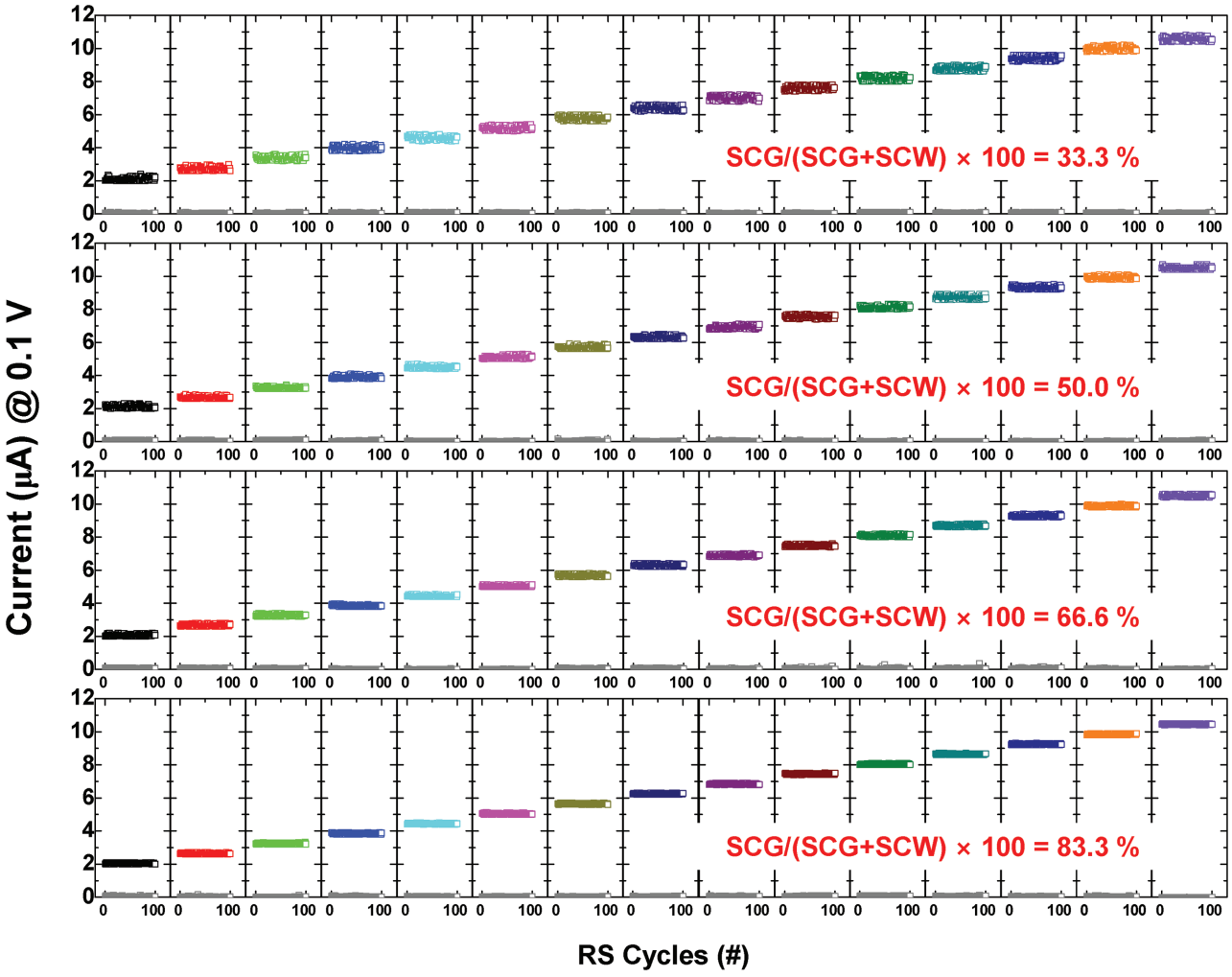

Figure 2. Four-bit (15 LRSs and 1 HRS) performance of the RS device as a function of various SCG/(SCG + SCW) ratios. The resistance of every state was switched by 100-RS cycle. After the successive progress from state 1 to state 15 in one ReRAM cell, the state 1 was confirmed again for the availability of the ReRAM device.

structured device is larger than that of CBA-type RS device, the abruptness of set-switching behavior is also ≈20 times larger (see Figures S4c and S3a, Supporting Information). Such problem hindered the five-bits-per-cell operation, which requires 32 states when a smaller SCG of 7.5 μA was adopted (only 4.5σ of state overlap probability could be achieved). More detailed explanation on this larger area device was provided in Section SIV in the Supporting Information.

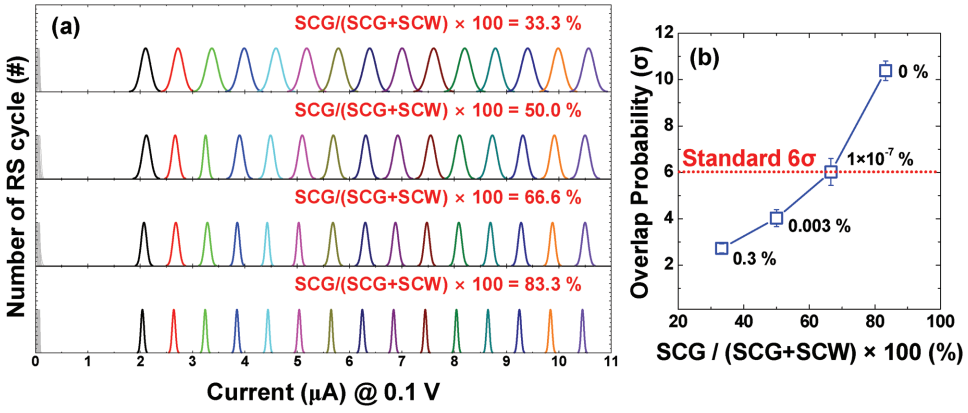

Figure 3. a) Plot of state overlap probability as a function of SCG/(SCG + SCW). It was assumed that the current distribution of the RS device obeys the normal Gaussian function. b) As the value of SCG/(SCG + SCW) increased, the state overlap probability decreased (increase of σ).

A similar problem had occurred for the CBA type device when the 32 states were attempted with a condition of SCG + SCW = 290 nA. Only ≈4.9σ of state overlap probability could be confirmed.

The retention and endurance characteristic of the QLC were also confirmed. As shown in Figure S5a,b in the Supporting Information, the 15 resistance states showed stable retention characteristic with 22σ of overlap probability at 66.6% of SCG/(SCG + SCW) condition. This means the CBA-type RS device in this study is free from the signal-to-noise disturbance issue. The higher value of 22σ (≈6σ in 66.6% of SCG/(SCG + SCW) condition in Figures 2 and 3) was originated from the significantly decreased standard deviation of resistance values in retention measurement. The CBA-type RS device showed up to 10^4 endurance cycles (see Figure S5c, Supporting Information) with almost identical pulse amplitude condition with the highest current level of QLC, which corresponds to the most severe measurement condition. This implies that the CBA-type RS device of this study can endure the repetitive RS cycles of QLC operation reliably. It should be noted that the required endurance cycle of current v-NAND is also ≈10^4 cycles due to the adoption of wear-leveling technique. Finally, the temperature effect on such ISPP/ECC performance was tested. For this test, a sufficiently large SCG of 4 μA was selected, and three states were programmed at 25, 55, and 85 °C, respectively. As shown in **Figure 4**a,b, the data in each state maintained the normal Gaussian distribution, with no notable degradation with increasing temperature. Due to the ISPP/ECC mechanism, identical target current values can be achieved at different temperatures (Figure 4a), but the required pulse amplitude for achieving the target program current increases with increasing temperature (Figure 4b). The variations in the average value of the applied pulse amplitudes were plotted as a function of the temperature for each state, as shown in Figure 4c. The best linear fittings showed a 1.5 mV °C^{-1} slope, which the control circuitry in the memory can easily take care of.

In conclusion, the QLC operation of a CBA-type Au/Al_2O_3/HfO_2/TiN ReRAM device is demonstrated using the industry-standard ISPP/ECC method, which has not been accomplished even in highly matured NAND flash devices. The critical factors that permitted such supreme performance as an emerging NVM were self-compliance, gradual set-switching performance, and appropriate read current range for high speed and low power operation. If another device shows a gradual reset-switching with the abrupt set-switching property, the memory can be operated with one programmed state and multiple erased states. Through the variation of SCG/(SCG + SCW) values within total achievable reading current range (2–11 μA), the overlap probability could be controlled, and 6σ was achieved in the case of 66.6% of SCG/(SCG + SCW). Moreover, 21-state of multiple-level operation with 6σ reliability was also confirmed in larger allowable current range (100–500 μA). This work reports a critical step forward in the ReRAM field for its future adoption for data storage that can show higher competitiveness than the industry-standard NAND flash.

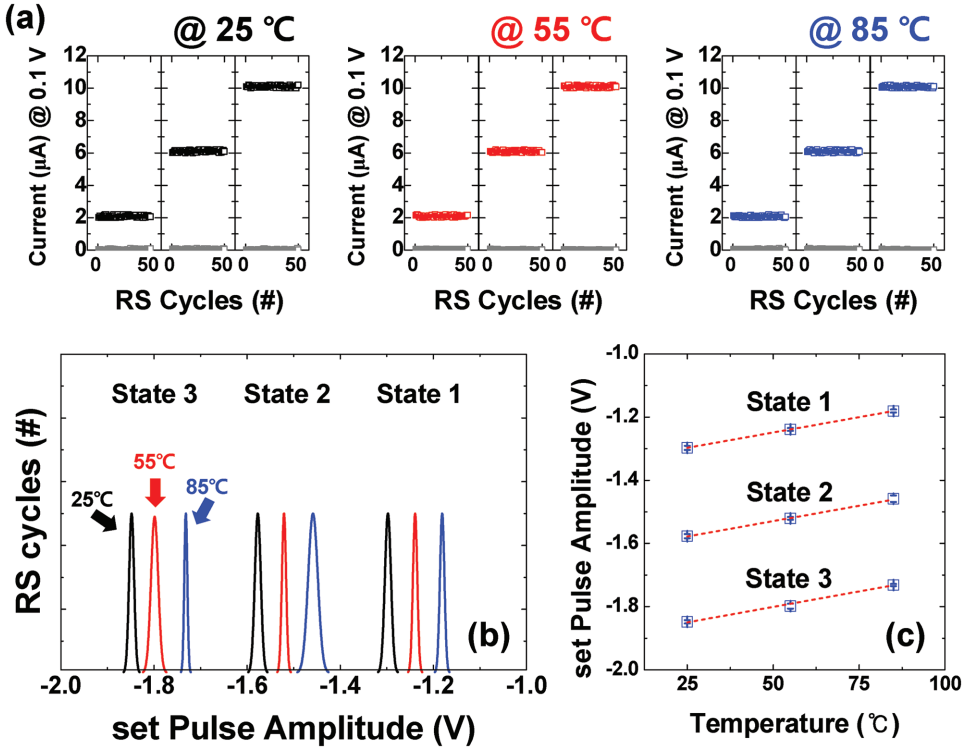

Figure 4. a) Temperature-dependent two-bit (3 LRSs and 1 HRS) operation at 25, 55, and 85 °C, respectively. b,c) Extracted temperature dependency of the voltage distribution according to each resistance level in MLC operation. As the measuring temperature increased, a higher operation voltage was required. Although a temperature-dependent voltage distribution was observed, the automatic voltage compensation function of the ISPP/ECC algorithm was demonstrated.

Experimental Section

A 100 nm thick TiN layer was sputtered on SiO_2/Si substrate at room temperature and patterned to a shape of CBA-type BE. The sputtering condition for the TiN was 1 Torr and 80 W plasma power. The blanket-type TiN was patterned to CBA-type BE by photolithography and wet-etching process with aqueous solution of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and deionized water (H_2O) 1:1:5 at 70 °C. The residual photoresist on TiN after the wet-etching process was sufficiently removed by acetone. Then blanket-type 6 nm thick HfO_2 and 2 nm thick Al_2O_3 thin film layer were deposited by ALD process at 250 and 150 °C, respectively. The tetrakis-ethylmethylamido hafnium, trimethylaluminum precursor, and H_2O were utilized as a source of Hf, Al, and O, respectively. Then a 150 nm thick Au layer was deposited as CBA-type TE through the thermal-evaporation method at a 10^{-6} Torr pressure at room temperature and was patterned with the conventional lift-off process.[23] The final junction area of the CBA-type device was defined with 10×10 μm^2.

The electrical measurement was performed using an HP4145B SPA, an Agilent 81150A arbitrary function generator (AFG), an electromechanical radio frequency (RF) electric-circuit switch box, and a hot chuck with a temperature controller. All the electric measurements were performed with the TE biased and the BE grounded. The resistance (or current) values of the programmed or erased states were read at +0.1 V using SPA. For MLC operation, writing and reading (verifying) operations were performed with two switchable electric circuits composed of an AFG-RS device and an SPA-RS device. These two kinds of electric circuits were alternately accessed through the electromechanical RF electric-circuit switch box. The electric-pulse width was 100 ns. The incremental step voltage of 5 mV was adopted in this work, and the details for determining the optimal incremental step voltage were described in Section SVI in the Supporting Information. The cross-sectional view of the RS device was observed using a high-resolution transmission electron microscope (HR-TEM, LIBRA 200 HT Mc Cs TEM, Carl Zeiss) and chemical structure of the RS device was analyzed using energy dispersive spectroscopy. The samples for HR-TEM observation were prepared using the focused-ion-beam method (Quanta 3D FEG, FEI Company).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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