

Ridge-Valley Nanostructured Samaria-Doped Ceria Interlayer for Thermally Stable Cathode Interface in Low-Temperature Solid Oxide Fuel Cell

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Agglomeration of the metal electrode decreases the performance of low-temperature solid oxide fuel cells (LT-SOFC) during operation at elevated temperatures. Here, we report a Pt electrode/ridge-valley nanostructured samaria-doped ceria (SDC) layer interface with extended lifetime. LT-SOFCs with RF-sputtered SDC interlayers with thicknesses in the range 65–260 nm show a >20 times lower degradation of performance as compared to cells without interlayer when operated at 450 °C (1.8% h⁻¹ vs. 45% h⁻¹). Micromorphological analysis reveals that the coarsening of the Pt electrode is significantly suppressed by the presence of the nanostructured SDC interlayer, possibly due to a stronger bonding between this layer and the Pt grains.

1. Introduction

Solid oxide fuel cells (SOFC), which make use of ceramic oxide electrolytes, are attractive as next-generation energy conversion devices due to their high energy conversion efficiencies, fuel flexibility, and environmental friendliness.^[1–4] SOFCs, however, usually operate at high temperatures (700–1000 °C) to retain adequate power output, which often leads to practical problems such as thermal stress or rapid material degradation. Many studies have been conducted with the aim to lower the operating temperature, in other words, to develop low-temperature (<500 °C) SOFC (LT-SOFC), by fabricating the cell with thin film components.^[5–9] In thin film electrolytes, which are employed in LT-SOFC, the ohmic loss stemming from ionic transport inside the electrolyte is minimized, which means that the fuel cell performance is predominantly determined by the activation loss. In particular, the activation loss at the cathode side, which is also called the oxygen side, is usually dominant

due to the sluggish oxygen reduction reaction ($E_a \sim 1$ eV) at low temperatures.^[10,11] Accordingly, it is important to redesign the cathode to improve the performance of LT-SOFC.

A noble metal electrode, for example, Pt, Ru, or Pd, is indispensable in LT-SOFC because of its extremely high catalytic activity when compared to other catalytic materials. Even though their high cost has often prevented the wide use of noble metals in LT-SOFCs, recent reports have shown that this may be overcome by replacing the bulk metal electrode by an ultra-thin film with nanoscale porosity (usually <100 nm). However, one unresolved issue in the porous novel metal electrode is its poor thermal stability, which causes an irreversible degradation of cell

performance. Indeed, the agglomeration of nano-porous Pt at the operating temperature of LT-SOFCs causes critical performance degradation.^[12–16] Due to the high free energy of the metal film surface, the film tends to agglomerate to lower its interface energy, which decreases the density of the effective triple phase boundary (TPB), where gas, electrolyte and electrode meet and where the ion incorporation reaction actually takes place.

One interesting way to enhance the thermal stability of noble metal electrodes for low-temperature SOFCs is by the oxide overcoating method. Previous studies observed that a zirconia (ZrO₂), ceria (CeO₂), or tin oxide (SnO₂) capping layer formed using thin film deposition techniques, for example, sputtering, atomic layer deposition (ALD), on nano-porous metal electrodes can protect the nano-porous Pt cathode morphology from thermal agglomeration.^[17–19] Su et al. showed that an ALD ZrO₂ over-layer (1 nm) on a Pt electrode improved the lifetime of the electrode by nearly 70%. Cha et al. demonstrated the application of ultra-thin (1 nm) ALD yttria-stabilized zirconia (YSZ) to enhance the performance at extended time of operation (~3 h) by a factor of 2. While the stabilization effect of the oxide over layer has been widely studied recently, there are only few reports on the underlying oxide substrate. Khan et al. recently demonstrated the effect of a microstructured gadolinia-doped ceria (GDC) interlayer in stabilizing electrodes for SOFC, which, however, only focused on the effect of its microscale thickness (2.5–6 μm) and did not elucidate the surface structure effect.^[20]

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In this paper, we demonstrate the effect of a nanocrystalline samaria-doped ceria (nanoSDC)-porous Pt interface on the thermal stability of the Pt electrode. We have systematically varied grain sizes of the ridge-valley shaped SDC surface, from 38 to 90 nm, by controlling the thickness of the SDC layer. The thermal stability of the porous Pt electrodes deposited on the nanoSDC surface was significantly improved (~ 20 times) as demonstrated by chronoamperometry. We further demonstrate that this improved stability is predominantly determined by structural effects, rather than by material aspects. SEM and TEM analysis show that the improved stability of operation at higher temperatures is due to the decreased coarsening of the Pt electrode on the nanoscale ridge-valley shaped SDC surface. A mechanism is proposed to explain this stabilization based both on the energetics of the metal nanoparticles dispersed on a ridge-valley type nanostructured surface, and percolation theory.

2. Experimental

Single crystalline yttria-stabilized zirconia (YSZ) substrates (1×1 cm, $200 \mu\text{m}$ thick, 8 mol.% doping, MTI Corporation, USA) were used as electrolyte pellets in the fabrication of the cells. The samaria-doped ceria (SDC) film was deposited by radio frequency (RF) reactive sputtering at 200 W RF power and 10 mTorr pressure under flowing Ar + O₂ gas mixture in the ratio 4:1. The deposition time was varied to be 35, 70, and 140 min (deposition rate $\sim 1.85 \text{ nm min}^{-1}$). The thicknesses of the SDC layers as determined by field-emission scanning electron microscope (FE-SEM; SU8010, Hitachi Technologies Corporation) were 65 ± 5 , 130 ± 9 , and 260 ± 16 nm. For electrochemical analysis, 80 nm-thick porous Pt electrodes were deposited on both sides of the substrate using direct current (DC) sputtering (SRN-110, Sorona) with 400 W DC power under 45 mTorr of pure Ar (99.999% purity). The Pt cathode was patterned with a shadow mask (pad size: $2 \times 2 \text{ mm}^2$).

The doping level of the SDC pellet and the sputtered SDC film was measured to be 15 mol.% (Ce 29.2%, Sm 10.5%, O 59.9%, C 0.5%) by X-ray photoelectron spectroscopy (XPS) using an Al K α source, a spot size of 400 nm^2 , a step size of 1 eV step^{-1} , and in the binding energy range 0–1150 eV (XPS data shown in Figure S1). The crystallinity of the SDC thin film was analyzed by X-ray diffraction (XRD; Bruker DE/D8 advance, Bruker). The surface morphologies of the SDC thin films and the Pt electrodes (before and after operation) were investigated by FE-SEM and atomic force microscopy (AFM; SPM-1000, AIST-NT). Field emission transmission electron microscopy with an acceleration voltage of 200 kV (FE-TEM; JEOL LTD. JEM-2100F(HR)) was used to study the cross-sectional morphology; samples were prepared by Ar ion-milling.

The performance of the fuel cell was measured using a customized micro-probing test station at 450°C with a flow of 20 sccm of dry H₂ at the anode (Figure S2). The anode side of the fuel cell was sealed to a customized stainless steel hydrogen flow chamber with a gold ring. The cathode side was exposed to ambient air and contacted with a $550 \mu\text{m}$ -in-diameter gold probe tip for current collection using a micromanipulator. Current-voltage measurement, electrochemical impedance spectroscopy (EIS) and chronoamperometry were performed

with a potentiostat (EC-LAB, Bio-Logics). Current-voltage measurement was conducted by using linear sweep voltammetry method starting from open circuit voltage (OCV) with a step size of 10 mV and a scan rate of 20 mV s^{-1} . EIS spectra were obtained at the cell voltage of 0.7 and 0.5 V with the sinusoidal AC voltage (amplitude of 50 mV) within a frequency range of 1 MHz to 1 Hz at 450°C . For chronoamperometry tests, the cells were operated at the cell voltage of 0.5 V at 450°C for 15 h, and the current output was recorded. The cell fabricated on a SDC substrate (1×1 cm, $200 \mu\text{m}$ thick, 15 mol.% doping, Kurt J. Lesker, USA) with 80 nm-thick porous Pt electrodes was additionally prepared and tested for chronoamperometry.

3. Results

Figure 1 shows the top-view and cross-sectional view SEM images of SDC films with thicknesses of 65, 130, and 260 nm on single crystalline YSZ substrates. The top-view images (Figure 1a–c) show that as the thickness of the SDC film increases, the grain structure is more clearly visible and the grain size gradually increases, which indicates a better crystallinity; this tendency is also observed in the XRD spectra (Figure S3). The cross-sectional SEM images (Figure 1d–f) illustrate the growth of columnar grains, which is a generally observed trend in sputtered films.^[21,22] The surface also shows clear triangular ridge-valley morphology due to the high plasma power (200 W) used in the sputtering process. At greater RF power, a greater number of energetic particles ejected from the target arrive at the

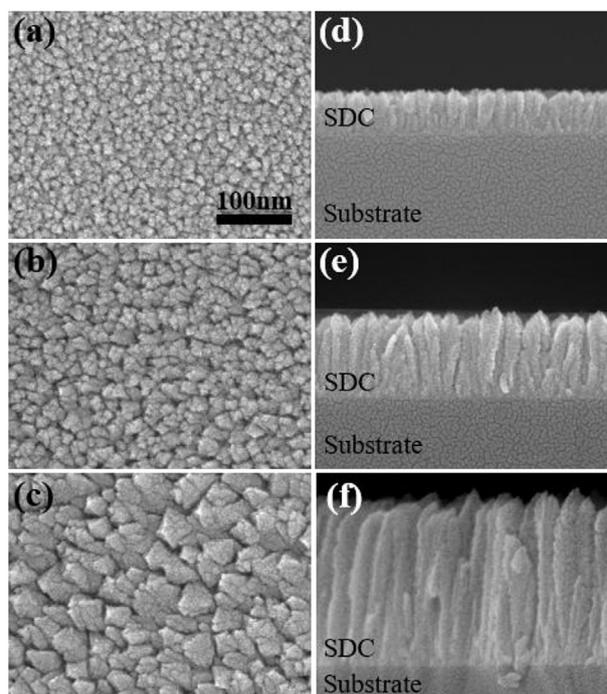


Figure 1. FESEM images of SDC interlayers with varying grain sizes: top view of (a) 65 nm, (b) 130 nm, and (c) 260 nm samples and images of cross-sections of the same (d) 65 nm (e) 130 nm, and (f) 260 nm samples. All the images have the same scale.

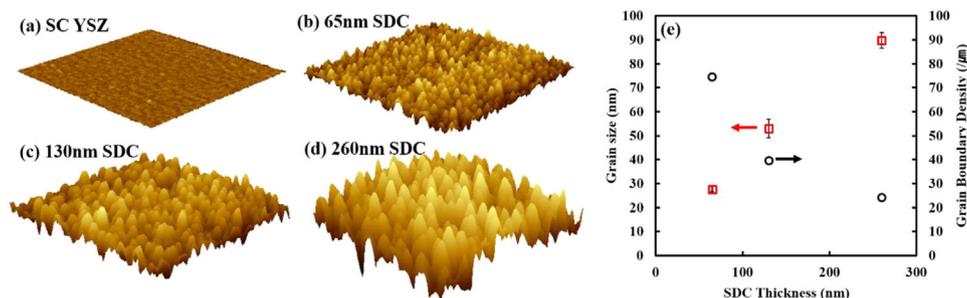


Figure 2. AFM images ($1 \times 1 \mu\text{m}^2$, Z-scales are identical) of the sample surfaces: (a) single crystalline YSZ and (b) 65 nm, (c) 130 nm, and (d) 260 nm thick SDC interlayers. (e) The dependence of grain size and grain boundary density on SDC layer thicknesses as estimated from AFM images. The grain boundary density calculation is based on the brick-layer model.

sample, resulting in better crystallization as well as a rougher surface.^[23]

Figure 2a–d show, respectively, the AFM images of single crystalline YSZ surfaces (reference), 65, 130, and 260 nm thick SDC film surfaces. Figure 2e summarizes the dependence of the grain size and the grain boundary density on SDC film thicknesses as estimated from AFM images. RMS surface roughness values for the samples are measured to be 1.4, 9.5, 17.8, and 31.3 nm for single crystalline YSZ surfaces corresponding, respectively, to the film thicknesses of 65, 130, and 260 nm. The roughness values tally well with the ridge-valley height differences estimated from SEM images. The variation in surface area due to difference in roughness is marginal: there is a 5, 7, and 15% increase for 65, 130, and 260 nm thick samples, respectively, as compared to a flat surface. Grain sizes also increase as the film gets thicker; 28, 53, and 90 nm were, respectively, the in-diameter grain sizes for 65, 130, and 260 nm film thicknesses. Based on the brick-layer model,^[24] the surface grain boundary densities are calculated to be 74.5, 39.7, and 24.26 μm^{-2} , respectively, for 65, 130, and 260 nm thick films.

Current-voltage-power curves and EIS spectra of the cells with YSZ electrolyte pellets (200 μm thick) are shown in Figure 3a and b. The cells with SDC interlayers show improved maximum power densities when compared to the reference cell (YSZ electrolyte cell without SDC interlayer), that is, a 54, 27, and 13% increase, respectively, for 65, 130, and 260 nm thick SDC interlayered samples, which is due to the enhanced cathode kinetics on the doped CeO_2 surface.^[10] A lower improvement in the sample with a thicker interlayer stems from the larger surface grain size. In general, the incorporation of the oxide ion occurs preferentially at the surface grain boundary as compared to the grain center and therefore, the smaller density of the surface grain boundary in thicker SDC samples results in higher activation resistance; this conclusion is well substantiated by EIS results (Figure 3b). To differentiate the contributions from the ohmic and activation processes, we varied the cell voltage, that is, OCV and 0.7 V, where EIS was performed (Figure S4). The high frequency loop in the frequency range of $\sim 10^4$ Hz and higher, whose size is independent of cell voltage, is thought to be associated with the ohmic process. The size of the low frequency loop in the frequency range of $\sim 10^3$ Hz and lower, is dependent on the cell voltage and is known to be associated with the

activation process.^[10] Since the cathodic process is significantly slower than the anodic process in a symmetrically structured (Pt(cathode)/YSZ/Pt(anode)) H_2 - O_2 cell in the low temperature regime ($< 500^\circ\text{C}$),^[10] we can assume that the activation resistance observed in the EIS spectra is dominated by the cathodic activation process. Ohmic resistances tend to increase with increase in SDC thickness due to the longer ionic path. Activation resistances of nanoSDC interlayered samples are lower than that of the reference (YSZ only) sample; however, the

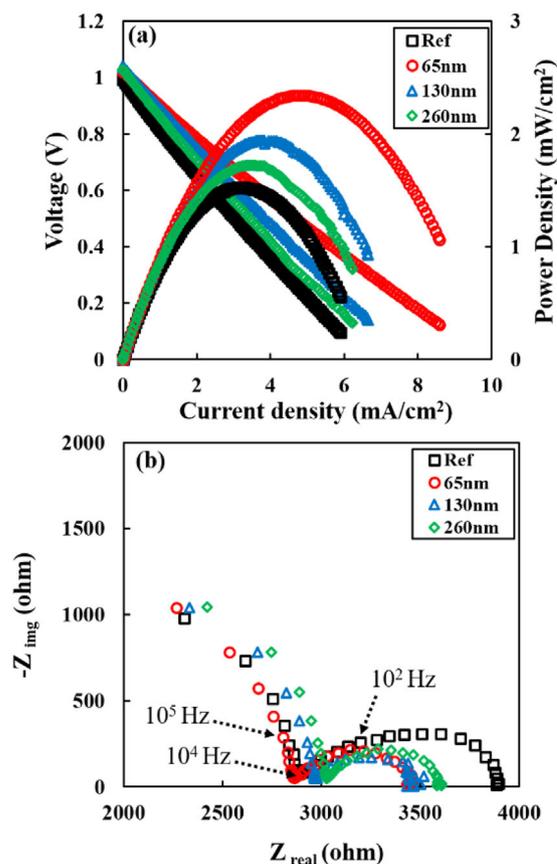


Figure 3. (a) Current density versus voltage, and current density versus power density curves and (b) EIS spectra of the samples at 0.7 V at 450°C.

activation resistance increases with nanoSDC thickness due to the lower surface grain boundary density (578 ohms (65 nm), 585 ohms (130 nm), and 590 ohms (260 nm)). The ionic conductivity of the single crystal YSZ electrolyte, calculated based on measured ohmic resistance values and the geometry of the electrolyte and the electrode, is $1.6 \times 10^{-4} \text{ S cm}^{-1}$, which is similar to values reported in the literature ($1.5\text{--}3 \times 10^{-4} \text{ S cm}^{-1}$ for 8 mol.% single crystal YSZ) at 450°C .^[25,26]

Figure 4 shows the chronoamperometry results of the five cells with different electrolytes, namely, YSZ pellet, SDC pellet, and nanoSDC interlayers on SDC pellets with thickness of 65, 130, and 260 nm. The performances of the cells with YSZ and SDC pellets rapidly decrease: $33\% \text{ h}^{-1}$ (YSZ ref) and $45\% \text{ h}^{-1}$ (SDC ref) for 2 h, respectively. However, the cells with nano SDC interlayer show significantly lower performance degradation rates in the range $1.7\text{--}2.8\% \text{ h}^{-1}$ for the first 5 h. It is notable that for the first 15 h, the degradation rate decreases as the thickness is increased, that is, the nanoSDC surface with larger grains becomes rougher: $6.0\% \text{ h}^{-1}$ (65 nm), $3.0\% \text{ h}^{-1}$ (130 nm), and $1.8\% \text{ h}^{-1}$ (260 nm).

Figure 5 shows the top view FE-SEM images of the porous Pt electrodes before and after operation in samples with and without the nanoSDC interlayer. The top surfaces of the Pt electrode show coalescence in all the samples, resulting in a significant reduction of nanoscale pores on the top surface (Figure 5e–h). Relatively small grains ($\sim 10 \text{ nm}$ (inset in Figure 5a)) with sharp facets are transformed into larger grains ($20\text{--}30 \text{ nm}$ (inset in Figure 5e)) showing a spherical morphology after operation. SEM results confirm that the differences in performance following extended operation is not dominated by the Pt top surface morphology, but may be related more to the interface between the bottom surface of Pt and the nanoSDC surface.

Cross-sectional TEM images reveal more details on the morphological changes taking place in porous Pt electrodes upon annealing. The as-deposited Pt grains show an average width of $\sim 15 \text{ nm}$ (Figure S5) and the Pt grains on single-crystal YSZ substrate coalesce with each other after operation for 20 h at

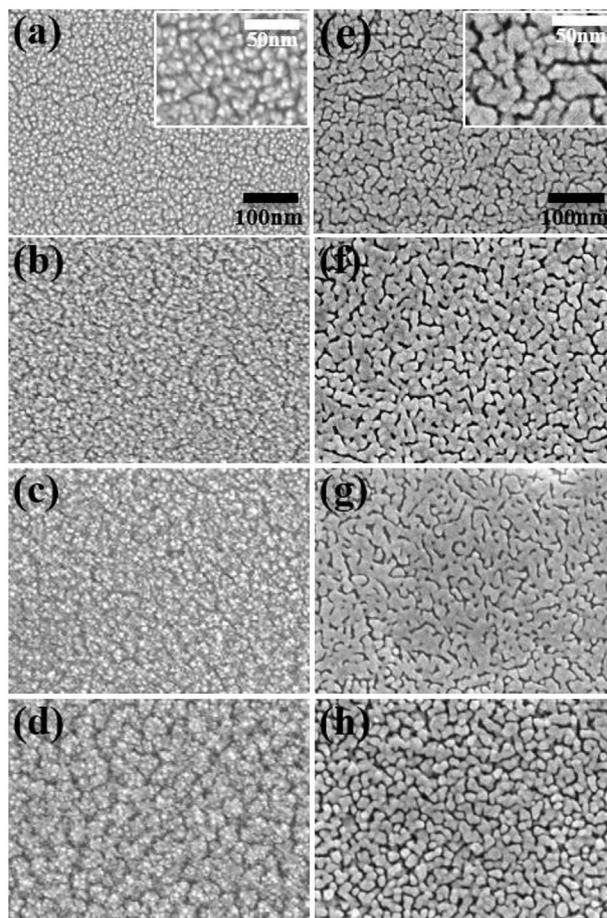


Figure 5. FE-SEM top-view images of the electrodes before and after operation (450°C , 20 h); the surfaces of porous Pt electrodes on 0 nm (on bare YSZ surface) ((a) before and (e) after), 65 nm ((b) before and (f) after), 130 nm ((c) before and (g) after), and 260 nm ((d) before and (h) after) SDC layer thicknesses.

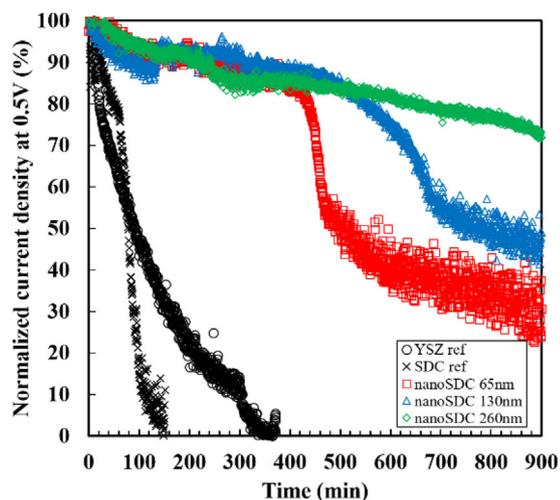


Figure 4. Chronoamperometry curves of the samples at 0.7 V at 450°C for 15 h. Current density values were normalized with respect to the initial values for better comparison.

450°C , causing a significant increase in the average grain width to $\sim 71 \text{ nm}$ (Figure 6a). In the nanoSDC sample however, the bottom part of columnar Pt grains appears to be much more intact than the top surface of the Pt grains after operation (Figure 6b), and shows the presence of nanopores (white dotted arrows in the inset image).^[27,35] By virtue of a hindered coarsening at the Pt-nanoSDC interface, nanoscale pores survive even after prolonged operation at elevated temperatures (inset image of Figure 6b), which helps to maintain the TPB density, and consequently, the electrochemical performance.

4. Discussion

The observed performance degradation of the cells in our experiments is mainly due to the coarsening of porous Pt electrodes. Coarsening, or sintering of metal particles on a certain substrate is determined by a combination of several effects which mainly include 1) the nature of the material (i.e., substrate material) and 2) the structure (i.e., substrate surface structure).^[28–30] The material effect is relevant to the bonding

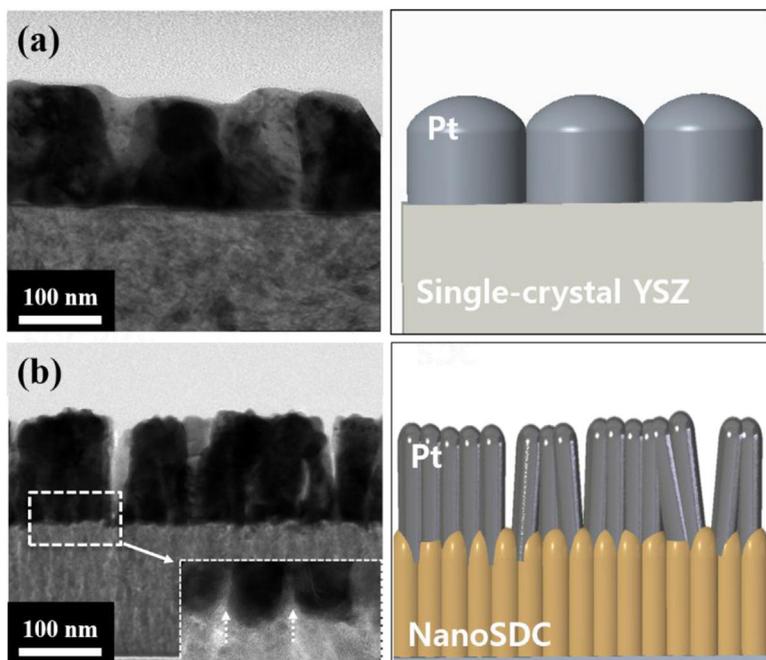


Figure 6. Cross-sectional TEM images and the corresponding schematics of (a) the reference sample (on single crystal YSZ substrate) and (b) 130 nm nanoSDC sample after operation for 20 h at 450 °C. Inset in (b) shows a magnified view of the Pt-nanoSDC interface with white arrows indicating nanoscale pores.

energy between the substrate and overlaid particle. For example, Nagai et al. reported that the bonding between Pt and CeO₂ is stronger than that between Pt and ZrO₂.^[31] Nevertheless, the similar behavior in chronoamperometry experiments observed for the cells on the YSZ pellet and the SDC pellet (Figure 4) show that the material effect does not play a major role in our experiment, but instead, it is the structure effect that mainly determines the coarsening behavior.

It is well known that the structure effect is relevant to the chemical potential of a particle. The chemical potential of a metal nanoparticle on ridge-valley nanostructured surface can be described by the following equation^[32]:

$$\mu(x) = \mu_0 + 2\gamma\Omega/R(x)$$

where $\mu(x)$ and μ_0 are the chemical potentials of the particles at a position x on the nanostructured surface and on a flat surface, respectively, γ is the surface energy of the metal particle, Ω is the atomic volume of the particle, and $R(x)$ is the local radius of the particle at a position x on the nanostructured surface (Figure 7a). This relation implies that a metal particle will tend to move from convex (ridges) to concave (valleys) regions to increase its radius of curvature ($R_1 < R_2$ in Figure 7a) and thus tend to reduce its chemical potential during annealing, which has also been reported by other researchers.^[32–34] Durability improvement on nanoSDC surface, therefore, may also be due to the stabilization of Pt grains by the larger density of the concave regions, that is, $\mu_c < \mu_f$ in Figure 7a; this tendency is also clearly demonstrated in the TEM images (Figure 6).

One more notable characteristic of the chronoamperometry curves of nanoSDC samples is the sudden drop in performance. The chronoamperometry spectra of the nanoSDC cell show 3 different phases as shown in Figure 7b: a gentle performance drop (phase A), a sharp drop (phase B), and a consistently low performance with large fluctuations (phase C). Interestingly, the sharp performance drop (phase B) happens earlier when the SDC grain size is reduced: ~70 min (ref), ~450 min (65 nm), ~630 min (130 nm), and ~900 min (260 nm) after operation (Figures 4 and S6). We speculate that this behavior is relevant to the 2-dimensional percolation of the porous Pt electrode. It is

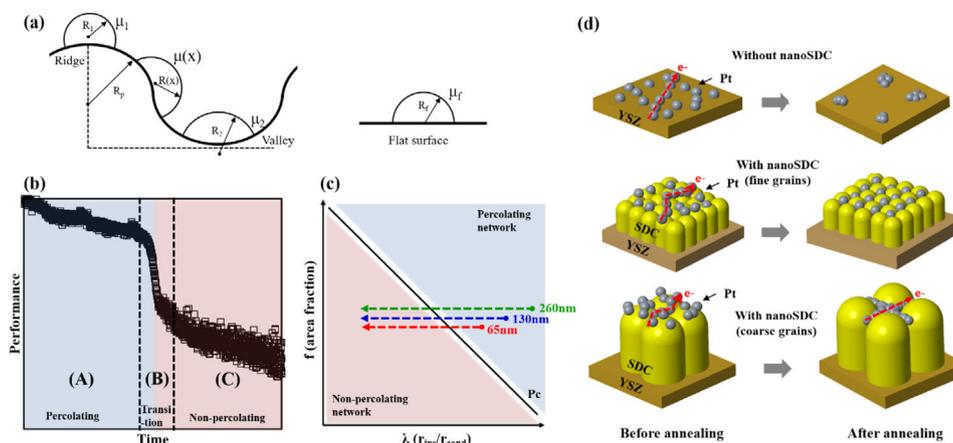


Figure 7. (a) Schematic of particle configuration on curved flat surfaces (all particles shown here have the same volume) redrawn from Ref. [32]. (b) General performance degradation curve based on Figure 4. (c) λ (the size ratio between the insulating particle and the conducting particle) versus f (area fraction) showing the changes taking place during annealing, leading to a transition from percolating to a non-percolating network in the 65, 130, and 260 nm thick nanoSDC samples. (d) Schematics showing the coarsening pattern of Pt grains on various substrates: YSZ pellet (without nanoSDC), nanoSDC with fine grains, and nanoSDC with coarse grains. Red dotted lines represent the percolating paths of electrons.

known that the transition from a percolating to a non-percolating network depends on the ratio (λ) between the size of an insulating particle (\sim surface grain size in our experiment) and that of a conducting particle (\sim Pt grain width, 15 nm). The conducting particles will percolate to a greater extent when λ is large. As the thickness and the grain size of the SDC film increase, λ increases and has the values of, 1.9, 3.5, 6.0, respectively, for 65, 130, and 260 nm thick nanoSDC samples. With continued cell operation, λ decreases as the Pt grains are coarsened to increase in size (dotted lines in Figure 7c), while the area fraction (f) of conducting particles (Pt grains) on the insulating particles (SDC surface grains) is mostly the same. The transition from percolating to non-percolating network therefore, will occur faster in the 65 nm thick nanoSDC sample (red dotted line in Figure 7c) than in the 130 nm (blue dotted line) or 260 nm (green dotted line) thick nanoSDC samples, which is accordance with the results from chronoamperometry (Figure 7c and d). Pt grains on the YSZ pellet (without nanoSDC; $\lambda \sim 0$) may show dramatic performance drop due to the instant transition into a non-percolating network during annealing (Figure 7d). A more detailed investigation on this aspect is underway.

5. Conclusions

In this paper, we have shown that the thermal stabilization of a porous Pt electrode and consequently, that of LT-SOFC can be achieved by incorporating nanostructured SDC interlayers. The relation between the nanostructured SDC surface grain size and the stabilization effect was elucidated based on the mechanism of coarsening of metal particles on ridge-valley nanostructured substrates. The performance degradation of a LT-SOFC cell was also discussed in light of the percolation mechanism. The results described in this paper will pave the way to designing thermally-stable metal-oxide interfaces in various energy conversion devices including LT-SOFCs.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Acknowledgements

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Keywords

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