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## Enhancing thermal-stability of metal electrodes with a sputtered gadolinia-doped ceria over-layer for low-temperature solid oxide fuel cells

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### ABSTRACT

Cathodic activation loss is the dominant loss mechanism in the operation of low-temperature solid oxide fuel cells (LT-SOFCs). The thermal degradation of metallic cathodes decreases the performance of LT-SOFCs, causing practical issues in long-term operation. In this paper, we investigate the effect of the sputtered gadolinia-doped ceria (GDC) over-layer on the thermal stability of platinum (Pt) cathodes. The thermal stability of Pt cathodes with 23 nm-thick GDC over-layers significantly increased compared to that of the Pt-only cathodes after 2hrs' operation at 450 °C. (< 4% vs. 17% performance degradation, respectively).

### 1. Introduction

Solid oxide fuel cells (SOFC) are energy conversion devices which show high energy conversion efficiency, low emission, and fuel flexibility. SOFCs usually operate at a high temperature range of 800–1000 °C, which can facilitate the electrochemical reactions associated with SOFC operation. However, high operating temperature poses practical issues such as thermal degradation [1–4]. Therefore, low-temperature SOFCs (LT-SOFCs, operated at 300–500 °C) have been investigated by many researchers [5–9]. In LT-SOFCs, the losses in fuel cell operation vastly increase, thereby decreasing the electrochemical performance of the cell. Specifically, the loss associated with the electrochemical reaction at the cathode, *i.e.*, cathodic activation loss, significantly increases as the operating temperature drops due to the sluggish oxygen reduction reaction (ORR) [10,11].

The use of platinum (Pt) is, therefore, essential for high performance low-temperature fuel cells because of its superior electrochemical catalytic activity at low temperatures compared with other materials. Even though the high material cost of Pt (~\$ 50/g) may seem to be a practical bottleneck in applying it to catalytic electrodes of SOFCs, previous research has shown that the material cost can be dramatically reduced if the Pt electrodes are fabricated as ultra-thin films (< 100 nm) [12,13]. For instance, An *et al.* demonstrated that a 10 nm thick Pt electrode fabricated by atomic layer deposition (ALD) can be employed for LT-SOFCs, achieving both ultra-low Pt loading (0.02 mg/cm<sup>2</sup>) and high performance comparable to even thicker

sputtered Pt electrodes(80 nm). However, nanoscale thin film Pt electrodes are known to be vulnerable to thermal degradation even at low temperatures, which is primarily due to coarsening by extremely high surface energy(~2 eV/atom) of Pt [12]. For example, the performance of a LT-SOFC with sputtered Pt electrodes dropped by up to 30% after only 3 h of operation at 450 °C [10,12,13]. For reducing the thermal degradation of electrodes, researchers have investigated Pt-M (M = Ni, Co, Mn, F, Vr, Cr, Ir) alloys and Pt-oxide composites. Specifically, the Pt-Ni alloy catalyst significantly enhanced the thermal stability of electrodes, *i.e.*, the Pt-Ni alloy catalyst maintained its morphological properties even at elevated temperatures (> 500 °C), while the Pt catalyst did not [14–16]. The Pt-oxide composite also enhanced both the thermal stability and the performance of the cells [17–20]. For instance, Chang *et al.* showed that ultrathin yttria-stabilized zirconia (YSZ) coatings on Pt electrodes prepared by atomic layer deposition (ALD) helped to maintain morphology during high temperature operations (500 °C) and enhance the reaction area density [20]. Recently, Lee *et al.* also showed that co-sputtering Pt and GDC can minimize the performance loss stemming from thermal degradation of electrodes down to ~7% after 1 h of operation at 500 °C [18].

In this study, we successfully demonstrate the effective enhancement of the thermal durability of the Pt cathode over-layered with sputtered gadolinia-doped ceria (GDC) at 450 °C. When a GDC over-layered Pt cathode structure (23 nm-thick GDC on 80 nm-thick porous Pt) was applied to the cell with YSZ electrolyte, the performance drop of the cell was less than 4% after operation at 450 °C for 2 h, which is a

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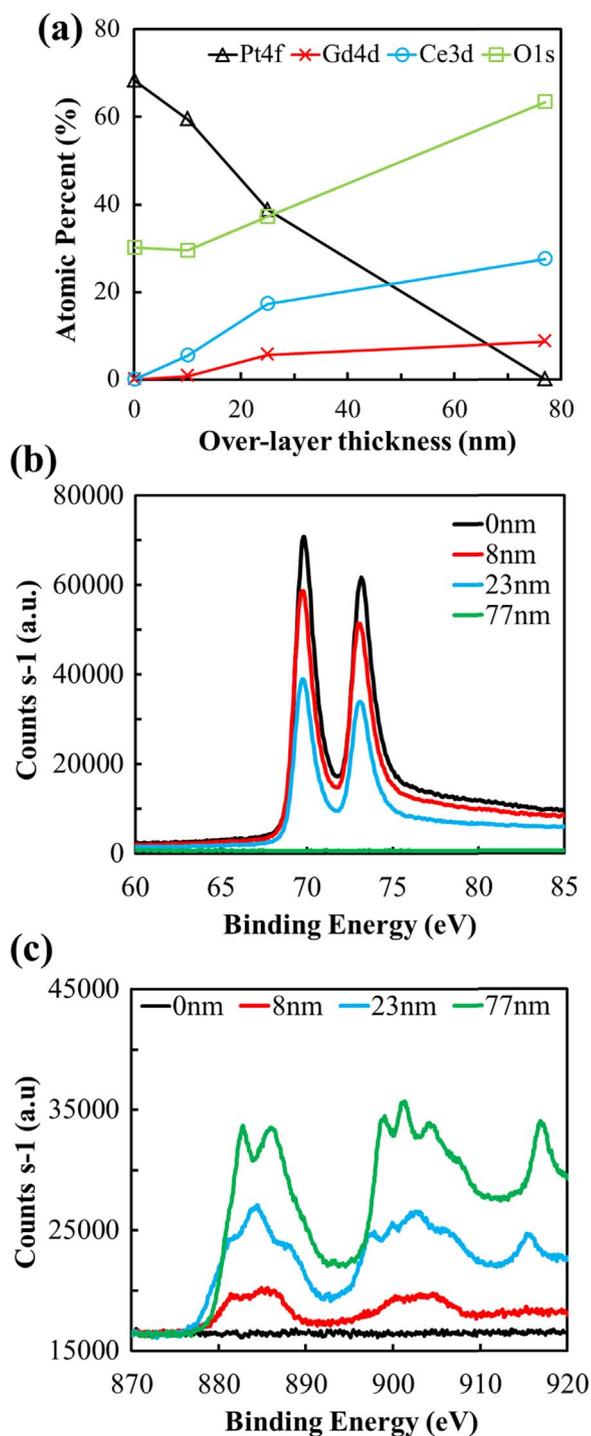
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**Fig. 1.** XPS spectra of GDC over-layers on Pt cathode surfaces with 0–77 nm GDC thicknesses. (a) Relative atomic percentage of Pt, Gd, Ce, and O. High-resolution spectra near (b) Pt<sub>4f</sub> and (c) Ce<sub>3d</sub> peaks.

significant improvement compared the cell with the Pt-only cathode(17%). Morphological and compositional characterization of the GDC/Pt composite electrode reveal that the enhanced performance mainly comes from the suppressed coarsening of Pt electrode surface.

## 2. Experimental

Single crystalline yttria-stabilized zirconia (YSZ) substrates (1×1 cm, 200 μm thick, 8 mol% doping, single-side polished, MTI Corporation, USA) were used as electrolytes for the fabrication of the cell. For electrochemical analysis, 80 nm-thick porous Pt electrodes were deposited on both sides of the substrate using direct current (DC) sputtering (A-Tech System Ltd.) with 100 W DC power under 75 mTorr of pure argon gas (99.999% purity). The Pt on the cathode side was patterned with a shadow mask (1×1 mm). On top of the Pt cathode, gadolinia-doped ceria (GDC) was deposited with radio frequency (RF) sputtering at 60 W RF power and 5 mTorr Ar pressure. The deposition time was controlled to 3 and 30 mins (deposition rate ~2.57 nm/min). The thicknesses of GDC layers determined by ellipsometry were 8, 23 and 77 nm, respectively. The doping level of sputtered GDC was measured to be 11 mol% by X-ray photoelectron spectroscopy (XPS).

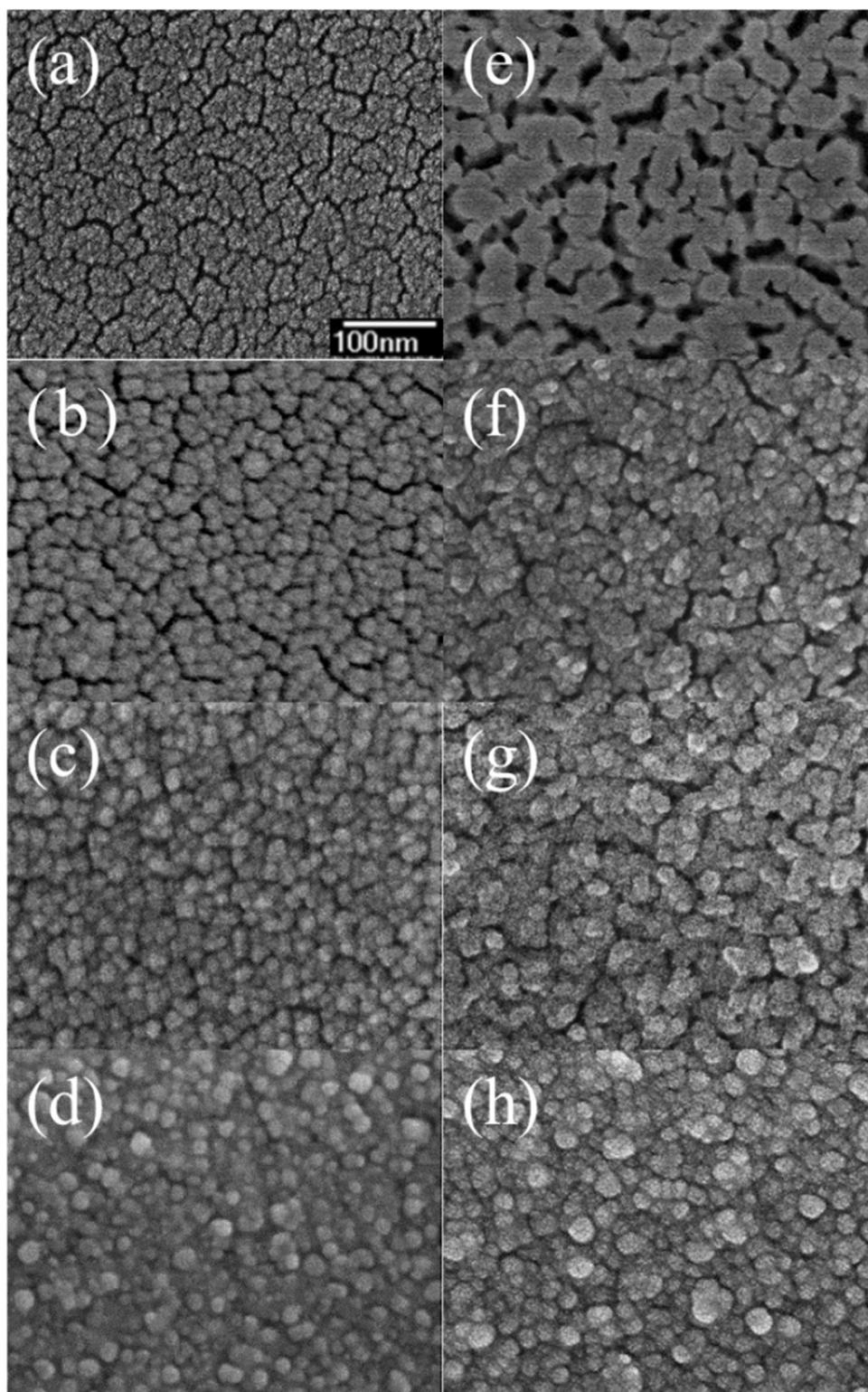
The performance of the fuel cell was measured using a custom micro-probing station at 450 °C with 20 sccm of dry H<sub>2</sub> flowed to the anode side. The cathode was exposed to ambient air. Polarization curves and electrochemical impedance spectroscopy (EIS) spectra were obtained with a potentiostat (Gamry Instruments) at the cell voltage of 0.8 V and 0.6 V at 450 °C.

The surface morphology of the composite electrode was investigated with a field-emission scanning electron microscope (FE-SEM; JEOL LTD. JSM-6700F). Post-processing of images for TPB density calculations was conducted with ImageJ software. 200 kV field emission transmission electron microscopy (FE-TEM; JEOL LTD. JEM-2100F(HR)) was used for imaging and energy dispersive spectroscopy (EDS) analysis. Surface compositional analysis was performed with X-ray photoelectron spectroscopy (XPS; VG ESCALAB 220i) with an Al Kα source, a spot size of 400 nm<sup>2</sup>, a step size of 1 eV/step, and a binding energy range of 0–1000 eV.

## 3. Results and discussion

Fig. 1a-c present the XPS spectra of the prepared samples. Fig. 1a shows the atomic percentages of Pt, Gd, Ce, and O at the sample surfaces. As the GDC layer becomes thicker, the atomic percentage of Pt decreases while those of Ce, Gd, and O increase as expected. It is notable that the composition of Pt is still significant (~40%) even with the 23 nm GDC over-layer surface. Considering that the analyzing depth of the XPS technique is less than 10 nm from the topmost surface, this result confirms that the sputtered GDC layer is still porous due to slow nucleation of sputtered GDC on Pt surface. Such porosity may have accommodated the access of gas molecules to the triple phase boundary (TPB) region, where electrolyte (YSZ), electrode (Pt), and gas (air) meet, and is known to be the preferential site for ion incorporation as was also shown in the previous reports [13,21,22]. Pt is not detected at the surface of the 77 nm GDC over-layer cell at all, which signifies that the GDC layer is now completely covering the Pt surface.

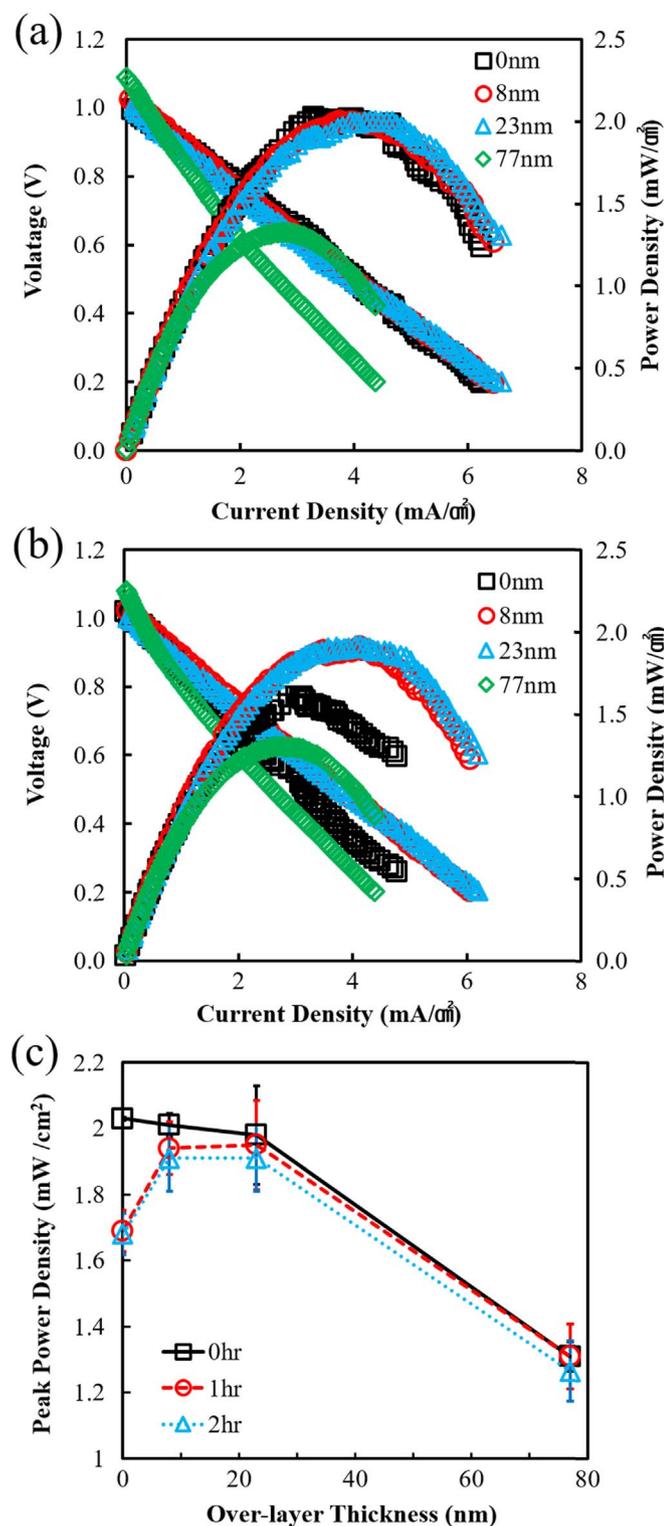
Fig. 2 compares the top-view FE-SEM images of as-deposited cathode surfaces and those after operation at 450 °C for 2 h. As can be seen in Fig. 2a and e, the reference cell without a GDC over-layer (i.e., 0 nm GDC thickness) shows the typical morphological change of a Pt electrode due to coarsening at elevated temperatures [23,24]. The Pt electrode agglomerated which results in a decrease in the density of pores (dark regions in the images). The characteristic width of the pores also increases from < 10 nm (Fig. 2a) to ~20 nm (Fig. 2e) and



**Fig. 2.** Top-view FE-SEM images of as-deposited GDC over-layers on Pt cathode surfaces with thicknesses of (a) 0 nm, (b) 8 nm, (c) 23 nm, and (d) 77 nm. Corresponding FE-SEM images after 2 h of operation for thicknesses of (e) 0 nm, (f) 8 nm, (g) 23 nm, and (h) 77 nm. All images are shown in the same scale.

the TPB density decreases from  $80 \pm 9 \mu\text{m}/\mu\text{m}^2$  to  $24 \pm 3 \mu\text{m}/\mu\text{m}^2$  (approximately 70% decrease) after operation. It is also notable that the fine structure of nanoscale cracks between pores largely disappears.

Such abrupt morphological change of the sputtered Pt electrode without further treatment may be largely due to the coarsening that mainly occurs in two mechanisms: the merging of the individual Pt



**Fig. 3.** Current density-voltage and power density curves at 450 °C: (a) as-deposited and (b) after 2 h of operation. (c) Summary of GDC thickness vs. peak power density after 0, 1, and 2 h of operation.

particles by physical movement and the Ostwald ripening, *i.e.*, the evaporation of energetically unstable surface atoms from relatively small particles and the following adhesion of the atoms to relatively

large particles. Cells with GDC over-layers on Pt electrodes show much less agglomeration compared to the reference cell. The 8 nm and 23 nm GDC over-layer cells show a surface morphology (Fig. 2b and c) comparable to that of the reference cell before operation. Nanopores in the 8 nm and 23 nm GDC over-layer cells seem to retain their original morphology after operation at 450 °C for 2 h (Fig. 2f and g). The surface of the 77 nm GDC over-layer cell is completely covered by GDC grains both before and after operation, and nanopores are not visible (Fig. 2d and h).

Fig. 3 shows the current-voltage and power density curves for the samples as-prepared (Fig. 3a) and after 2 h of operation (Fig. 3b) at 450 °C. The open circuit voltages are measured to be  $1.05 \pm 0.02$  V for all the samples, which are close to the thermodynamic limit at 450 °C (Nernst voltage of 1.1 V). Peak power densities of the cells after 0, 1, and 2 h of operation are summarized in Fig. 3c. Initially, the maximum power densities of the 0, 8, and 23 nm GDC over-layer samples are similar, *i.e.*, less than 5% difference each other. After operation for 2 h, however, the difference in power density change between the untreated (0 nm) sample and the other samples is notable: the peak power density of the 0 nm GDC over-layer cell significantly decreases by 17% while those of the 8, 23, and 77 nm cells decrease only by 5.0%, 3.5%, and 3.4%, respectively. These results prove that the over-layer enhances the thermal stability of the cathode and the overall cell performance at extended operation times. The power density of the 77 nm GDC over-layer cell is dramatically lower than those of the other samples, which is due to the formation of the thick GDC film on the Pt electrode as shown in the FE-SEM images.

To investigate the relative contributions of ohmic and activation losses, electrochemical impedance spectroscopy was performed. To differentiate the contributions from the ohmic and activation processes, we varied the cell voltage, *i.e.*, 0.8 V and 0.6 V, where EIS was performed (Fig. 4). The high frequency loop at the frequency range of  $\sim 10^5$  Hz and higher, whose size is independent of cell voltage, is thought to be associated with the ohmic process. The size of the low frequency loop at the frequency range of  $\sim 10^4$  Hz and lower is dependent on cell voltage and is known to be associated with the activation process [10]. Since cathodic activation is significantly slower than the anodic process in such a symmetrically structured (Pt(cathode)/YSZ/Pt(anode))  $H_2$ - $O_2$  cell at low temperature regime ( $< 500$  °C) due to several orders of magnitude smaller exchange current density [10], we can unarguably assume that the activation resistance in the EIS spectra is dominated by the cathodic activation process.

Fig. 5 shows EIS spectra of the samples after 0, 1, and 2 h of operation, and Fig. 6 shows the summary of the EIS analysis that demonstrates the change in ohmic (Fig. 6a) and activation resistances (Fig. 6b) as a function of the GDC over-layer thickness and the operation duration. Ohmic resistances of the 0, 8, and 23 nm GDC over-layer samples are also similar (11460–11820  $\Omega$ ) and do not change considerably as the cells are operated (Fig. 6a). Ionic conductivity of single-crystal YSZ electrolyte calculated based on the measured ohmic resistance values and the geometry of the electrolyte and the electrode is  $1.7 \times 10^{-4}$  S/cm, which is similar to the reference values ( $1.5$ – $3 \times 10^{-4}$  S/cm for 8 mol% single crystal YSZ) at 450 °C reported elsewhere [1,10]. In the meantime, the activation resistances, which are associated with the high frequency loops, for the 0, 8, and 23 nm GDC over-layer cells are similar each other before operation (black lines in Fig. 6b). However, after 2 h of operation at 450 °C, the 0 nm GDC over-layer cell shows 114% increase in activation resistance while the 23 nm cell shows only 17% increase. This result clearly implies that the suppressed performance degradation in the 23 nm GDC over-layer cell in Fig. 3 is due to the marginal increase in cathodic activation resistance upon prolonged operation. The activation and

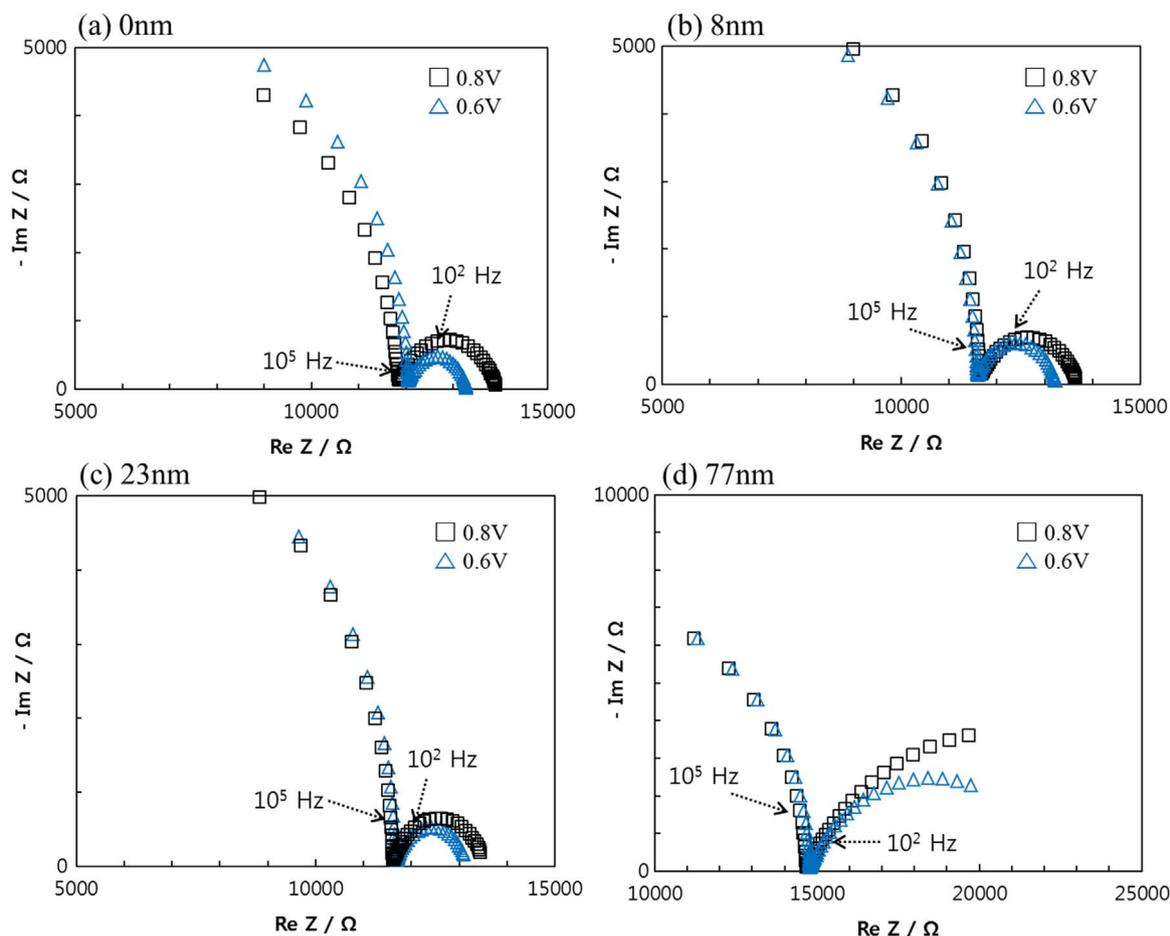


Fig. 4. EIS spectra of the samples at varying cell voltages at 0hr of operation: (a) 0 nm, (b) 8 nm, (c) 23 nm, and (d) 77 nm-thick GDC overlayer samples.

ohmic resistances of the 77 nm GDC over-layer sample are significantly higher than those of the others before and after operation, which seem to stem from impeded reactant gas access to Pt-YSZ interface and current collection by the non-porous GDC film, respectively.

In depth investigations of the morphological and compositional changes of GDC over-layers on Pt cathodes following operation were performed with HRTEM and TEM-EDS. Fig. 7a and e show the TEM images of the 23 nm GDC over-layered cell before and after 2 h of operation, respectively. No clear difference was observed between the two cells in terms of Pt and GDC thicknesses; columnar grains and nanoscale cracks (white arrows in Fig. 7a and e) between grains are observed. Also, the lattice spacing analyses in the inset images of Fig. 7b and f show that the crystal structure is similar to 10 mol% doped GDC ( $a$ : 0.544 nm) and remains intact after operation [25]. One notable thing is the average width change of the columnar Pt grain from  $\sim 10$  nm to  $\sim 15$  nm. This data indicates that the minor morphological changes in the Pt electrode occurred by merger between neighboring Pt grains. It is possible this was not clearly observed in the FE-SEM images (Fig. 1) due to limited resolution. Such slight coarsening in nanoscale granular structure may account for the minimal drop ( $< 4\%$ ) of the performance of the 23 nm GDC over-layered cell after operation. The TEM-EDS mapping results quantitatively describe the compositional change in the 23 nm GDC over-layer cell before (Fig. 7c and d) and after (Fig. 7g and h) operation. The distribution of Pt content is shown to be homogenous throughout the

electrode layer. Ce content is observed primarily at the top of the GDC film with little portion of penetrated contents into Pt layer, *i.e.* the penetration of sputtered GDC film into pores is largely limited. GDC layer have slightly diffused into Pt layer (data not shown here), which, however, does not seem to affect the performance significantly.

The mechanism of the thermal stabilization of metal electrode by sputtered GDC overlayer may be compared to that by ALD overlayer; Previous reports regarding similar oxide over-layers by atomic layer deposition (ALD) process have argued that the conformal nature of ALD over-layer film on the surface of individual metallic electrode grains is essential in maintaining the morphology upon annealing [20,23,26]. ALD oxide overlayer, which is deposited conformally on Pt surface, is known to be slightly coarsened upon annealing, rendering higher density of pores and TPB sites at Pt surface (Fig. 8b). GDC film in our samples, however, mostly stays near the top surface of Pt electrode due to the nature of sputtering method, which is a kind of line-of-sight physical vapor deposition process, as confirmed by TEM and EDS analysis. Interesting point, though, is that the thermal stabilization effect was still significant; the difference in the thermal agglomeration behavior between the electrode top and electrode-electrolyte interface could substantiate such results. The unbounded surface of Pt is known to be more vulnerable to the thermal agglomeration by heat compared to the Pt-YSZ interface that is constraint to migrate due to atomic bonding (Fig. 8a) [23]. Indeed, Yu et al. visually showed that porous Pt's top surface significantly agglomerate at the temperature of 100 °C

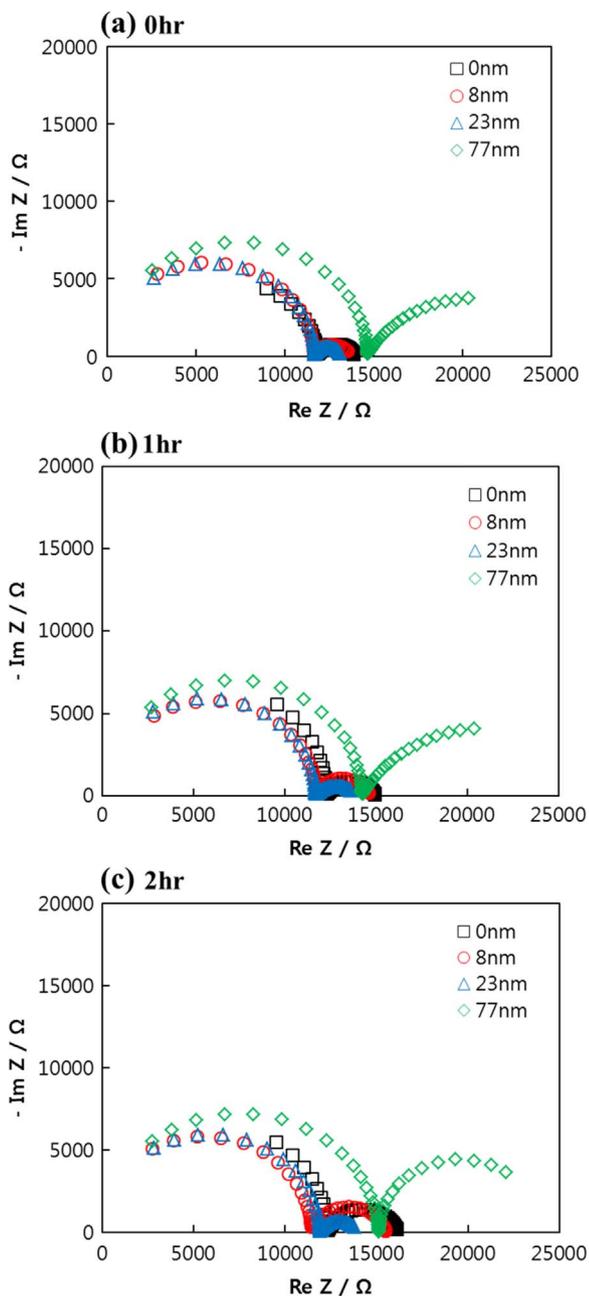


Fig. 5. EIS spectra of the samples after (a) 0 h, (b) 1 h and (c) 2 h of operation.

lower than Pt-YSZ interface, *i.e.*, 400 °C vs. 500 °C [23]. Their results correspond very well to our observation in Fig. 2a and e, where nanoscale cracks disappear and pore size increases upon annealing. The sputtered GDC over-layers on top of Pt electrodes in our samples seem to have posed physical constraints on the agglomeration of the top surface, thereby preserving the surface area and the catalytic activity of the electrodes (Fig. 8c). This result also implies, with such over-layers, one may effectively increase the maximum operating temperature of low-temperature SOFCs without significant thermal

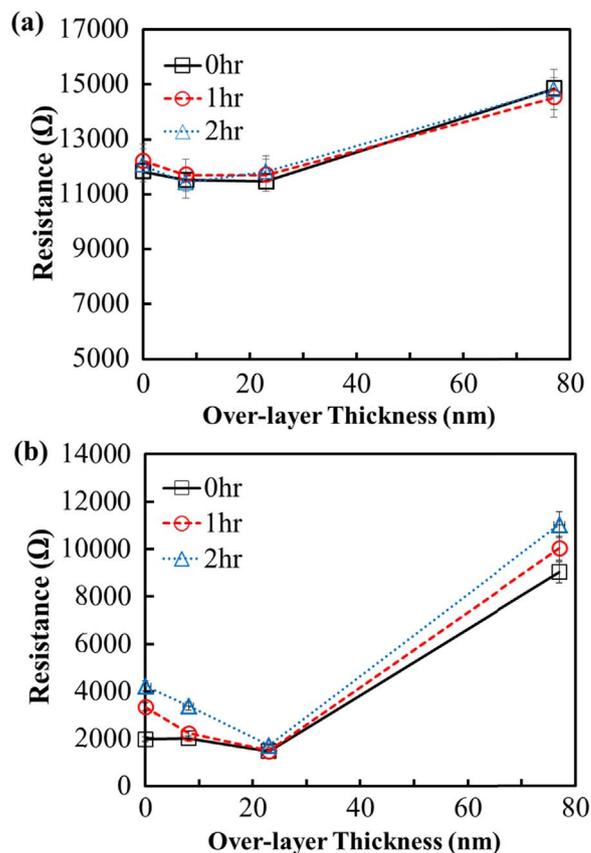


Fig. 6. Resistances obtained from EIS analysis. (a) ohmic and (b) polarization resistances as a function of GDC layer thickness.

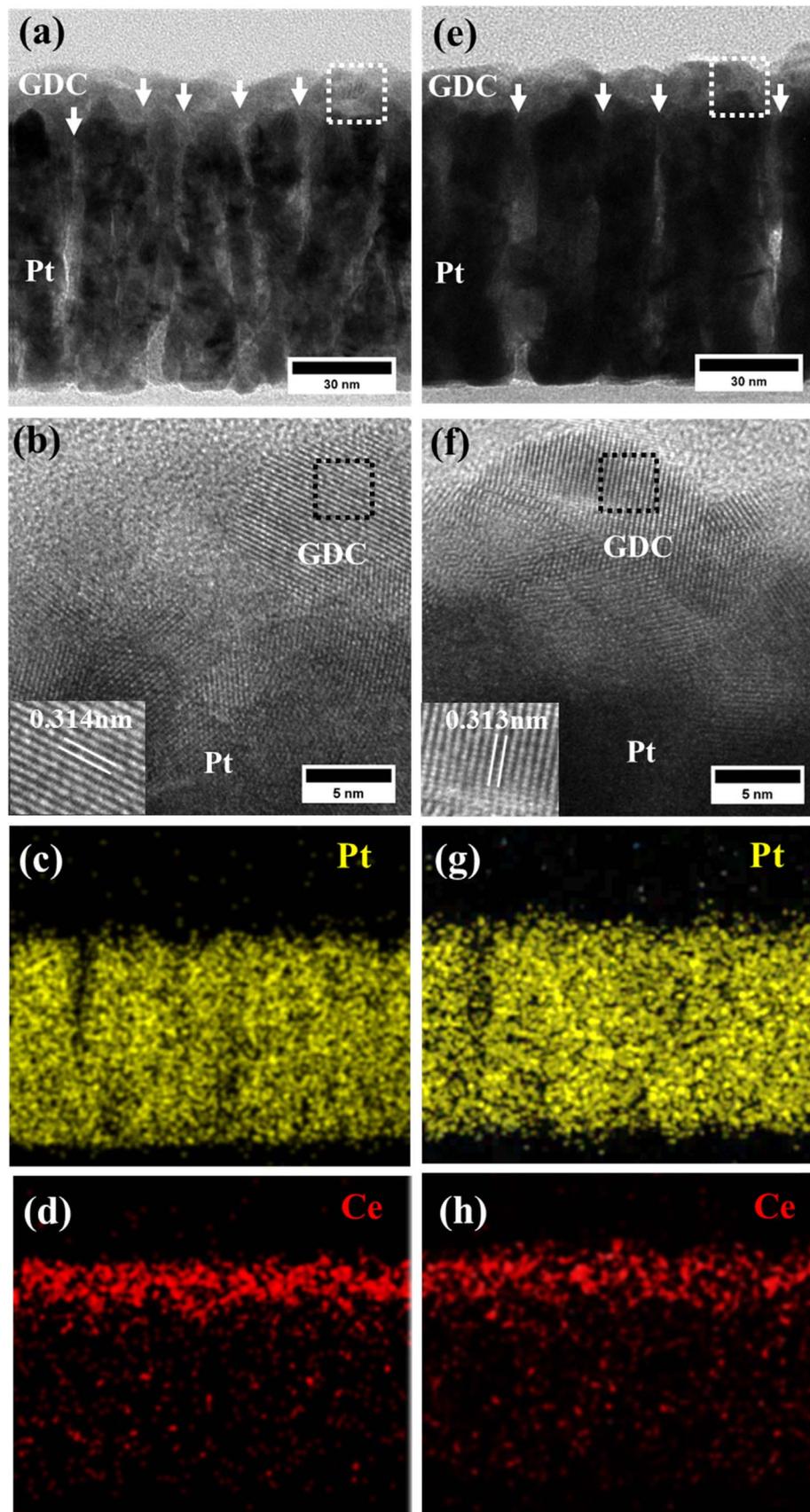
degradation by 100 °C, which will greatly help the wider application of the devices.

#### 4. Conclusion

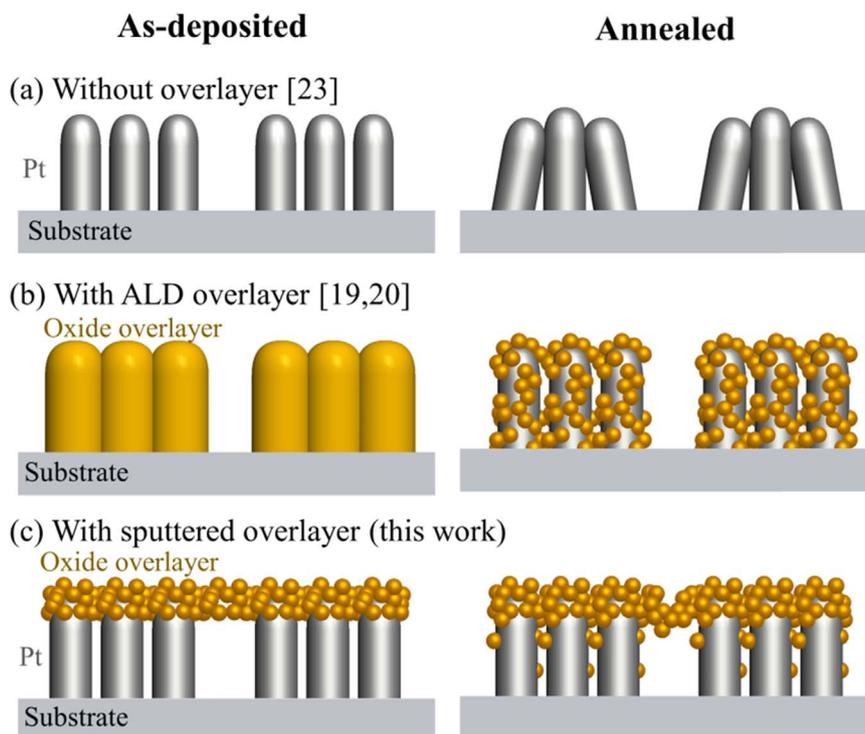
In this report, we have demonstrated the fabrication of a thermally stable GDC over-layered Pt cathode for the possible application to low-temperature SOFCs. Furthermore, we investigated the effect of the GDC over-layer on the electrochemical performance and thermal stability of the Pt cathodes. We have shown that the 23 nm-thick GDC over-layer significantly reduces the performance loss of the cell to < 4% after 2 h of operation at 450 °C. Morphological and compositional analyses further revealed that the suppressed coarsening of Pt at the top surface may account for the enhanced thermal stability of the composite electrodes. The result described here may provide interesting and useful design rules for fabricating electrodes with extended lifetimes which in turn could provide stable operation of LT-SOFCs and other types of energy conversion devices.

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**Fig. 7.** (a, b) TEM images and (c, d) EDS mapping results of the 23 nm GDC over-layer cell before operation: (a) overall image, (b) image near the GDC/Pt interface, (c) Pt elemental mapping, and (d) Ce elemental mapping. (e, f) TEM images and (g, h) EDS mapping results of the 23 nm GDC over-layer cell after operation: (e) overall image, (f) image near the GDC/Pt interface, (g) Pt elemental mapping, and (h) Ce elemental mapping. Lattice spacing shown in the inset images(b, f) corresponds to (111) direction of 10 mol% GDC ( $a$ : 0.544 nm).



**Fig. 8.** Schematics showing merging behaviors of Pt electrodes by differently fabricated overlayers: (a) without overlayer [23], (b) with ALD overlayer [19,20], and (c) with sputtered overlayer (this work).

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