



# Influence of the grain size of samaria-doped ceria cathodic interlayer for enhanced surface oxygen kinetics of low-temperature solid oxide fuel cell

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## Abstract

The catalytic role and grain boundary effect of samaria-doped ceria (SDC) interlayers were investigated. To see the catalytic role, an SDC interlayer was deposited on a single crystalline YSZ (100) substrate by using the pulsed laser deposition (PLD) for an epitaxial film. The grain boundary effects were analyzed with SDC interlayers with various grain sizes on polycrystalline YSZ substrates. As a result, the membrane electrode assembly (MEA) with an epitaxial SDC interlayer exhibited a peak power density that was twice that of a YSZ controlled MEA. More detailed experiments were conducted with MEAs with various grain sizes. In the electrochemical analysis, the MEA with a nano grain SDC interlayer showed an increased maximum power density and lower cathodic impedance. This result suggests that the performance of low temperature solid oxide fuel cells (LT-SOFCs) could be enhanced by applying an SDC interlayer with nano grains for the enhanced oxygen reduction reaction.

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**Keywords:** Samaria-doped ceria; Composite electrolyte; Oxygen activation; Grain boundary; Solid oxide fuel cell

## 1. Introduction

Among renewable energy conversion systems, solid oxide fuel cells (SOFCs) have received a great deal of attention due to their high energy conversion efficiency, intensive power generation, environmentally friendly emissions, and fuel flexibility. However, due to the low ionic conductivity of the commonly-used electrolyte material, yttria-stabilized zirconia (YSZ), the operating temperature had to be high (800–1000 °C) in order to overcome the ohmic loss, which comes from oxide ion transportation through the electrolyte. Unfortunately, this high operating temperature yields many critical obstacles for the widespread application of SOFCs, such as the thermal

degradation of the membranes, difficult system insulation, and narrow material selections. Therefore, lowering the operating temperature of SOFCs below 500 °C is desirable in order to resolve the various thermal issues. However, decreasing the operating temperature to the low-temperature solid oxide fuel cell (LT-SOFC) regime (300–500 °C) significantly lowers the overall fuel cell performance by reducing the ionic conductivity of the ceramic electrolyte as well as the oxygen reduction reaction (ORR) rate, which is related to the charge transfer reaction, mainly at the cathode/electrolyte interface. To alleviate the increased ohmic resistance, many researchers have investigated fabricating and minimizing the electrolyte thickness by developing thin film deposition techniques, including sputtering and atomic layer deposition (ALD).<sup>1–4</sup> However, electrode polarization loss, which mostly comes from the cathode interface due to the sluggish ORRs, is still a critical challenge, and is more dominant than anode polarization for LT-SOFCs.<sup>5–7</sup> Also, it is generally agreed that platinum (Pt) is still the best cathode material for enhancing the oxygen reaction kinetics at this low

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operating temperature regime, since the typically used mixed conducting ceramic electrodes have poor catalytic activity and transport properties for the use of LT-SOFC electrodes.<sup>8–11</sup> Acceptor-doped ceria materials such as gadolinia-doped ceria (GDC) and yttria-doped ceria (YDC) have been considered as promising oxygen ion conducting electrolyte materials because they have higher ionic conductivity than YSZ below 700 °C.<sup>12,13</sup> In addition to the higher ionic conductivity, the doped ceria materials have higher surface exchange coefficients than YSZ since it is well known that there is a positive relation with oxygen ionic conductivity in the ceramic material.<sup>13</sup> This surface exchange coefficient is related to the oxygen reduction reaction at the electrochemical reaction sites of the cathode interface in the intermediate temperature regime (500–700 °C).<sup>14–16</sup> Previously in our laboratory, we conducted quantum mechanical simulation to calculate the activation energy for oxygen incorporation at the interface between Pt and YDC using density functional theory.<sup>17</sup> The energy barrier for the incorporation reaction is only 0.07 eV, while it is 0.38 eV for the YSZ interface with the Pt cathode.<sup>17</sup> Furthermore, experiments showed that the cathodic interface resistance for the YDC/Pt interface was much lower than that of the sample with the YSZ/Pt interface.<sup>17,18</sup> However, these doped ceria materials are chemically unstable in a reducing environment showing electron conduction. Thus, despite their superior ionic conductivity, applying only these materials as electrolytes is not suitable because of the lowered open circuit voltage (OCV). Therefore, to avoid the instability issue, many researchers have attempted to fabricate composite electrolytes in order to fully utilize the advantages of doped ceria oxides.<sup>17–20</sup> Grain boundaries with high concentration of oxygen vacancies on the cathode side of the electrolyte are the preferential pathways for oxygen incorporation, which are generated through dopant segregation. Through the hybrid Monte Carlo molecular dynamics simulation, it was reported that the dopant segregation of Gd<sup>3+</sup> ions is vivid near the surface of GDC, resulting in high oxygen vacancies at the surface.<sup>21</sup> Those oxygen vacancies are particularly concentrated in the grain boundary region, as reported in previous studies, showing that the Gd<sup>3+</sup> to Ce<sup>4+</sup> ratio is higher at the grain boundary than in the bulk region.<sup>22</sup> Due to the vigorous segregation of the dopant, Gd<sup>3+</sup>, the grain boundaries result in more oxygen vacancy formations. Accordingly, the surface exchange kinetics is hugely affected by the grain boundary density for oxygen incorporation. Therefore, in addition to the superior catalytic property of the doped ceria material, the grain boundary engineering of the doped ceria interlayer also plays an important role for surface kinetics.<sup>17,18</sup> A greater density of grain boundaries would contribute to higher oxygen vacancy concentration at the surface, thereby substantially reducing the polarization loss.<sup>23–27</sup> In this study, the catalytic role of samaria-doped ceria (SDC) cathodic interlayers on the LT-SOFC performance and grain boundary effects were fully investigated. We successfully fabricated SDC/YSZ composite electrolytes by using pulsed laser deposition (PLD). By varying the orientation of the YSZ substrate and the post heat treatment condition, we could systematically control the grain structures of the SDC interlayer deposited on the YSZ

substrate. Firstly, to verify the superior catalytic activity of the SDC/Pt interface compared to that of the YSZ/Pt interface, an epitaxial SDC interlayer with no grain boundary was deposited on the cathode side of a single YSZ substrate. Another sample set was prepared that has different grain structures of the SDC cathodic interlayer. The grain structure was controlled by varying the post-annealing temperature (750–1350 °C) after the deposition on polycrystalline YSZ substrate. As a result, larger grains were observed as the annealing temperature increased. The fuel cell performance for both cases was characterized by current–voltage (*i*–*V*) behavior measurements and electrochemical impedance spectroscopy (EIS) in the operating temperature range from 350 °C to 450 °C. It was observed that the fuel cell performance with an SDC interlayer was enhanced, and this was mainly due to the decreased cathodic interfacial resistance. In addition, the SDC interlayer with a nanogranular surface structure outperformed the fuel cell samples having larger grains due to the higher grain boundary density, which enhances the surface oxygen kinetics and significantly reduces the cathodic interface resistance in the measured temperature ranges. The results of this study provide significant implications for designing the composite electrolytes with nanostructured cathode surface grains to enhance the performance of LT-SOFCs.

## 2. Experimental

For the fabrication of the SDC/YSZ composite electrolyte, a 300 μm thick single crystalline YSZ (100) substrate (Marketech Inc.) was used as a guiding structure to deposit an epitaxial SDC cathodic interlayer with no grain boundary. To make the surface grain structured composite electrolyte, 100 μm thick polycrystalline YSZ substrates (BEANS International Corp.) were used to create polycrystalline SDC interlayers. All of the SDC thin interlayers were deposited via the PLD method, and a sintered Sm<sub>0.1</sub>Ce<sub>0.9</sub>O<sub>2</sub> disk pellet (Kurt J. Lesker Company) with 25.4 mm diameter and 3.175 mm thickness was used as a target. A Lambda Physik 248 nm KrF excimer laser was used, and the energy density was 1.5 J/cm<sup>2</sup> per pulse. Under a 100 mTorr oxygen gas environment in the deposition chamber, SDC layers were deposited while the substrate temperature was maintained at 750 °C. The sample-to-target distance was 50 mm, and about 60 nm of epitaxial and 400 nm of SDC thin films were deposited on single and polycrystalline YSZ substrates with a growth rate of 0.22 Å/pulse.

For engineering the surface grain sizes and grain boundary densities of the SDC interlayer, the deposited samples on the polycrystalline YSZ substrate were post-annealed at 750 °C, 1150 °C, and 1350 °C for 10 h in ambient air conditions. After the heat treatment process, the membrane–electrode-assembly (MEA) fabrication was completed by depositing porous Pt on both sides of the substrates as catalytic electrodes having reaction area of about 0.2 cm<sup>2</sup>. The deposition was conducted by dc sputtering under the conditions of 50 W of plasma power and 10 Pa of argon (Ar) background pressure for 150 s.

The composition of the deposited SDC layer was analyzed by X-ray photoelectron spectroscopy (XPS) in an SSI S-Probe monochromated XPS spectrometer with Al Kα radiation. The

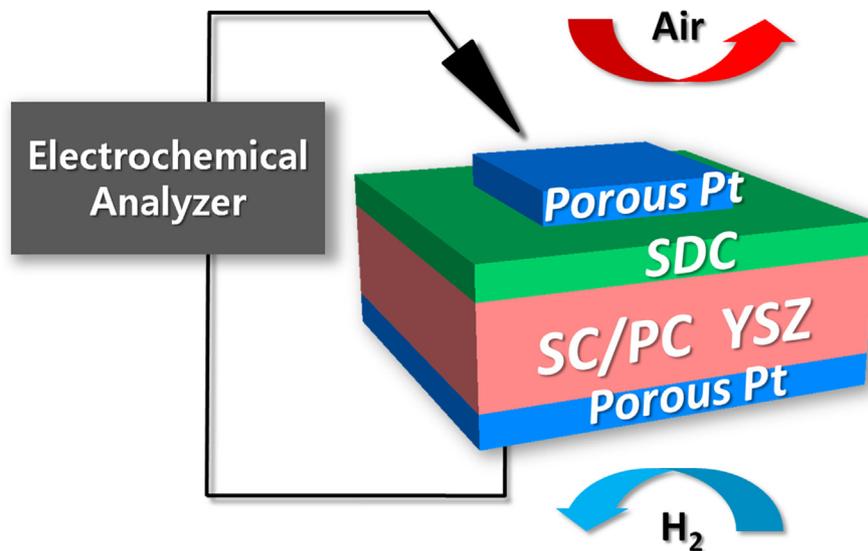


Fig. 1. Schematic diagram for the customized test set up with electrochemical analyzer and the entire MEA structure with SDC interlayer on single crystalline (SC) and polycrystalline (PC) YSZ electrolytes.

nanostructural phase and crystallinity of the SDC interlayers on single and polycrystalline YSZ substrates were analyzed by the X-ray diffraction (XRD) technique using a PANalytical X'pert PRO XRD system (Cu K $\alpha$  X-ray with  $\lambda = 1.54 \text{ \AA}$ ). Non-contact surface scanning mode atomic force microscopy (AFM, XE-70, Park Systems Inc.) was used to investigate the surface grain sizes of the SDC layers according to the post-annealing temperatures. The fuel cell performance measurement and electrochemical characterization were conducted with a customized micro-probing test station sitting on a temperature-controlled heating stage to maintain a constant temperature. Pure dry hydrogen was supplied as fuel through the chamber at the anode side while the cathode side was exposed to ambient air as shown in Fig. 1. The  $i$ - $V$  behaviors and EIS were measured by the electrochemical analyzer, a Gamry Potentiostat (FAS2, Gamry Instruments, Inc.). The fuel cell performance was measured at operating temperatures from 350 °C to 450 °C, and the EIS was measured under various cell voltage conditions in the frequency range from 300 kHz to 0.1 Hz. The obtained data was analyzed by using Zview software (Scribner Associate, Inc.).

### 3. Results and discussion

The atomic composition of the deposited SDC interlayer film on a YSZ substrate was analyzed through the XPS measurement. The measured XPS data showed the proper composition ratio of the SDC film ( $\sim 13 \text{ mol\% SDC}$ ), which is close to the  $\text{Sm}_{0.1}\text{Ce}_{0.9}\text{O}_2$  target composition, indicating that the SDC film was properly fabricated. The entire MEA of the SDC interlayered SOFCs used in this study is shown in Fig. 1.

To see the catalytic role of the SDC interlayer, an epitaxial SDC film that has no grain boundary was deposited on a single crystalline YSZ substrate. To confirm the epitaxial growth of the SDC interlayer, the crystalline structure of the deposited SDC film on the YSZ substrate was investigated through XRD measurement as exhibited in Fig. 2(a). As can be seen in the

XRD data, only a YSZ (100) peak and an intensive SDC (100) peak are observed, ensuring the epitaxial growth of SDC film on a single crystalline YSZ substrate. Fuel cell characterization was conducted for the epitaxial SDC interlayer on a single crystalline YSZ substrate, and was compared to that of only a YSZ controlled cell at 450 °C. Due to the epitaxial film of the SDC interlayer on the single crystalline YSZ (100) substrate, the fabricated cells could be assumed to have no grain boundary, which confirmed that the measurement would show only the catalytic effect of the SDC interlayer. Fig. 3 shows the  $i$ - $V$  behaviors for both cells. As shown in the  $i$ - $V$  plots, the peak power density of the SDC interlayered cell is twice as high as that of only the YSZ controlled cell. This result

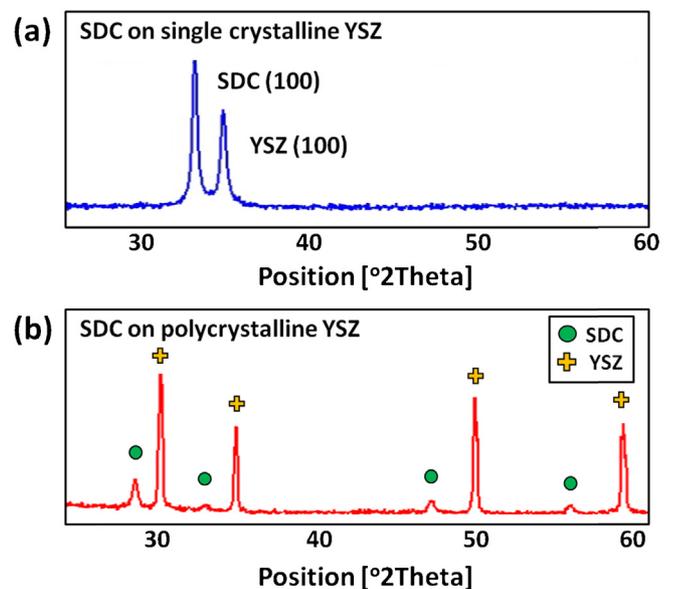


Fig. 2. X-ray diffraction (XRD) patterns for MEA with (a) epitaxial SDC interlayer on single crystalline YSZ substrate, and (b) fully developed SDC interlayer on polycrystalline YSZ substrate deposited by pulsed laser deposition (PLD) at 750 °C.

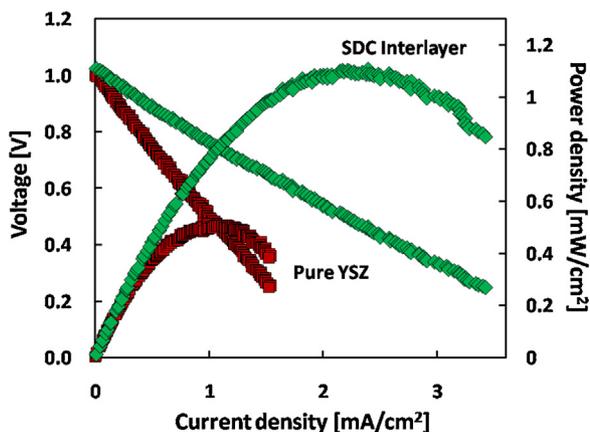


Fig. 3. Current–voltage ( $i$ - $V$ ) behavior of MEA with epitaxial SDC interlayer deposited on single crystalline YSZ substrate operating at 450 °C.

mainly stems from the enhanced cathodic interface kinetics of the SDC interlayer. The influence of the ohmic loss originating from the SDC interlayer could be neglected when the fuel cell performance is analyzed due to the superior ionic conductivity and much smaller thickness of the SDC interlayer ( $\sim 60$  nm) than those of YSZ substrate.<sup>12,13</sup> However, the superior surface exchange rate of the ceria-based materials would enhance the ORRs which results in the reduced cathodic interfacial resistance showing a higher peak power density.

The grain boundary effects of the SDC interlayers were analyzed with polycrystalline SDC interlayered cells. On the polycrystalline YSZ substrate, an SDC interlayer ( $\sim 400$  nm) was deposited that had a fully-developed polycrystalline structure, which corresponds to the polycrystalline property of the YSZ substrate as shown in Fig. 2(b). After the deposition of the SDC interlayer on the polycrystalline YSZ substrate at 750 °C, the post-annealing process was conducted for variations of the surface grain sizes and grain boundary densities at 750 °C, 1150 °C, and 1350 °C for 10 h. To see the surface topography, the post-annealed SDC film was investigated through AFM analysis, through which the grain size of each sample could be defined. Fig. 4 shows the AFM images of the various surface grains after the post-annealing process at 750 °C, 1150 °C, and 1350 °C, respectively. As seen in Fig. 4(a), nano grains (40–70 nm) of the SDC interlayer were observed at the annealing temperature of 750 °C. However, as the annealing

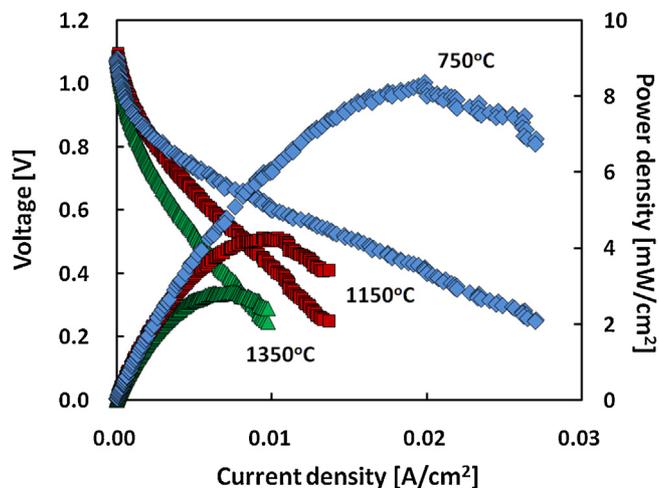


Fig. 5. Current–voltage behaviors of SDC interlayered MEAs with various annealing temperatures (750–1350 °C) measured at 450 °C.

temperature increased, the nano grains agglomerated and coarsened, becoming larger grains. The estimated grain sizes were 110–200 nm for annealing at 1150 °C, and 2–5  $\mu\text{m}$  for annealing at 1350 °C, as shown in Fig. 4(b) and (c), respectively. This tendency of the increasing grain size corresponds to decreasing grain boundary densities. Therefore, the post-annealing experiment suggests that a higher annealing temperature yields lower grain boundary densities.<sup>17–19</sup> The grain boundary effects were analyzed through the fuel cell characterization after the deposition of porous Pt electrodes on both sides of the samples. The post-annealed fuel cells having various grain sizes were characterized via  $i$ - $V$  measurements as shown in Fig. 5. The highest peak power density was observed with the smallest grain sized SDC interlayer, which was annealed at 750 °C. On the other hand, the peak power density becomes lower as the grain size increases. Therefore, it can be speculated that the higher grain boundary density (smaller grains) reduces the cathodic resistance by enhancing the surface exchange kinetics with a higher oxygen vacancy concentration at the grain boundary region, which well agrees with previous literature.<sup>17–20,23–27</sup> One may consider that the enhanced performance mainly came from the increase of the electrochemical reaction sites due to surface roughness increase after the SDC interlayer deposition. To exclude the possibility

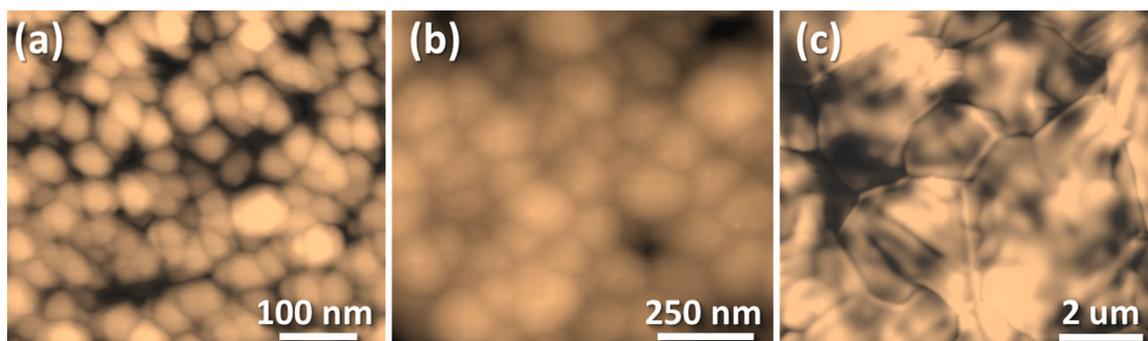


Fig. 4. Atomic force microscopy (AFM) images for surface topography of SDC interlayers deposited on polycrystalline YSZ substrate after annealing at various temperatures (a) 750 °C, (b) 1150 °C, and (c) 1350 °C, respectively.

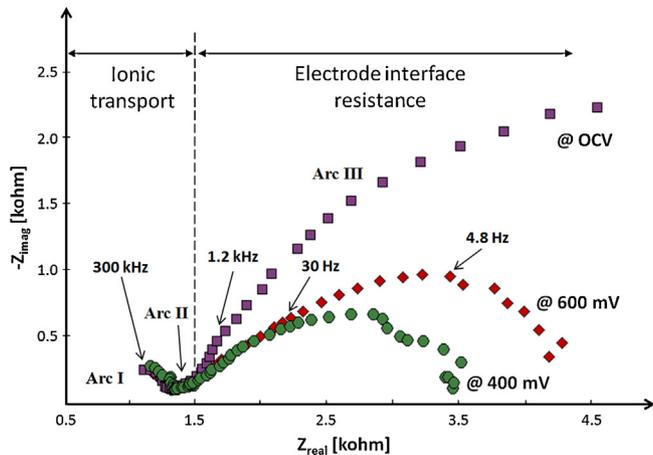


Fig. 6. The representative Nyquist plot of MEA with SDC interlayer on polycrystalline YSZ substrate annealed at 1350 °C. Electrochemical impedance spectroscopy (EIS) was conducted at 400 °C with different cell voltage conditions.

of surface roughness effect, root mean square (RMS) roughness values for each sample were measured and the average value was about 10 nm. Therefore, the contribution of the surface area roughness that increases the effective reaction area is negligible and the performance enhancement mainly came from the enhanced oxygen kinetics.

For more details of the grain boundary effects on the fuel cell performance, an EIS analysis was conducted in the temperature range of 350–450 °C. Fig. 6 shows the representative Nyquist plot of the 1350 °C annealed sample measured at 400 °C with different cell voltages of OCV, 400 mV and 600 mV. As seen in the Nyquist plot, no matter what voltage condition was applied, the high frequency loops did not change (Arc I and II), indicating that the high frequency loops correspond to the ionic transport through the bulk electrolyte (Arc I) and grain boundary (Arc II).<sup>12,18,19</sup> On the other hand, the low frequency loop (Arc III) changed according to the cell voltage conditions implying that the low frequency arc is relevant to the electrode interface resistance. Since the sluggish oxygen reduction reaction at the cathode interface is well known for the rate-determining step of LT-SOFCs, the cathode resistance is dominant for electrode polarization. Therefore, it can be suggested that the low frequency loop conforms to the cathode interface resistance.<sup>5–7,28–30</sup> To verify the relation between the grain boundary and electrode polarization loss, the electrode interface resistances were extracted for all the measurement samples with regard to the operating and annealed temperatures were obtained. Fig. 7 shows the Arrhenius plot for the measured electrode interface resistance values of the SDC interlayer/YSZ electrolyte MEAs at 0.6 V cell voltage conditions. It is clearly shown that the MEAs with higher annealing temperatures tended to have increased electrode interface resistances. The nano grain SDC interlayer annealed at 750 °C exhibited an electrode resistance that was 5–6 times lower than that of the 1150 °C annealed sample. In addition to the  $i$ - $V$  behaviors, the Arrhenius behaviors also verified that the nano grain SDC interlayer with a higher grain boundary density had a significantly lower electrode resistance (or cathode interface resistance) than the MEAs with lower

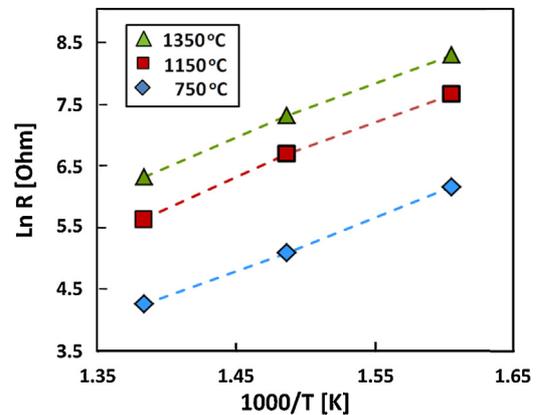


Fig. 7. Arrhenius plot showing interface electrode resistances of MEAs having different grain sized SDC interlayers on polycrystalline YSZ substrates after annealing at various temperatures (750–1350 °C). The extracted activation energies were about 0.7 eV.

grain boundary densities. These results agree well with previous studies and literature which indicate that the grain boundary plays an important role in oxygen incorporation with a low cathode interface resistance.<sup>17–19</sup> The low electrode resistance of the nano grain SDC interlayer originates mainly from the oxygen vacancy concentration at the grain boundary region.<sup>22,27</sup>

#### 4. Conclusion

The catalytic effect of SDC interlayers for surface oxygen kinetics has been investigated. Applying an SDC interlayer on a single crystalline YSZ substrate results in a peak power density that is twice higher than that of the YSZ controlled cell due to its fast surface exchange rate, which lowers polarization loss. Grain boundary effects are also investigated with various grain sizes (40 nm–5 μm) of the SDC interlayers. The highest cell performance was observed with the smallest grains (~45 nm), while the performance degraded as the grain size of the interlayers increased. This result suggests that higher grain boundary densities have lower cathodic interface resistance since more oxygen vacancies exist at the grain boundary region. Therefore, nano grains enhance the surface exchange kinetics by facilitating ORRs.

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