Piezoresistive Sensing Performance of Junctionless Nanowire FET

Pushpapraj Singh, Jianmin Miao, *Member, IEEE*, Vincent Pott, *Member, IEEE*, Woo-Tae Park, *Member, IEEE*, and Dim-Lee Kwong, *Fellow, IEEE*

***Abstract*—This letter investigates junctionless nanowire field-effect transistor (NWFET) (JL-NWFET) parameters such as piezoresistance and low-frequency noise (*LFN*) with respect to channel doping and gate bias. The JL-NWFET is piezoresistive, and its gauge factor (*GF*) is increased from 24 to 47 by reducing the channel doping ten times from 6.7×10^{19} to 6.7×10^{18} cm^{-3}. Significant variations of *GF* and *LFN* are observed when the JL-NWFET is operated from subthreshold to ON-state regime, and resolution (minimum detectable strain) is improved four times compared to inversion-mode NWFET. The simple fabrication and superior resolution formulate JL-NWFET as a promising sensing element for miniaturized nanoelectromechanical sensors.**

***Index Terms*—Junctionless field-effect transistor (JLFET), piezoresistivity, sensor resolution, strained silicon.**

I. Introduction

PIEZORESISTIVE sensors are widely used in various applications, such as measuring fuel pressure in automobiles or monitoring blood pressure [1], [2]. However, lower piezoresistive coefficient and higher electronic noise are serious limitations for piezoresistive sensors in measuring ultrasmall strain [3]. To improve the strain resolution, efforts have been made by using nanowire channel field-effect transistors (FETs) as piezoresistors [4], [5]. The piezoresistive coefficient was enhanced, but higher electronic noise (at inversion regime) and lower drain current (at subthreshold regime) are still major concerns in the nanowire FETs. Recently, junctionless (JL) FET has been reported with no physical junction between source and drain and offered advantages in terms of simple fabrication, reasonable ON/OFF ratio, low electronic noise, and elevated velocity saturation index [6]–[8]. In conjunction with all these advantages, since the JL nanowire field-effect transistor (NWFET) (JL-NWFET) channel is heavily doped, the concern is whether strain-induced resistance change can be efficiently used in these devices to further improve strain detection limits.

Manuscript received August 22, 2012; accepted August 29, 2012. Date of publication October 11, 2012; date of current version November 22, 2012. This work was supported by the Science and Engineering Research Council, Agency for Science, Technology and Research under Grant 102-165-0088. The review of this letter was arranged by Editor E. A. Gutiérrez-D.

P. Singh, V. Pott, and D.-L. Kwong are with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore 117685 (e-mail: singhp@ime.a-star.edu.sg).

J. Miao is with the Division of Engineering Mechanics, School of Mechanical and Automotive Engineering, Nanyang Technological University, Singapore 639798.

W.-T. Park is with the Department of Mechanical and Automotive Engineering, Seoul National University of Science and Technology, Seoul 139-743, Korea (e-mail: wtpark@seoultech.ac.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2012.2217112

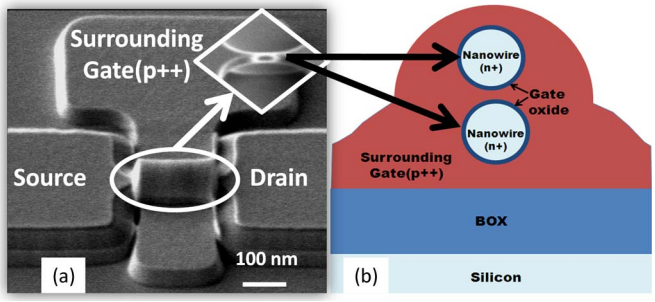

Fig. 1. (a) SEM image of JL-NWFET after the gate patterning. Inset shows a pair of twin silicon nanowires before the gate formation. NW length and diameter are 160 and 10 nm, respectively. (b) Cross-sectional view of the n-type JL-NWFET.

This letter aimed at analyzing the piezoresistive behavior of gate-all-around (GAA) JL-NWFET to find its suitability for strain sensing applications. The electromechanical properties of the JL-NWFET are characterized, and the strain-induced change in the drain current (ΔI_{DS}) is measured. Results present the following: 1) the channel doping and 2) the gate bias impact on the piezoresistance and low-frequency noise (*LFN*). The GAA JL-NWFET device has simple fabrication, and the electromechanical results reveal better piezoresistive sensing capability in comparison with a conventional GAA NWFET.

II. Device Fabrication

The JL-NWFET devices were fabricated on 8-in p-type (100) silicon-on-insulator wafers with a device layer of 117 nm and a buried oxide of 145 nm. Top silicon device layer was doped with n-type (arsenic) using ion implantation. Three sorts of devices were considered with doping concentrations of 6.7×10^{18}, 1.3×10^{19}, and 6.7×10^{19} cm^{-3}, named as devices A, B, and C, respectively. Silicon fins (width $= 50$ nm and thickness $= 117$ nm) were achieved with deep UV patterning and oxidized to convert into twin nanowires (diameter $= 10$ nm). The twin nanowire formation (one top and one bottom) is achieved by designing proper aspect ratio (thickness/width) for the silicon fin. The complete oxidation of nanowires was prevented due to stress-limited oxidation [9]. It was followed by 4-nm gate oxide and 130-nm gate electrode (amorphous Si) deposition and then heavy p^{++} doping (dose $= 1 \times 10^{16}$ cm^{-2}). The gate electrode was then patterned, and metallization process completed the JL-NWFET fabrication. Fig. 1(a) shows the SEM image of the JL-NWFET after gate patterning, and Fig. 1(b) shows the cross-sectional view of the n-channel JL-NWFET. The heavy p^{++} doping in the gate electrode was used to deplete the channel carriers from

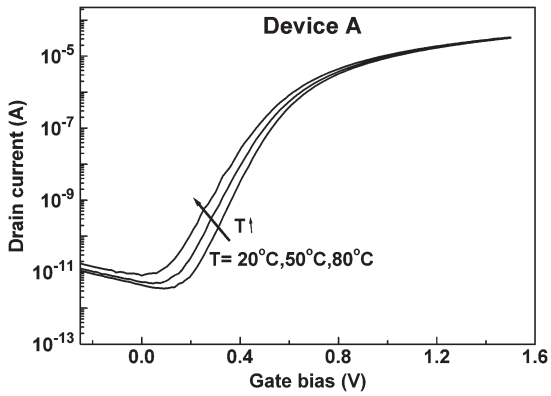

Fig. 2. Measured $I_{\rm DS}-V_{\rm GS}$ characteristics at various temperatures of JL-NWFET ($V_{\rm DS} = 2.5$ V, $L = 160$ nm, and $d = 10$ nm).

$Si-SiO_2$ interface and to operate the doped nanowire channel as an enhancement-type FET.

III. Results and Discussion

The JL-NWFET devices were tested to investigate the dependence of the electrical characteristics on the mechanical strain. Fig. 2 shows the $I_{\rm DS}-V_{\rm GS}$ characteristics for JL-NWFET (device A) at different temperatures. At room temperature, the JL-NWFET device exhibited a high $I_{\rm ON}/I_{\rm OFF}$ ratio of seven orders of magnitude with a subthreshold slope of 67 mV/dec. The GAA structure facilitated carrier depletion in the nanowire channel, and observed threshold voltage [$V_{\rm th} = 0.6$ V (device A)] was similar to that of the n-channel inversion-mode NWFET. Fig. 2 shows that the drain current increases at higher temperatures and confirms the JL behavior for the device A. The increase of drain current at higher temperatures is attributed to the heavy channel doping and bulk carrier conduction, which produce lower phonon scattering in JL-NWFET [10].

Next, the piezoresistive response of JL-NWFETs was established by calculating the relative drain current change per unit strain. The piezoresistive sensitivity is represented in terms of gauge factor (GF) (GF $= (\Delta I_{\rm DS}/I_{\rm DS})/\varepsilon$), where $(\Delta I_{\rm DS}/I_{\rm DS})$ and ε are the relative change in the drain current and applied strain, respectively. A four-point bending technique was used to generate uniform longitudinal tensile strain in the JL-NWFET channel [5], and the piezoresistive measurements are compared for the devices A, B, and C. The piezoresistive effect in FETs generally originates from the following: 1) strain-induced changes in energy-band structure and 2) intervalley scattering effect. Under the applied strain, the energy of conduction-band minima changes, and carriers start to redistribute among the valleys of dissimilar effective masses. The carrier concentration then increases/decreases in lower effective mass valleys, and average mobility that is increased/decreased results in the higher/lower drain current.

Fig. 3 shows that the JL-NWFET piezoresistive sensitivity increased when the doping concentration was decreased and confirmed a higher GF for devices with a lower channel doping concentration. Furthermore, the piezoresistive sensitivity was also measured when gate voltage varied from ON-state (above threshold) to the subthreshold mode of operation. The results confirm considerable gate bias influence on the piezoresistive properties of JL-NWFET. Fig. 3(a)–(c) shows that the normalized current change increased at lower gate bias and indicated a higher *GF* near threshold region. The higher *GF* near subthreshold regime may be attributed to the variation of effective channel width. The depletion region width depends on the doping profile, and increase in nanowire doping concentration results in reduced depletion region width. When gate bias is reduced, the width of the depletion region increases from all sides of nanowire, and cross-sectional area of the channel reduces. As higher piezoresistivity was reported for the smaller nanowire diameter [4], the reason of *GF* enhancement in subthreshold regime is the reduction of effective channel width.

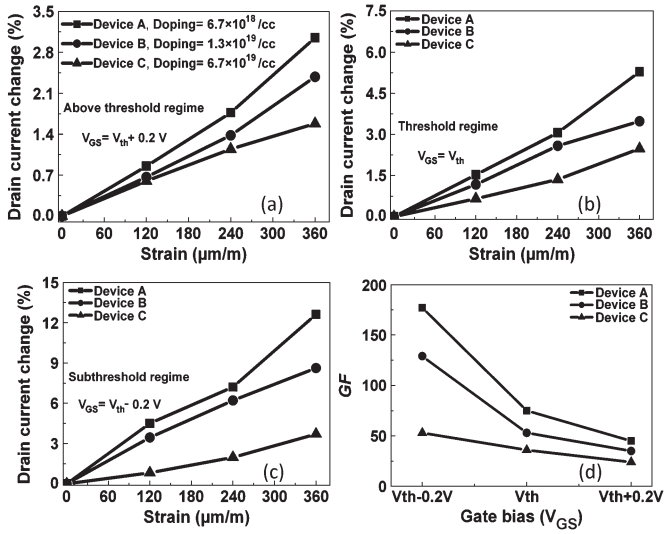

Fig. 3. Drain current variations versus longitudinal strain for the JL-NWFET devices under different biasing conditions (ON-state to subthreshold region): (a) $V_{\rm GS} > V_{\rm th}$, (b) $V_{\rm GS} = V_{\rm th}$, and (c) $V_{\rm GS} < V_{\rm th}$. (d) Gauge factor variations for the different channel doping JL-NWFETs at different gate biasing voltages.

Furthermore, as shown in Fig. 3(d), compared to the inversion region ($V_{\rm GS} = V_{\rm th} + 0.2$ V), the *GF* is enhanced four times for device A and two times for device C in the subthreshold region ($V_{\rm GS} = V_{\rm th} - 0.2$ V). As depletion width variation is less for the highly doped regions under similar gate bias, the high *GF* enhancement in device A can be explained due to the larger channel width variation compared to the higher doping (devices B and C). These results strongly support that the *GF* enhancement rate depends on the depletion width variation, and hence, higher enhancement rate is obtained for the lower doping channel (device A).

Fig. 4 shows the drain current noise dependence on the frequency for different operating bias regimes. The *LFN* has marginal $1/f$ dependence when JL-NWFET device operates at/below threshold voltage. *LFN* starts to follow the $1/f$ dependence once gate bias $(V_{\rm GS})$ exceeds the threshold voltage $(V_{\rm th})$. The JL-NWFET has lower *LFN* magnitude compared to inversion-mode NWFET, and it is mainly attributed to the bulk carrier conduction. The bulk conduction helps to keep the carriers away from the silicon–silicon dioxide interface, and less scattering results in less *LFN* magnitude. The GAA JL-NWFET *LFN* is different from the recently reported trigate JL n-FET in [11]. JL trigate channel forms near to the bottom interface, and *LFN* is affected with the interface interaction. However, channel formation in GAA structure starts from the nanowire core and then expands toward the interface, keeping the *LFN* free from interface scattering [12].

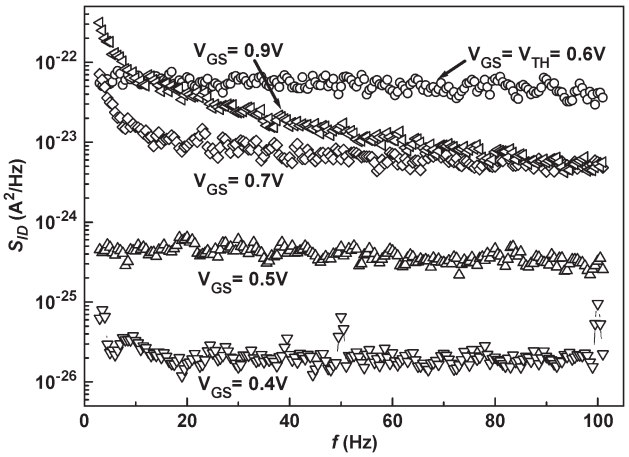

Fig. 4. Drain–current noise power spectral density ($S_{\rm ID}$) versus frequency for JL-NWFET ($V_{\rm DS} = 0.1$ V).

TABLE I
BENCHMARK COMPARISON OF DIFFERENT SENSING ELEMENTS USED FOR STRAIN SENSING

Work	Sensing element	Spectral noise	Gauge factor	*MDS*
Rasmussen et al. [3]	Doped piezoresisitor	2.7 μV/√Hz	~30	3.3 X10^{-6}
Helbling et al. [13]	CNTFET	~1 μA/√Hz	~(1-463)	6.2 X10^{-6}
Singh et al. [5]	NWFET	~(100-1) pA /√Hz	~(60-250)	1.5 X10^{-7}
JL-NWFET (This work)	**Junctionless NWFET**	**~1pA/√Hz**	**~(30-175)**	**3.8 X10^{-8}**

The performance of the JL-NWFET strain sensing element is estimated by calculating the term minimum detectable strain "MDS $= (A/\text{GF} \times I_{\rm DS})$," which is defined as the drain current noise amplitude (A) divided by the strain sensitivity. Due to the higher doping concentration in the nanowire channel, the *GF* value was found lower for JL-NWFET. However, the less carrier scattering helped to get lower *LFN* even at above-threshold gate bias. The higher gate bias and twin nanowire channel turn out that high on-current and lower MDS $\sim 3.8 \times 10^{-8}$ value were obtained in ON-state ($V_{\rm GS} = V_{\rm th} + 0.2$ V) for device A. The extracted results for JL-NWFET MDS are compared with the doped piezoresistors [3] and FET-based sensing elements [5], [13], as shown in Table I.

The optimization results of JL-NWFET with doping concentration and operating gate bias present significant enhancement in resolution and signify JL-NWFET as a promising sensing element for nanoelectromechanical sensors.

IV. CONCLUSION

This work has presented JL-NWFET as a miniaturized sensing element with improved strain detection capability. High-work-function gate restrains the carrier travel through the core of the silicon body in JL-NWFET, and thus, there is less interaction with $\rm Si-SiO_2$ interfaces, resulting in much lower *LFN* compared to the inversion-mode counterpart. An assessment of the piezoresistance and device noise characteristics showed significant performance improvements with the right choice of operating parameters. Finally, the verification of lower noise and four times better *MDS* confirms the feasibility of the JL-NWFET as a promising miniaturized sensing element for nanoelectromechanical sensors.

ACKNOWLEDGMENT

The authors would like to thank Dr. N. Singh of the Institute of Microelectronics, Agency for Science, Technology and Research, for fruitful discussions.

REFERENCES

[1] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. E. Mansy, "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, Nov. 2004.

[2] C. Pramanik, H. Saha, and U. Gangopadhyay, "Design optimisation of a high performance silicon MEMS piezoresistive pressure sensor for biomedical applications," *J. Micromech. Microeng.*, vol. 16, no. 10, pp. 2060–2066, Oct. 2006.

[3] P. A. Rasmussen, J. Thaysen, O. Hansen, S. C. Ericsen, and A. Boisen, "Optimised cantilever biosensor with piezoresistive read-out," *Ultramicroscopy*, vol. 97, no. 1–4, pp. 371–375, Oct./Nov. 2003.

[4] R. He and P. Yang, "Giant piezoresistance effect in silicon nanowires," *Nat. Nanotechnol.*, vol. 1, no. 1, pp. 42–46, Oct. 2006.

[5] P. Singh, W.-T. Park, J. Miao, L. Shao, R. K. Kotlanka, and D.-L. Kwong, "Tunable piezoresistance and noise in gate-all-around nanowire field-effect transistor," *Appl. Phys. Lett.*, vol. 100, no. 6, pp. 063106-1–063106-4, Feb. 2012.

[6] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, l. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.

[7] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053511-1–053511-2, Feb. 2009.

[8] B. Sorée, W. Magnus, and G. Pourtois, "Analytical and self-consistent quantum mechanical model for a surrounding gate MOS nanowire operated in JFET mode," *J. Comput. Elect.*, vol. 7, no. 3, pp. 380–383, Sep. 2008.

[9] J. Kedzierski, J. Bokor, and C. Kisielowski, "Fabrication of planar silicon nanowire on silicon-on-insulator using stress limited oxidation," *J. Vac. Sci. Technol.*, vol. 15, no. 6, pp. 2825–2828, Nov. 1997.

[10] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "High-temperature performance of silicon junctionless MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 620–625, Mar. 2010.

[11] D. Jang, J. W. Lee, C. W. Lee, J. P. Colinge, L. Montés, J. Lee, G. T. Kim, and G. Ghibaudo, "Low-frequency noise in junctionless multigate transistors," *Appl. Phys. Lett.*, vol. 98, no. 13, pp. 133502-1–133502-3, Mar. 2011.

[12] B. Sorée, W. Magnus, and W. Vandenberghe, "Low-field mobility in ultrathin silicon nanowire junctionless transistors," *Appl. Phys. Lett.*, vol. 99, no. 23, pp. 233509-1–233509-3, Dec. 2011.

[13] T. Helbling, C. Roman, and C. Hierold, "Signal-to-noise ratio in carbon nanotube electromechanical piezoresistive sensors," *Nano Lett.*, vol. 10, no. 9, pp. 3350–3354, Sep. 2010.