An Inductively Powered Implantable Blood Flow Sensor Microsystem for Vascular Grafts

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***Abstract*—Monitoring blood flow rate inside prosthetic vascular grafts enables an early detection of the graft degradation, followed by the timely intervention and prevention of the graft failure. This paper presents an inductively powered implantable blood flow sensor microsystem with bidirectional telemetry. The microsystem integrates silicon nanowire (SiNW) sensors with tunable piezoresistivity, an ultralow-power application-specific integrated circuit (ASIC), and two miniature coils that are coupled with a larger coil in an external monitoring unit to form a passive wireless link. Operating at 13.56-MHz carrier frequency, the implantable microsystem receives power and command from the external unit and backscatters digitized sensor readout through the coupling coils. The ASIC fabricated in 0.18-μm CMOS process occupies an active area of 1.5 $\times$ 1.78 mm^2 and consumes 21.6 μW only. The sensors based on the SiNW and diaphragm structure provide a gauge factor higher than 300 when a small negative tuning voltage (−0.5–0 V) is applied. The measured performance of the pressure sensor and ASIC has demonstrated 0.176 mmHg/$\sqrt{\text{Hz}}$ sensing resolution.**

***Index Terms*—Blood flow monitoring, implantable biomedical IC, inductively powered, passive telemetry, piezoresistive sensor, successive approximation register analog-to-digital converters (SAR ADC), sensor interface IC, silicon nanowire (SiNW).**

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I. Introduction

PROSTHETIC grafts are frequently used in vascular surgery in the context of a bypass for lower limb ischemia or a conduit for haemodialysis in renal failure. At least 20–30% of the existing renal haemodialysis population has a prosthetic vascular graft *in situ*. In addition, thousands of lower limb bypasses are performed all over the world yearly, of which at least 20% require the use of prosthetic grafts. However, prosthetic grafts are prone to developing progressive stenosis, thrombosis, and ultimately graft abandonment. Thorough analysis of relations among graft blood flow, stenosis, luminal diameters, and other key variables in the graft circuit is presented in [1]. Flow rate monitoring provides an indication for early intervention to prevent graft failure. However, no single blood flow sensing technique has been adopted for frequent monitoring of the prosthetic graft. Advantages and disadvantages of various flow measurement techniques, such as ultrasound, computed tomography scan and formal angiograms, are explained in [2]. These techniques come with some procedural morbidity, significant amount of time and cost, and/or the exposure to the nephrotoxic contrast, making the frequency of their use very limited and not useful for the early detection of failing grafts. Therefore, an implantable sensor microsystem paired with a simple hand-held device for wireless telemetry and power transfer is highly desirable to provide convenient monitoring of the blood flow in prosthetic vascular grafts.

In this paper, an ultralow-power implantable microsystem that can be embedded within the vascular graft as shown in Fig. 1 is presented. The microsystem senses the blood flow rate and transmits the information through wireless interface to an external hand-held device. It is powered through the inductive link consisting of two coils in the implant and one coil in the external device. The command and data communication also occur through this wireless link. The blood flow over microelectromechanical systems (MEMS) devices causes the mechanical deformation in sensing elements, translating into the electrical signal through the piezoresistive transduction. The piezoresistive sensing element is a silicon nanowire (SiNW) and its piezoresistivity and conductivity are electrically tunable through a gate structure. The sensor is not only sensitive enough to provide a necessary sensing resolution while covering the required range, but also small enough to not to affect the blood flow and cause any blood clotting. An ultralow-power IC interfacing with this sensor was presented in [3] for implantable wireless blood flow measurement. The developed flow sensing microsystem demonstrates an excellent sensing performance with small dimensions and low

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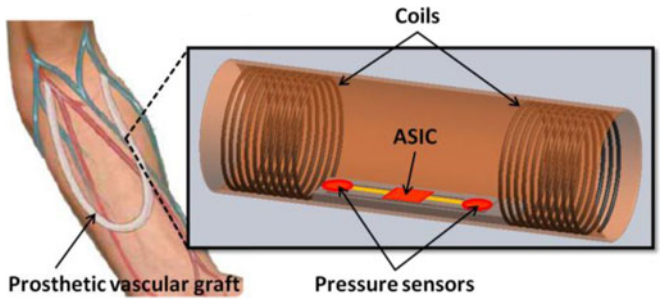


Fig. 1. Wireless implantable blood flow sensor microsystem including two MEMS pressure sensors, an ASIC and two coils. The microsystem measures the blood flow rate inside prosthetic vascular grafts to detect graft degradation at early stage for timely intervention and prevention of the graft failure.

power consumption. The overall microsystem integrating the piezoresistive sensor, the application-specific integrated circuit (ASIC), and the coupling coil are described in Section II. The details of ASIC building blocks are elaborated in Section III. In Section IV, the system characterization results are presented, followed by the conclusion in Section V.

II. Implantable Wireless Sensor Microsystem

The overall system architecture is shown in Fig. 2, consisting of an implant device that is the wireless sensor microsystem and an external hand-held device. The implantable microsystem integrates two MEMS pressure sensors, an ASIC and two coils. Each piezoresistive sensor produces resistance change in correspondence to the pressure applied by the flowing blood. The difference between the pressure values detected by two sensors is used to calculate the flow rate. The ASIC converts the resistance change into the form of voltage, digitizes it, and communicates this digital sensor readout data through a passive wireless telemetry. The coils serve two purposes in the microsystem—1) an inductive coupling with a primary coil placed in the hand-held device outside the patient's body, through which power and command are delivered to the ASIC and the digitized sensor data are backscattered to the external device; 2) a mechanical anchor to hold the sensors in position when blood flows. The communication distance of the system is determined by the coupling efficiency of RF energy from the external device to the implanted coil, conversion efficiency from the received RF power to the useful dc power, and the power consumption of the wireless flow-sensing ASIC. The range of depths for haemodialysis and prosthetic grafts is typically less than 2 cm.

A. Nanowire Piezoresistive Sensor

With the advances in technology, nanodevices have been developed to increase the piezoresistive coefficient of silicon by the minimization of size. SiNW has demonstrated giant piezoresistance because of the reduced dimension as well as large surface to volume ratio. Since a mechanical stress applied to an SiNW causes a dramatic change in the number of its charge carriers, the SiNW exhibits a large piezoresistance that can be modulated by an electric field perpendicular to its current flow [4]. By adding a proper gate structure surrounding the nanowire as shown in Fig. 3, a stress-gated field effect transistor (FET) is created, providing a large and tunable piezoresistance [5]. The piezoresistive effect in SiNW is improved by seven times compared to conventional piezoresistors.

In order to avoid the potential risk of sensitivity degradation due to endothelialization which cantilever-type structures may have, a diaphragm-based structure is used. A stack of silicon nitride and silicon oxide layers forms a membrane, and the piezoresistive single-crystalline SiNW FET is employed as a sensing element. The piezoresistive sensing element is embedded at the edge of the circular diaphragm as shown in Fig. 3. The circular membrane with a diameter of 200 μm is chosen for ease of backside release using deep reactive-ion etching. The membrane thickness of 2 μm is to minimize initial deflection. This MEMS sensor design allows robust and sensitive pressure measurement with the gate-surrounding SiNW and low noise level with a negative gate bias. The details of MEMS pressure sensors and SiNW can be found in [5]–[7].

B. Ultralow-Power ASIC

As shown in Fig. 2, the ASIC consists of a sensor interface circuit, an analog-to-digital converter (ADC), a digital baseband (DBB), a low-dropout (LDO) regulator, and front-end circuits for wireless powering and bidirectional telemetry that include rectifiers, limiters, a modulator, a demodulator, a clock extractor, and a power-on reset (POR) generator.

When the external monitoring unit is placed in close proximity to the implant microsystem and the passive sensing operation initiates, the external unit transmits the RF power through the carrier at 13.56 MHz. The carrier is ASK-modulated to send commands to the implant. After skin and tissue absorption, only a small fraction of the RF energy reaches the implant. The parallel resonant *LC* tanks and the rectifiers convert the received RF energy to the dc energy, followed by the LDO regulator to power the ASIC with the regulated dc supply. The incoming modulated carrier is demodulated by the ASK demodulator and despread by the DBB to configure the system parameters such as integration time, amplifier gain, selection between two sensors, resonance tuning, and modulation index. At the same time, the clock is extracted from the incoming carrier and provided to the DBB. The clock fed into the clock management block in the DBB is processed by frequency dividers to generate several low-frequency clocks including the sampling clock of 106 kHz for the ADC.

Once the system parameters are set according to the received commands, the digital core sends out readout enable signal, and the sensor interface circuit reads a resistance of the selected MEMS pressure sensor and produces a voltage output inversely proportional to the sensor resistance. The analog voltage output from the sensor interface circuit is converted into digital data by the successive approximation register ADC (SAR ADC). The digital data are spread and formatted by the DBB and sent to the load modulator that backscatters the incoming RF carrier according to the sensor data bit stream from DBB.

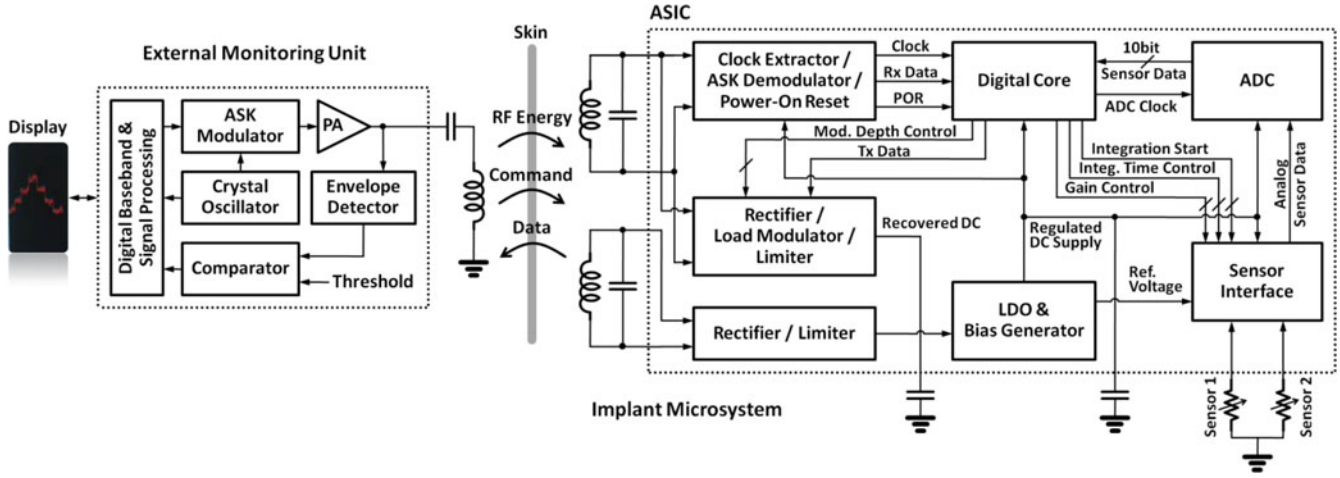


Fig. 2. Architecture of the implantable blood flow monitoring system consisting of an implant wireless flow-sensing microsystem and external monitoring unit. The ASIC block diagram is also shown.

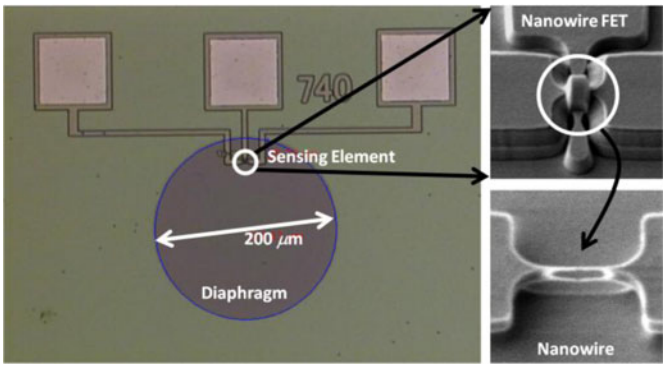


Fig. 3. Fabricated MEMS pressure sensor using a stack of silicon nitride and silicon oxide layers to form a 2-um-thick membrane and a piezoresistive SiNW FET as a sensing element.

C. Inductive Link

The wireless powering obviates the need of battery that fundamentally limits the miniaturization of implantable microsystems and causes inconvenience in replacement and recharging. Eliminating the battery also precludes the risk of infection and postimplant trauma for patients. However, the design of wireless power link is strictly limited by the implant size and the allowed transmission power in the consideration of living tissue safety. It is, therefore, important to achieve a high coupling efficiency while using a small implant coil and design a low-power ASIC for the implant.

Considering that at frequency range around 20 MHz, the losses of RF power transfer through biological tissue are mainly due to the reflections on the interface and do not present danger to the tissues, ISM band 13.56 MHz is chosen as the carrier frequency [8]. The implant coil is wrapped around an implant polytetrafluorethylene (PTFE) graft with a diameter of 6 mm. The coil material is Nitinol with biocompatible coating (ETFE). The external coil made of copper in the shape of solenoid with a diameter of 10 cm surrounds the implant coil. The quality factor and coupling coefficient of the implant and external coils are optimized to achieve the maximum power transfer efficiency so that the power link can provide the energy large enough to operate the microsystem. The prosthetic graft is implanted at the depth of 5–50 mm from the skin, and the implant coils and the external coil can be misaligned in practice.

III. ASIC Design

In the flow sensor microsystem, the ASIC interfaces with coils and sensors to power the microsystem, detect the flow rate, and communicate with the external device. While providing the required sensing performance, it is important to achieve low power consumption in operating the ASIC, as well as high efficiency in converting the RF power to the regulated dc power.

A. RF-to-DC Power Conversion and Load Modulation

The RF-to-dc power conversion circuit connects with the coupling coil, which resonates with a programmable array of on-chip capacitors at the input of rectifier. The power conversion efficiency (PCE) of the CMOS rectifier is mainly limited by dropout voltage of the rectifier associated with the transistor threshold voltage $V_{\rm th}$, and on-resistance $R_{\rm on}$ and reverse leakage current ($I_{\rm leak}$) of the transistors. In this design, eight-stages of differentially driven rectifiers [9] are used as shown in Fig. 4. The active differential $V_{\rm th}$ cancellation scheme implemented in the rectifiers reduces the effective $V_{\rm th}$, $R_{\rm on}$, and $I_{\rm leak}$ simultaneously to achieve high PCE. In the steady state, the common-mode component of V_A and V_B that is about a half of dc output V_0 biases gates of NMOS and PMOS transistors to reduce effective $V_{\rm th}$ and $R_{\rm on}$ of transistors. In addition, the gates of transistors are actively biased by differential-mode component of V_A and V_B. For example, when V_A goes positive, the differential counterpart V_B decreases the gate voltage of $M_{N0\ A}$ to reduce its $I_{\rm leak}$. When V_A goes negative, V_B increases the gate voltage of $M_{N0\ A}$ to reduce its effective $V_{\rm th}$ and $R_{\rm on}$. Eight stages of such rectifiers are connected to the differential RF input, $V_{\rm RFP}$ and $V_{\rm RFN}$ in parallel, while connected in series along the dc path to generate appropriate dc output voltage $V_{\rm DC}$ that is

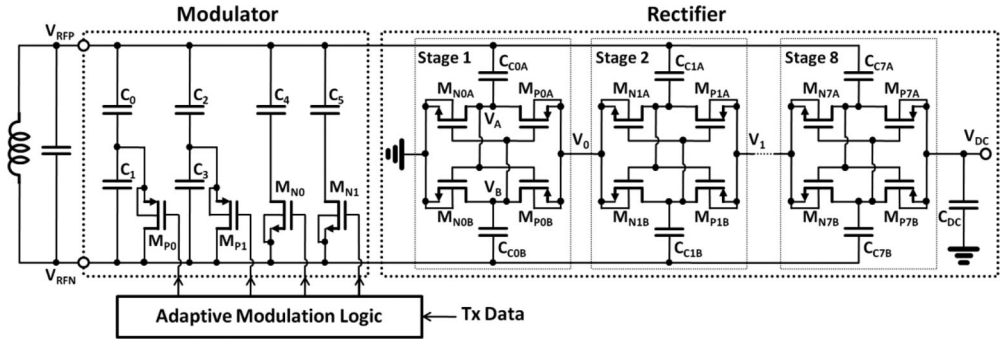


Fig. 4. Simplified diagram of RF-to-dc conversion and load modulation circuits. Eight stages of differentially driven rectifiers [9] are used for high-efficiency RF-to-dc conversion. A programmable array of on-chip capacitors are used for resonance tuning and variable-depth load modulation.

1.2–1.8 V in this design. A voltage limiter (not shown in Fig. 4) is also added for the protection of subsequent circuits. A PCE of approximately 70% is obtained with 20-kΩ output load.

The reverse wireless link is implemented using backscatter modulation by reflecting the incident carrier. Modulated reflection is achieved by varying the load impedance of the passive wireless link, which means the RF front-end input impedance of the implant ASIC. The input impedance can be modulated by shunting the circuit with either a resistor or a capacitor. While broadband in nature, the disadvantage of resistive modulator is being lossy, having unequal power delivery to the rectifier at the two modulated impedance states. On the contrary, if the reactive part of the input impedance is modulated symmetrically, a capacitive modulator is capable of delivering constant power to the rectifier at both impedance states. Hence, the capacitive modulator is chosen for a more stable supply during backscatter modulation, as shown in Fig. 4.

One important challenge in passive wireless link for an implant device is difficulty in achieving a good matching. Optimum values of input matching components cannot be known precisely before actual implantation due to the uncertainty of implantation depth, surrounding tissue composition, and alignment between coupling coils. In order to mitigate this issue, a programmable array of on-chip capacitors shown in Fig. 4 is used as a load modulator to tune the resonance capacitance value. The same array can be also used for varying modulation depth.

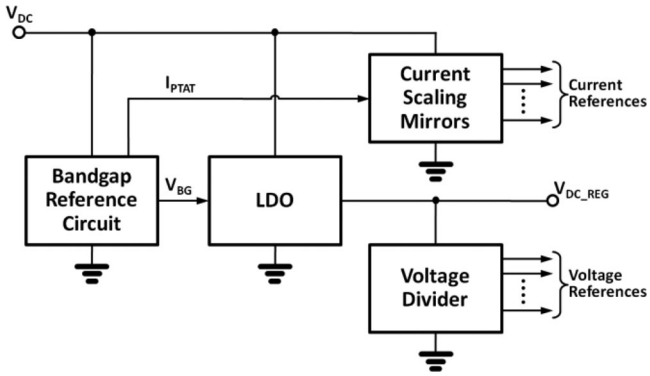


Fig. 5. Block diagram of power management circuits.

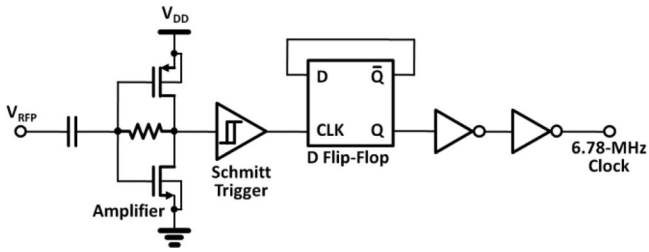


Fig. 6. Schematic diagram of the clock extractor.

B. Power Management

All the analog and digital blocks in the ASIC are designed to operate at 1-V supply and require several voltage and current references. The power management circuits consist of a bandgap reference circuit, an LDO voltage regulator, and voltage and current reference generators as shown in Fig. 5. The bandgap voltage generator produces a 1.2-V reference for the rest of power management circuits. The LDO regulator receives the unregulated dc voltage $V_{\rm DC}$ from the rectifier and provides all the internal circuit blocks with a well-defined 1-V supply, $V_{\rm DC\_REG}$. The current scaling mirrors generate the reference currents of 10 nA, 100 nA, and 1 μA from the proportional-to-absolute-temperature current produced by the bandgap circuit. The resistive voltage divider generates the reference voltages of 0.1, 0.2, 0.3, 0.5 and 0.7 V from $V_{\rm DC\_REG}$ for the analog circuits.

C. Clock Extraction, Demodulation, and POR Generation

Fig. 6 shows the clock extraction circuit composed of a resistive shunt feedback amplifier with its input ac-coupled and a following Schmitt trigger that edge-triggers a D flip-flop with its inverting output tied to its input [10]. The 13.56-MHz clock is extracted from the carrier, divided by two, buffered, and fed to the clock management block in DBB as a reference system clock signal.

The ASK modulation is a method commonly used for sending command at low data rate, to set the configuration of implant devices. The ASK demodulator shown in Fig. 7 extracts the command sent by the external unit. The envelope of the received ASK-modulated carrier is detected and compared with

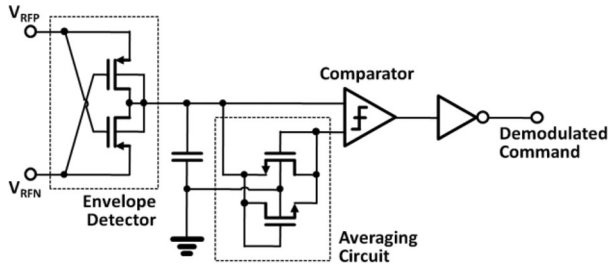


Fig. 7. Schematic diagram of the ASK demodulator.

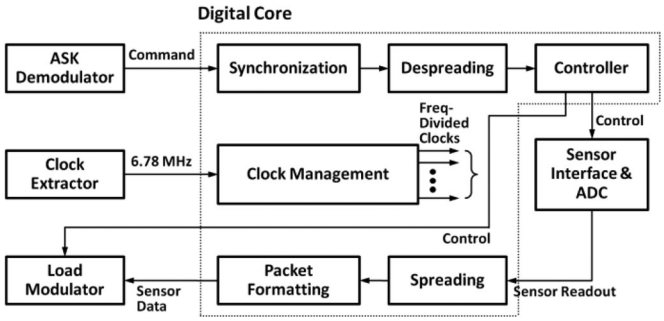


Fig. 8. Block diagram of DBB circuits.

the average value of the envelope to obtain the demodulated command signal.

The POR signal is generated by using the extracted clock as an input to the *RC* filter, the output of which is fed to a Schmitt trigger followed by a 100-μs delay circuit. The output of the delay circuit is used for resetting the registers in digital circuits.

D. Digital Baseband

Fig. 8 shows the block diagram of the DBB circuits that realize baseband signal processing such as synchronization, despreading, spreading, and packet formatting. It also generates the clocks and control signals for the sensor interface circuit and SAR ADC, and controls the states of the implant microsystem: *Idle*, *Reception*, *Processing,* and *Transmission*.

There are 16 information bits in one frame from the external monitoring unit to the implant device, to set the parameters such as selection between two sensors, integration time, gain, resonance tuning, and modulation index. In order to improve the robustness of the wireless communication, all the information bits are spread into seven chips. A maximum length sequence (M-sequence) with register length $m = 3$ is used as spreading sequence. The M-sequence generator is shown in Fig. 9 and the corresponding sequence is [0 0 1 1 1 0 1]. There are 12 bits in one frame from the implant device to the external unit. The first bit is the sensor identification (ID), followed by 11 bits of sensor readout data. All the data are again spread into seven chips. The start-of-frame (SOF) and end-of-frame (EOF) are generated and prefixed to each frame.

The state machine controls the operation of the implant microsystem. Before it receives any carrier signal from the external unit, the implant device stays in *idle* mode. As the carrier starts to come in, the implant device goes to *reception* mode after

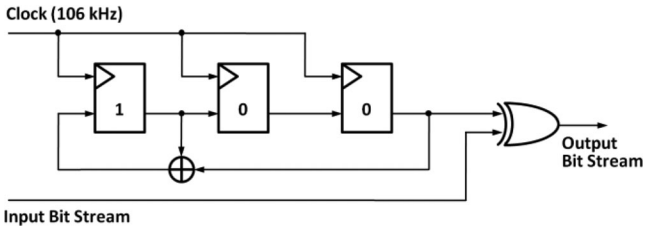


Fig. 9. M-sequence generation circuit used for spreading and despreading.

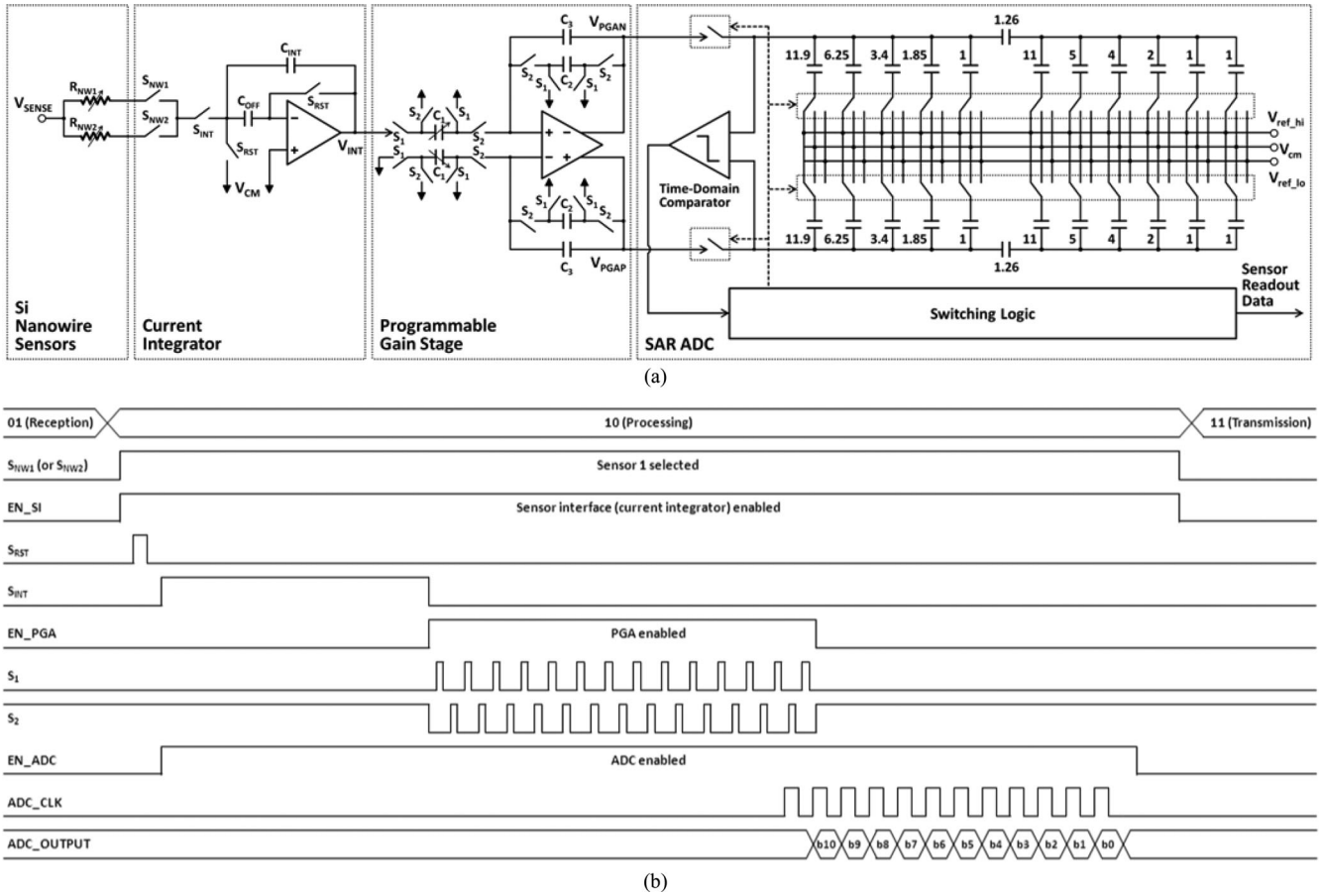
the clock is ready and the registers are reset by POR signal. It starts to search the SOF and receive the data frame. After all the information bits are received and despread, the tag system goes to *processing* mode. The parameters for the sensor interface and SAR ADC circuits are set based on the received information bits. Various clocks and control signals are generated to control the sensor interface and SAR ADC circuits. After the ADC finishes data conversion, all the sampled data are written to the 11-bit registers and the implant device goes to *transmission* mode. All the sampled data are spread to seven chips and backscattered to the external device.

The block diagram of the implemented DBB is shown in Fig. 8. The inputs of the receiver are the 6.78-MHz clock and demodulated signal waveform. The signal waveform is first sampled and fed into the despreading circuit that is an M-sequence generator. After despreading, the parameters are obtained from the command, and the microsystem is configured according to the extracted parameters. In the transmitter, the ADC outputs are first spread using the M-sequence generator, and formatted as a frame by adding the SOF and EOF bits. The completed transmission frame is fed to the backscattering modulator circuit.

E. Sensor Interface and Data Conversion

The schematic diagram of the sensor interface and data conversion circuits is shown in Fig. 10 together with the timing diagram of the control and clock signals used. The sensor interface circuit consists of a current integrator and a single-ended-to-differential programmable gain amplifier. The circuit reads from two nanowire-based pressure sensors one after another by time-multiplexing. A wide range of sensor resistance can be covered by changing the integration time. In the single-ended-to-differential gain stage, the gain is controlled by programming C_1 that is a 3-bit capacitor bank. More detailed explanation of the sensor interface circuit can be found in [3].

For data conversion, a 10-bit 80-kS/s ADC is used. The SAR ADC was chosen among different types of ADCs due to its excellent power efficiency. In this design, a new common-mode-resetting trilevel switching scheme is used together with a generalized nonbinary redundant algorithm and a time-domain comparator to minimize the ADC power consumption. The ADC operation and used design techniques are explained in [11] in detail.



(a)

(b)

Fig. 10. (a) Schematic diagram of the sensor readout circuit chain consisting of a current integrator, a single-ended-to-differential programmable gain amplifier, and a trilevel-switching SAR ADC using generalized nonbinary redundant algorithm. (b) Timing diagram of the control signals for sensor readout circuit chain.

IV. Implementation, System Integration, and Characterization

The micrograph and SEM image of the fabricated sensor based on the SiNW and diaphragm structure are shown Fig. 3. The sensor was characterized using a pressure regulator and Agilent 4156 parameter analyzer. Fig. 11(a) shows the measured current change as a function of the applied strain with varying the gate voltage. From Fig. 11(b), it is found that the sensor provides a gauge factor higher than 300 when a small negative tuning voltage (-0.5–0 V) is applied. Based on the gauge factor and the current noise measured in [6], the sensing resolution is calculated to be 0.176 mmHg/$\sqrt{\text{Hz}}$.

The ASIC has been fabricated in 0.18-μm CMOS process and the chip micrograph is shown in Fig. 12. The total active area is 1.5 mm $\times$ 1.78 mm and the total power consumption is 21.6 μW. The passive sensing carrier frequency is 13.56 MHz as per design. The ASK modulation depth of the forward link is programmable from 10% to 90% in steps of 10%, while the LSK modulation depth of the back telemetry is programmable from 10% to 70% in four steps. The implemented communication protocol is the simplified version of ISO 14443 RFID standard. The efficiencies of the rectifier and LDO regulator are measured as 66% and 56%, respectively. The fabricated 10-bit 80-kS/s SAR ADC consumes only 400 nW while achieving a signal-to-noise-and-distortion ratio (SNDR) of 50 dB, equivalent to effective number of bits (ENOB) of 8 bits, at 80-kS/s conversion rate up to 20-kHz input. The figure of merit (FOM) is 19.5 fJ/conversion-step. The input-referred noise of the sensor interface circuit is measured to be negligible compared to the sensor noise. The measured ASIC performance is summarized in [3].

The bench-top prototype of the microsystem shown in Fig. 13 was implemented and characterized. This first prototype integrates one MEMS pressure sensor, one ASIC, and one implant coil, and operates in pressure sensing mode for ease of testing. The external reader module interfaces with LabVIEW to send the RF energy and command to the sensor microsystem. The energy coupled with at the implant coil is converted to dc energy to power the ASIC, and the command from the reader module is demodulated for the microsystem configuration. The clock is extracted from the incoming carrier to provide necessary clock and control signals to the sensor interface and SAR ADC circuits. The digitized sensor readout data are fed to the load modulator for backscattering.

The pressure sensing data measured at a distance of 20 mm wirelessly are shown in Fig. 13(a) together with the bench-top

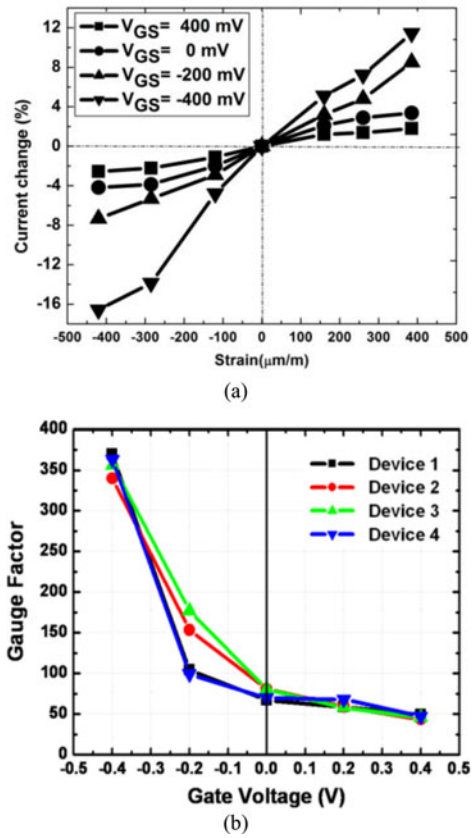


Fig. 11. (a) Current change versus strain characteristics measured with varying the gate voltage V_{GS}. (b) Gauge factor versus gate voltage characteristics measured from four different devices.

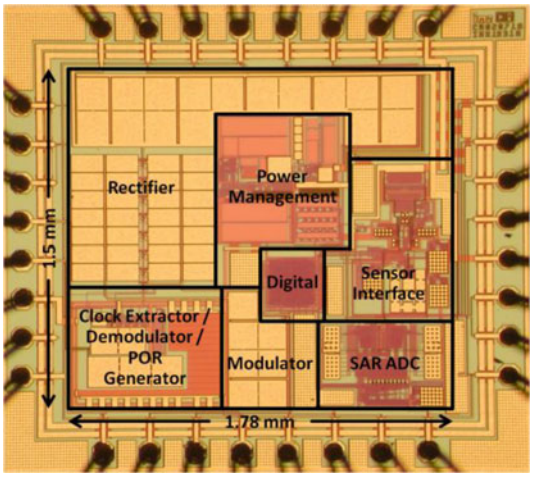


Fig. 12. Chip Micrograph of the ASIC.

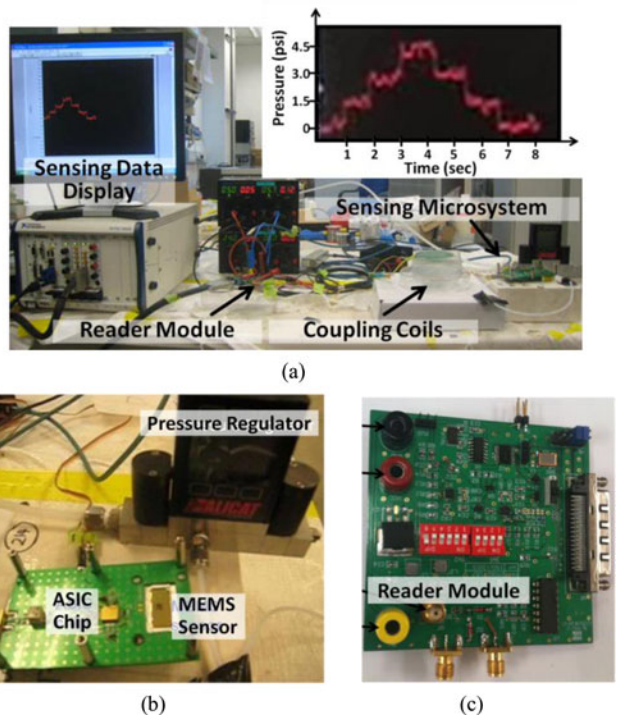


Fig. 13. (a) Bench-top measurement setup of the sensor microsystem prototype and the wirelessly measured pressure readout data. (b) Sensor microsystem prototype module. (c) External reader module.

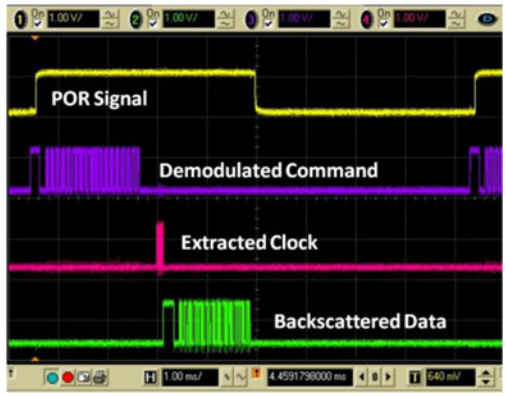


Fig. 14. Measured waveforms of the POR signal, demodulated command, extracted clock, and backscattered readout data.

test setup. The sensor microsystem and external reader modules are shown in Fig. 13(b) and (c), respectively. The measured waveforms of the POR signal, demodulated command, extracted clock, and backscattered readout data are shown in Fig. 14. Table I summarizes the measured performance of the sensor microsystem prototype and Table II shows the comparison with other published implantable pressure sensing microsystems. The presented microsystem is favorably compared with others by achieving good wireless sensing performance, small sensor size ,and low power consumption at the same time. The ASIC and sensor will be flip-chip bonded onto a flexible cable that will be embedded inside the PTFE graft. The coil with biocompatible coating will also be attached to the flexible cable and wrapped around the graft. One of the challenges is to integrate the entire system without altering the mechanical properties of the graft and affecting the normal implantation procedure.

TABLE I
MEASURED PERFORMANCE OF THE SENSOR MICROSYSTEM PROTOTYPE

Parameter	Measured Result
Carrier frequency	13.56 MHz
Communication protocol	Simplified version of ISO 14443 RFID standard
Forward command link modulation	ASK (programmable modulation depth from 10% to 90% in steps of10%)
Backward data link modulation	LSK (programmable modulation depth from 10% to 70% in four steps)
ASIC	Active area: 1.5 mm × 1.78 mm Power consumption: 21.6 μW (Rectifier: 5 μW; regulator: 12.8 μW; digital core: 2 μW; ADC: 0.4 μW; sensor interface: 1.4 μW)
Power conversion and regulation efficiency	Rectifier: 66% Regulator: 56%
SAR ADC	Resolution: 10 bits Sampling rate: 80 kS/s ENOB: 8.6 bits @ 5-kHz input 7.4 bits @ 25-kHz input INL/DNL: ±1.5 LSB / ±0.7 LSB FOM: 19.5 fJ/conversion-step
MEMS sensor	Diaphragm-based SiNW sensor Size: 0.064 mm^2 Sensing mechanism: piezoresistive Resolution: 0.176 mmHg/$\sqrt{\text{Hz}}$
Implant coil	Diameter: 6 mm Material: Nitinol

TABLE II
COMPARISON WITH OTHER IMPLANTABLE PRESSURE SENSING MICROSYSTEM

Parameter	This Work	[12]	[13]	[14]	[15]
Sensing Mechanism	Piezo-resistive	Capa-citive	Capa-citive	Capa-citive	Capa-citive
Resolution (mmHg)	0.176	3	3	0.1[b]	0.5
Bandwidth (Hz)	1	100	30	1,000[b]	N.A.
Sensor Size (mm^2)	0.064[a]	0.5	0.864	0.08	N.A.
Power/Data Carrier Frequency (Hz)	13.56M/ 13.56M	4M/ 4M	N.A.	4M/ 433M	3.65G/ 2.4G
IC Fabrication Process	0.18-μm CMOS	3-μm BiCMOS	N.A.	1.5-μm CMOS	0.13-μm CMOS
Power Consumption (μW)	21.6	340	N.A.	300	202.7[c]
Device Deployment	Vascular graft	Stent	Catheter	Cuff around vessel	Ocular implant

[a] Die area including both the sensor device and essential bonding pads.
[b] Only sensor interface IC noise taken into account. Sensor noise not included.
[c] Excluding the active wireless data transmitter power consumption.

V. CONCLUSION

A wireless implantable blood flow sensor microsystem for prosthetic vascular grafts is presented. The microsystem consists of diaphragm-based SiNW pressure sensors with tunable piezoresistivity, an ultralow-power CMOS ASIC, and miniature coupling coils. The power and command from the external unit are received and the digitized sensor readout data are backscattered through the coupling coils at 13.56-MHz carrier frequency.

The MEMS pressure sensors provide a high sensitivity (gauge factor >300) with the application of a small negative tuning voltage (>−0.5 V). The ASIC includes a complete set of necessary electronics for sensor interface, data conversion, digital control, power management, wireless powering, and bidirectional telemetry. The ASIC occupies an active area of 1.5 × 1.78 mm^2 and consumes 21.6 μW, when fabricated in 0.18-μm CMOS process. The fabricated pressure sensor and ASIC have demonstrated 0.176 mmHg/$\sqrt{\text{Hz}}$ sensing resolution. The implant coil is made of Nitinol with biocompatibile coating and wrapped around an implant PTFE graft with a diameter of 6 mm. The bench-top prototype of the microsystem has been implemented and demonstrated successfully, operating together with the external reader module and coupling coil.

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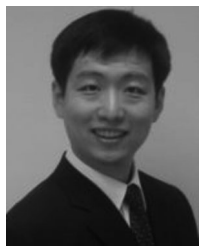
Andreas Astuti Lee, photograph and biography not available at the time of publication.



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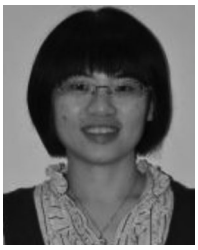

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