A CMOS Rectifier With a Cross-Coupled Latched Comparator for Wireless Power Transfer in Biomedical Applications

Hyouk-Kyu Cha, *Member, IEEE*, Woo-Tae Park, *Member, IEEE*, and Minkyu Je, *Member, IEEE*

***Abstract*—A highly efficient rectifier for wireless power transfer in biomedical implant applications is implemented using 0.18-μm CMOS technology. The proposed rectifier with active nMOS and pMOS diodes employs a four-input common-gate-type capacitively cross-coupled latched comparator to control the reverse leakage current in order to maximize the power conversion efficiency (PCE) of the rectifier. The designed rectifier achieves a maximum measured PCE of 81.9% at 13.56 MHz under conditions of a low 1.5-V_{pp} RF input signal with a 1-kΩ output load resistance and occupies 0.009 mm^2 of core die area.**

***Index Terms*—Biomedical implant devices, CMOS rectifier, cross-coupled latched comparator, wireless power transfer.**

I. Introduction

In RECENT years, research in the field of implantable biomedical devices has been extensively carried out for a wide range of applications such as neural recording [1], retinal prosthesis [2], and blood flow sensing [3].

One of the critical issues in the development of implantable biomedical devices is the consistent provision of a stable and reliable power supply. The usage of batteries must be avoided since it requires periodic replacement due to its limited lifetime and causes much discomfort and health risk to the patient with the implant device. Therefore, inductive links are widely utilized to transmit power to the implant device wirelessly. The efficiency of the wireless power transfer system must be maximized so that less transmitting power may be required and/or a longer distance between the external transmitting device and the implant device can be facilitated while using the same transmitting power from the external device. In addition, the operating frequency for power transfer must be relatively high considering the size of the coil inductor in the implant, but it must also not be too high due to the increased tissue absorption. Within the wireless power transfer system, as shown in Fig. 1, the rectifier is utilized to convert the transmitted ac signal to an unregulated dc signal so that it can be applied to a low-dropout (LDO) regulator to obtain a stable dc voltage to supply it to the building blocks in the implant device. The total efficiency of the wireless power transfer system can be represented as

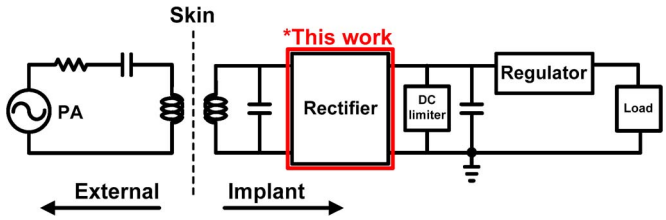

Fig. 1. Block diagram of a typical wireless power transfer system.

$$\eta_{\mathrm{Total}} = \eta_{\mathrm{PA}} \times \eta_{\mathrm{Coil}} \times \eta_{\mathrm{Rect}} \times \eta_{\mathrm{LDO}} \tag{1}$$

where η_{PA} represents the power amplifier efficiency, η_{Coil} is the inductive coil link efficiency, η_{Rect} is the efficiency of the rectifier, and η_{LDO} represents the LDO efficiency. The efficiency of the rectifier is usually the bottleneck on the implant side in achieving high overall transfer efficiency since the coil efficiency is limited due to the physical constraints of the implant coil, whereas high LDO efficiency can usually be achieved.

Among several choices for the rectifier, CMOS rectifiers have the advantage of its low-cost process and its compatibility with other building blocks in comparison to the Schottky diode rectifier [4], which requires additional process steps leading to an increase in the implementation cost. Moreover, the Schottky diode is not a readily available option in many CMOS fabrication processes.

In this brief, we present a highly efficient CMOS rectifier for wireless power transfer operating at an industrial, scientific, and medical band of 13.56 MHz in biomedical implant applications. nMOS and pMOS active diodes are used with a shared comparator to control both nMOS and pMOS switches. The proposed comparator is a common-gate cross-coupled latched comparator for fast output response time to maximize the forward current in the rectifier and minimize the reverse current leakage to ultimately achieve high power conversion efficiency (PCE) at a small input power. Section II briefly addresses the conventional CMOS rectifier topologies, whereas Section III describes the proposed circuit design in detail. Section IV

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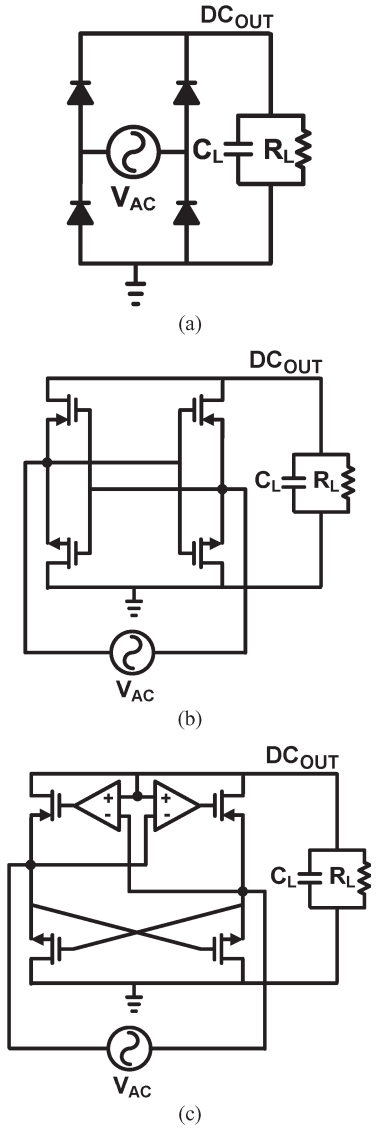

Fig. 2. Schematic of the conventional rectifiers. (a) Full-wave diode rectifier. (b) CMOS gate cross-coupled rectifier. (c) nMOS gate cross-coupled rectifier with active pMOS diode.

presents the experimental results followed by the conclusions in Section V.

II. Conventional CMOS Rectifiers

There are several types of CMOS rectifiers reported in previous publications. Fig. 2(a) is the well-known full-wave diode-bridge rectifier. Both Schottky and CMOS types can be used in this topology. As it operates as a full-wave rectifier, the corresponding diode pair turns on during each cycle, and the current flows to the output load. However, this topology has a limitation in achieving high PCE due to the two threshold voltage $V_{\rm TH}$ drops. Fig. 2(b) shows a CMOS gate cross-coupled rectifier [3], [5], [6]. The advantage of this topology is that it enables low ON-resistance in comparison to the diode-bridge structure and can achieve moderate efficiency at low input signals. However, whenever the potential in the output node is higher than the input signal, reverse leakage current results on every cycle of its operation if the input transistor is not turned OFF fast

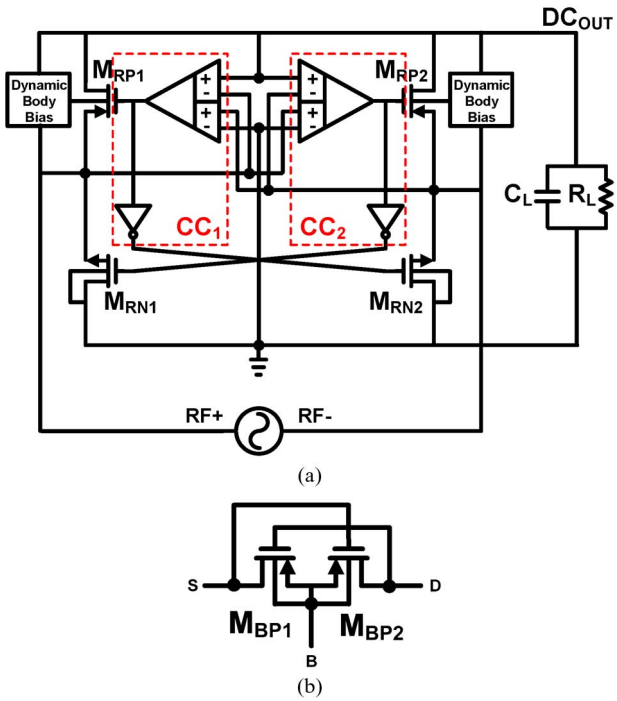

Fig. 3. (a) Schematic of the proposed rectifier with shared comparators. (b) Schematic of dynamic body bias circuit.

enough during the ON–OFF transition. This causes a severe degradation of the rectifier PCE. To alleviate this issue, several comparator-based rectifiers have been proposed [7]–[12]. As shown in Fig. 2(c), a comparator is used to drive the gate of the main transistor and control the operation in such a way that the forward current is maximized and, at the same time, the reverse leakage current is minimized. Many of these comparator-based works achieve a relatively high simulated/measured PCE of over 80%. However, these rectifiers operate at a very low frequency [7], require a large input signal to achieve such high PCEs [8]–[12], or some calibration control is needed to improve the efficiency [12]. Operation at a too low frequency leads to the poor overall link PCE due to the limited coil link efficiency when the coil size is restricted. The requirement of the large input signal for high efficiency limits the allowed operation distance of the rectifier. In addition, this may cause tissue damage/heating issues for implant applications.

III. Proposed CMOS Rectifier

A. Rectifier

Fig. 3(a) shows the proposed rectifier. The rectifier consists of active nMOS ($M_{\rm RN1}$ and $M_{\rm RN2}$) and pMOS ($M_{\rm RP1}$ and $M_{\rm RP2}$) diodes operating as switches, in which the gates are driven by shared self-dynamically-powered comparators ($\rm CC_1$ and $\rm CC_2$) that do not require fixed voltage supplies. In the positive cycle of the operation (when RF+ is high), the output of $\rm CC_1$ will go low to turn ON $M_{\rm RP1}$, and the inverted output of $\rm CC_1$ (after the inverter) will be high to turn ON $M_{\rm RN2}$. The current in the forward direction will flow to the load consisting of R_L and C_L to produce the rectified dc voltage. At this cycle, the output of $\rm CC_2$ will be the opposite to turn OFF both $M_{\rm RP2}$ and $M_{\rm RN1}$. In the negative input cycle, the rectifier will operate

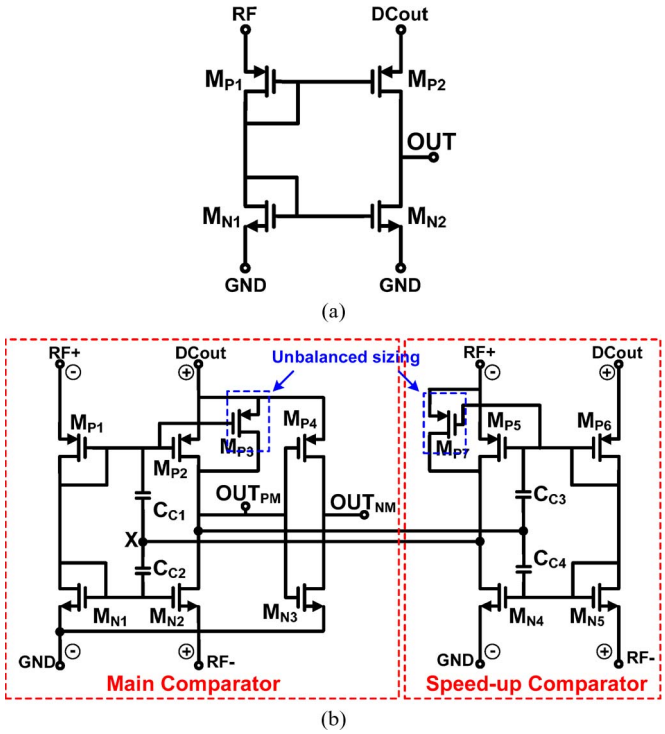

Fig. 4. (a) Simplified schematic of a conventional common-gate-type comparator. (b) Proposed four-input cross-coupled latched comparator.

similarly with M_{RP2} and M_{RN1} with CC_2. However, during its operation, if the output dc voltage is higher than the input ac voltage while the transition (switching time of the pMOS switches M_{RP1} and M_{RP2} and nMOS switches M_{RN1} and M_{RN2}) from one cycle to the next cycle is not fast enough, this will result in a reverse leakage current flowing out from the output load, which will degrade the efficiency of the rectifier. The transition is decided by how fast the comparator operates, and therefore, a careful design of the comparator is critical in maximizing the efficiency of the rectifier.

The schematic of the dynamic body biasing [11] utilized in both the main rectifier and the comparator is depicted in Fig. 3(b). Two pMOS transistors, namely, M_{BP1} and M_{BP2}, are used to connect the substrate of M_{RP1} and M_{RP2} in the rectifier to a higher potential between RF + /RF− and DCout in order to avoid the latch-up of the device and prevent breakdown.

B. Comparator

In order to improve the efficiency of the rectifier, the conduction time of the active diodes in the rectifier in the positive cycle (when the load is being charged) must be maximized, whereas the reverse conduction time must be minimized. The simplified schematic of the conventional widely used common-gate-type comparator is shown in Fig. 4(a). The comparator compares the two inputs, i.e., RF and DCout, and the output will be "high" if the input RF signal is smaller than DCout, whereas it will be "low" if the RF signal is larger. Many of the previous comparator-based rectifiers [9]–[12] use this basic comparator topology or a slightly modified version of this.

The schematic of the proposed self-biased comparator for a fast ON–OFF output response is shown in Fig. 4(b). In this design, the comparator consists of two parts. The main comparator is a four-input common-gate type where the inputs are RF+, RF−, DCout, and GND. To explain the operation of the comparator, the case for the CC_1 comparator side in Fig. 3(a) will be used. When the ac voltage at RF+ is higher than the dc voltage at DCout, M_{P2} is turned off, whereas M_{N2} is turned ON, and the output node $\mathrm{OUT}_{\mathrm{PM}}$ is equal to RF−, which is low in this cycle, switching ON the pMOS M_{RP1} and nMOS M_{RN2} of the rectifier circuit in Fig. 3(a). When the voltage at RF+ is lower than the dc voltage at DCout, M_{P2} is turned ON, whereas M_{N2} is turned OFF, and the output node $\mathrm{OUT}_{\mathrm{PM}}$ is equal to DCout, turning OFF M_{RP1} and M_{RN2} of the rectifier circuit. An additional pMOS transistor M_{P3} is connected to M_{P2} for unbalanced sizing to slightly improve the pull-up response so that the reverse conduction time is minimized to reduce the leakage current.

In order to improve the output transient response of the comparator, a small speed-up comparator is connected to the main comparator, in a capacitively cross-coupled latched formation. A similar four-input common-gate topology is used with the inputs interchanged compared with the main comparator. When the voltage at RF+ is higher than the dc voltage at DCout, M_{P5} will turn ON, whereas M_{N4} is turned OFF, which will result in the node "X" being high, which helps the main comparator to turn ON M_{N2} harder and turn OFF M_{P2} during this operation cycle. A faster response in this cycle will increase the conduction time in the positive cycle so that more current flows into the output load. Likewise, when the voltage at RF+ is lower than the dc voltage at DCout, then M_{N4} will turn ON, whereas M_{P5} is turned OFF, and the node "X" will be shorted to ground, which will aid the main comparator to turn ON M_{P2} quicker, leading to a faster pull-up of $\mathrm{OUT}_{\mathrm{PM}}$ to DCout and helping to minimize the negative conduction time to reduce the reverse leakage current and ultimately improve the efficiency.

The transient simulation plot in Fig. 5 compares the rectifier with the proposed comparator and the rectifier with the conventional comparator, which does not have the cross-coupled latched speed-up comparator part. All the sizes of the transistors are identical for both cases in the main rectifier part. Fig. 5(a) shows the voltage response of the input and output of the comparator in the proposed and conventional cases, whereas Fig. 5(b) plots the current flow comparison. It is shown that the added cross-coupled latched comparator results in a much faster output response, which increases the forward current flowing into the load while minimizing the reverse leakage current, improving the simulated PCE of the rectifier from 72% to over 87% at 13.56 MHz when the input signal is 1.1–1.5 $\mathrm{V_{pp}}$ and the load is 1 kΩ.

IV. Experimental Results

The rectifier is fabricated in a one-poly six-metal (1P 6M) 0.18-μm CMOS process. The chip microphotograph is shown in Fig. 6, where the total chip area of the core is 0.009 mm^2. The rectifier input is placed as close as possible to the pads in order to minimize the on-chip parasitic resistive loss that degrades the efficiency. The die is housed in a quad flat nonleaded (QFN16) package for measurement on an FR4 PCB. The default

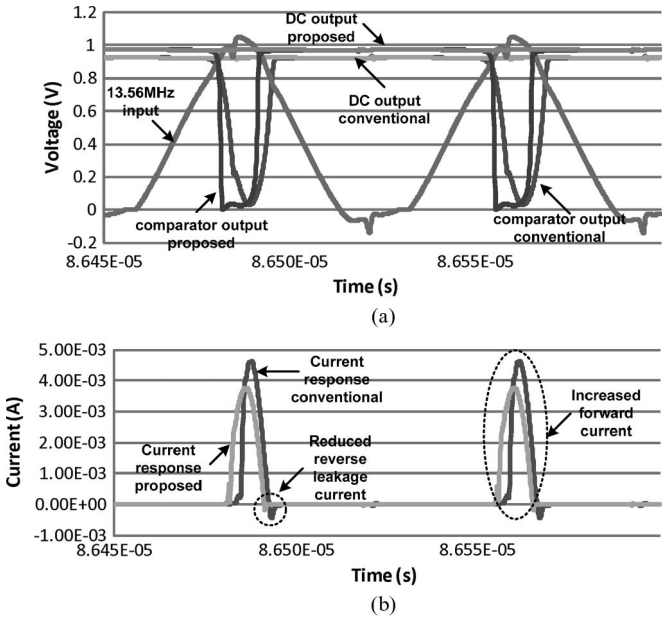

Fig. 5. Transient simulation plot of the rectifier with the conventional and proposed comparator. (a) Voltage response. (b) Current response.

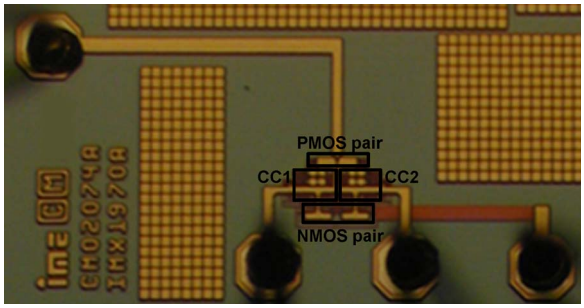

Fig. 6. Chip microphotograph of the implemented rectifier.

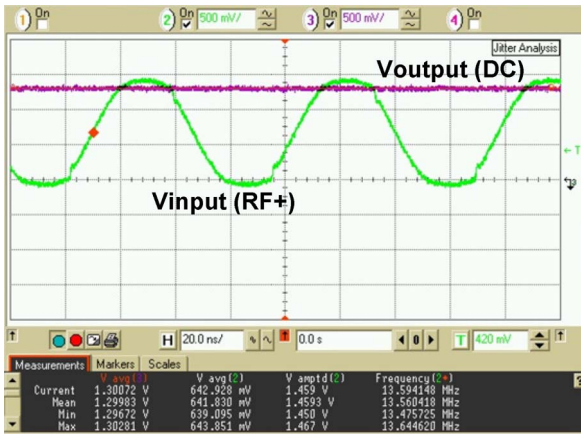

Fig. 7. Measurement plot capture of the probed output dc voltage and the input ac voltage at 13.56-MHz input frequency with 1-kΩ R_L.

measurements are carried out at 13.56-MHz input frequency with an output load of 1-kΩ resistor and 10-μF capacitor. Fig. 7 shows the measurement plot capture where a rectified dc output of 1.3 V is achieved with an input ac voltage of 1.46 V_{pp}. The measured voltage conversion efficiency (VCE) and rectified output dc voltage versus input ac voltage is shown

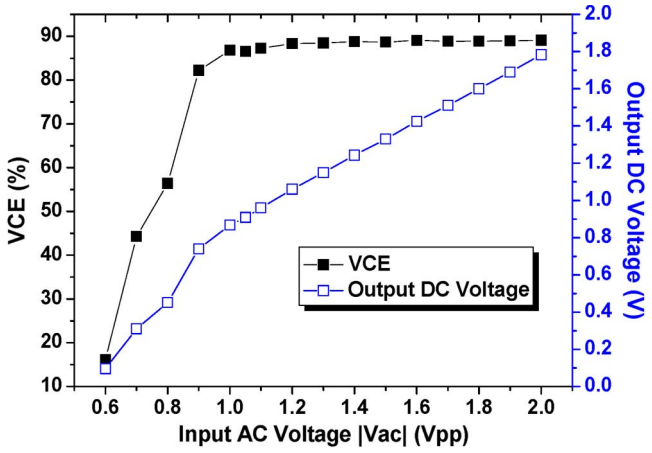

Fig. 8. Measured output dc voltage and VCE versus input voltage at 13.56-MHz input frequency and 1-kΩ R_L.

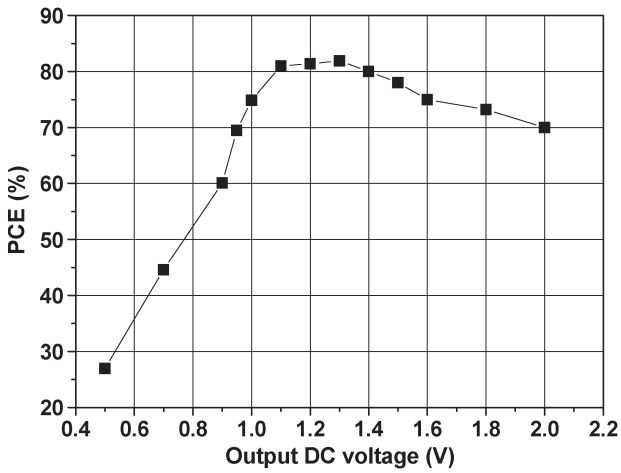

Fig. 9. Measured PCE versus output voltage at 13.56-MHz input frequency and 1-kΩ R_L.

in Fig. 8. A maximum VCE of 89% is measured. The VCE in this measurement is defined as

$$\eta_{\text{Voltage}} = \frac{V_{\text{out\_dc}}}{|V_{\text{in\_ac}}|} \tag{2}$$

while PCE is defined as

$$\eta_{\text{Power}} = \frac{P_{\text{out\_dc}}}{P_{\text{in\_ac}}}. \tag{3}$$

In order to measure the input current, a small series resistor is placed at the input of the rectifier on the PCB, and the voltage across it is measured by using an active probe to calculate the current. The input power is then calculated by taking the average of the product of the input current and voltage over several measured period cycles. The output power is calculated by measuring the average output dc voltage and dividing the square of this value by the load resistor. A peak measured PCE of 81.9% is achieved at an output dc voltage of 1.3 V, as shown in Fig. 9. The operation of the self-biased comparator starts up at the input of around 0.9–1 V_{pp}, which results in an abrupt increase in the output voltage, VCE, and PCE. After the start-up

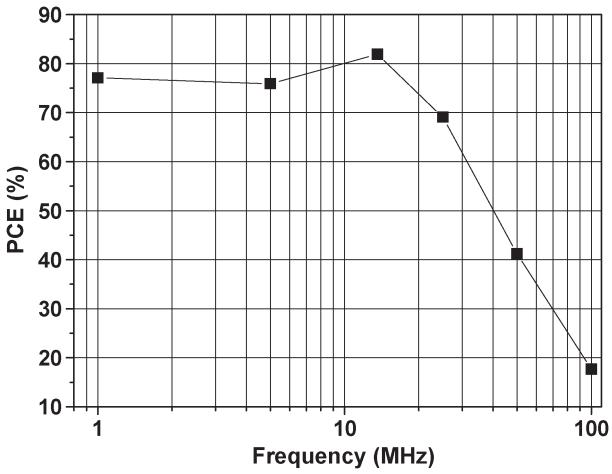

Fig. 10. Measured PCE versus variation in input frequency with 1-kΩ R_L.

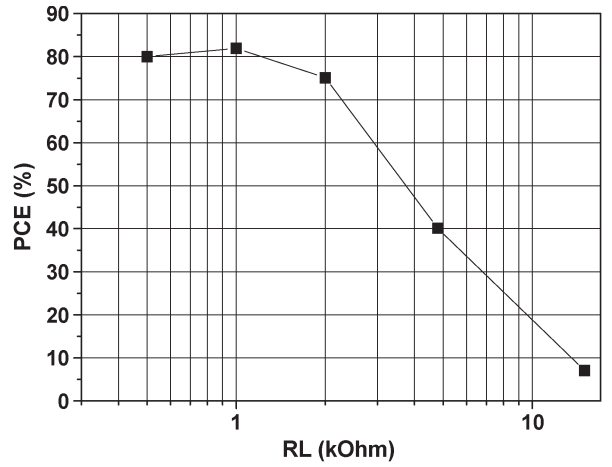

Fig. 11. Measured PCE versus variation in R_L at 13.56-MHz input frequency.

of the comparator, the output dc voltage increases quite linearly according to the increase in the input voltage.

The PCE dependence on input frequency is presented in Fig. 10 when the output dc voltage is at 1.3 V. As the input frequency increases, the PCE decreases mainly due to the speed limitation of the comparator. The measured output load dependence of PCE is plotted in Fig. 11 at 13.56-MHz input frequency when the output dc voltage is at 1.3 V. The difference in the peak PCE depending on the variation of the load resistance is because of the difference in the optimal rectifier transistor size depending on the output loading condition. Hence, the rectifier transistor size has to be optimized considering the required power delivery condition. The rectifier performance is summarized in Table I and compared with previously reported comparator-based CMOS rectifiers. The proposed rectifier shows favorable performance, in which the highest PCE is measured at 13.56-MHz input frequency due to our proposed comparator without any offset calibration.

V. Conclusion

A highly efficient rectifier for wireless power transfer in biomedical applications is implemented using a 0.18-μm CMOS process. The proposed rectifier consists of active nMOS and pMOS diodes with a cross-coupled latched comparator to maximize the PCE. An 81.9% maximum PCE is achieved at 13.56 MHz under conditions of a low 1.5-V_{pp} RF input signal with a 1-kΩ output load resistance.

TABLE I
Comparator-Based CMOS Rectifier Benchmark

Parameter	[7]	[8]	[9]	[12]	This work
Freq. (MHz)	0.2-1.5	0.125-1	13.56	13.56	13.56
Process	0.35μm CMOS	0.5μm CMOS	0.35μm CMOS	0.5μm CMOS	0.18μm CMOS
|Vtp|/Vtn (V)	0.82/ 0.69	N/A	0.73/ 0.55	0.92/ 0.78	0.49/ 0.42
Input Amplitude (|Vac|)	2.4	5	3.5	3.8	1.5
Output DC (V)	2.28	4.36	3.2	3.12	1.33
R load (kΩ)	2	1	1.8	0.1	1
Max.VCE (%)	95	87	92	82	89
Max.PCE (%)	87 (sim.)	84.8	87 (sim.)	80.2	81.9
Area (mm^2)	0.4	0.4	0.0055	0.18	0.009

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