A Low-Power Video Recording System With Multiple Operation Modes for H.264 and Light-Weight Compression

Hyun Kim, Chae Eun Rhee, and Hyuk-Jae Lee

***Abstract*—An increasing demand for mobile video recording systems makes it important to reduce power consumption and to increase battery lifetime. The H.264/AVC compression is widely used for many video recording systems because of its high compression efficiency; however, the complex coding structure of H.264/AVC compression requires large power consumption. A light-weight video compression (LWC), based on discrete wavelet transform and set partitioning in hierarchical trees, consumes less power than H.264/AVC compression thanks to its relatively simple coding structure, although its compression efficiency is lower than that of H.264/AVC compression. This paper proposes a low-power video recording system that combines both the H.264/AVC encoder with high compression efficiency and LWC with low power consumption. The LWC is used to compress video data for temporal storage while the H.264/AVC encoder is used for permanent storage of data when some events are detected. For further power reduction, a down-sampling operation is utilized for permanent data storage. For an effective use of the two compressions with the down-sampling operation, an appropriate scheme is selected according to the proportion of long-term to short-term storage and the target bitrate. The proposed system reduces power consumption by up to 72.5% compared to that in a conventional video recording system.**

***Index Terms*—Down-sampling, H.264/AVC compression, light-weight compression (LWC), low power implementation, multi operation modes, multi video codec, video recording system (VRS).**

I. Introduction

A VIDEO recording system (VRS) receives input videos from a camera and stores them in a memory when an important event takes place. The demand for mobile VRSs such as eye glasses, car black boxes, surveillance cameras or badge cameras is increasing due to recent trends. With an increased use of unmanned vehicles such as drones, which by necessity would use a VRS, the demand is expected to increase further in the future. Typically, a VRS operates with a limited battery capacity. Thus, the power consumption of a VRS should be maintained small in order to extend battery lifetime. In most VRSs, video compression is essentially used due to the limited memory capacity although it consumes a major portion of the available power in a VRS. Among various available compression formats, the H.264/AVC video compression standard proposed by the Joint Video Team [1] is widely used in a VRS due to its high compression efficiency [2]–[4].

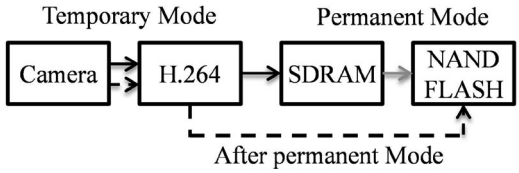

Fig. 1. Conventional VRS.

For storage space reduction in the VRS, a particular event (e.g., motion or impact) in video input data can be tested by various sensors (e.g., gyro-sensor, and passive infrared sensor), and the captured images are permanently stored in memory only when such an event is detected. The process from the camera input to permanent storage can be categorized as two modes: the temporary and permanent modes. In the temporary mode, the video data are stored temporarily in memory every time. In temporary storage, the video data are stored for a short time in a small memory space; moreover, the data that are turned out to be meaningless may be overwritten by incoming new video data. The permanent mode is activated when any event is detected by the sensor and the data stored in the temporary memory are regarded as important. In the permanent mode, the important data are compressed and moved to a different memory space for long-term storage. In case of the moving devices such as a car black box during driving, a badge camera and a drone, the permanent mode is frequently activated because image contents of video frames are continuously changing. In contrast, in case of the stationary devices such as a surveillance camera and a car black box in a parked car, the permanent mode is activated only when motion is detected. In the absence of motion, long-term storage is not necessary as the frames are unchanged; thus, the power consumption in the permanent mode is reduced by the detection.

A conventional VRS, which only uses an H.264/AVC encoder is shown in Fig. 1 [5], [6]. In the temporary mode of this system, an input video is continuously captured by the camera and compressed by the H.264/AVC encoder. The compressed video data are stored temporally in an SDRAM. This data flow

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is indicated by the black arrows in Fig. 1. If any event is detected by the sensor, the permanent mode is activated and the compressed data are moved from an SDRAM to a NAND flash memory for long-term storage. This flow is represented with a gray arrow in Fig. 1. In the conventional VRS, the flow of data in the temporary mode and the permanent mode are summarized as follows:

Temporary mode: Camera→H.264/AVC encoder→SDRAM
Permanent mode: SDRAM→NAND flash memory.

When meaningful events are detected, the video data after the events also need to be stored. Thus, once the permanent mode is activated, event-related video data after the activation of the permanent mode are compressed by the H.264/AVC encoder and stored in a NAND flash memory. This data flow is indicated by black-dashed arrow labeled "After permanent mode" in Fig. 1. However, compression and storage for the event-related video data are not considered in this paper because this operation has no difference for all VRSs.

The operation of a conventional VRS is inefficient in that H.264/AVC compression is used every time. Only meaningful video data are stored in long-term memory in the permanent mode, therefore, achieving high compression efficiency to minimize storage requirements is desirable. On the contrary, the high compression efficiency in the temporary mode is not required because the input video data which are unrelated to the event are stored temporarily and are eventually overwritten. Thus, the use of H.264/AVC compression may not be suitable for the temporary mode because H.264/AVC compression requires a large amount of computation; thus, it consumes a considerable amount of computational power. Furthermore, the operations required for inter-frame prediction in H.264/AVC compression frequently access external memory and result in a large amount of power consumption being used for memory access. Extensive researches have been conducted to develop an efficient VRS. However, these researches, solely employing the H.264/AVC compression, focused on achieving efficient video streaming [7], enhancing the detection and tracking for moving objects based on a spatio-temporal graph-based method [8], or improving the transcoding efficiency [9].

This paper concentrates on the video compression module and proposes a low-power VRS that incorporates multiple video compression modules and selects an appropriate compression module for use in the temporary and permanent modes that will improve upon the inefficient structure in a conventional VRS. To that end, the proposed VRS utilizes the widely used H.264/AVC compression in conjunction with a light-weight compression (LWC) which offers low power consumption. It should be noted that the LWC is not a standard acronym, but the term is used in this paper to represent a compression method which requires relatively low complexity compared to the high efficiency video compression standard with the high computation complexity such as H.264 or high efficiency video coding (HEVC) standard [10]. In the proposed VRS, the LWC is used in the temporary mode. The LWC can compress an image with lower power consumption than that by H.264/AVC compression due to the small computational complexity of the LWC, although it has lower compression efficiency than that of H.264/AVC compression. As power consumption is more important than compression efficiency in the temporary mode (a mode in which video data are stored temporarily), the use of the LWC is more suitable than the use of a H.264/AVC encoder. The temporary data which are compressed by the LWC encoder in the temporary mode are recompressed by the H.264/AVC encoder in order to accomplish the high compression ratio and video compression standard format for long-term storage in the permanent mode.

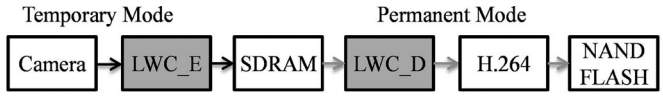

Fig. 2. Proposed LWC-based VRS.

The proposed VRS may have two disadvantages. First, the image quality may be degraded as a result of using two compressions. The LWC encoder degrades image quality once and then the H.264/AVC encoder causes an additional quality degradation. Second, the proposed VRS may achieve little power saving compared to the conventional VRS when the proportion of the temporary modes that turn into the permanent modes is significantly high. In the permanent mode, the power consumption in the proposed VRS is greater than that in the conventional VRS by decoding the short-term data and recompressing them through an H.264/AVC encoder. Thus, the proposed VRS consumes similar power with the conventional VRS if most temporary modes are being changed to permanent modes.

In order to avoid the disadvantages of the proposed VRS and to achieve further power reduction with a minimal quality degradation, this paper proposes a down-sampling operation in the permanent mode. The proposed VRSs are implemented on the integrated hardware platform. Furthermore, a selection scheme is proposed to determine optimal operation option that achieves the best trade-off between power consumption and quality degradation depending on the frequency of the permanent mode and the target bitrate. When the integrated VRS operates with the optimal selection scheme, the power consumption is reduced by up to 72.5% from that in a conventional VRS.

The rest of this paper is organized as follows. In Section II, two types of VRS that use the LWC and the down-sampling are proposed. Section III presents an algorithm for selection of the appropriate VRS according to the goal and requirement of the system. In Section IV, an integrated VRS is presented and the power consumption of the proposed VRS is estimated and compared to that in the conventional VRS. Section V concludes the paper.

II. A Low-Power VRS

A. LWC-Based VRS

Fig. 2 shows the proposed LWC-based VRS (LWC VRS). In that system, LWC encoder (LWC_E) and LWC decoder (LWC_D) modules are added to the conventional VRS shown in Fig. 1. These modules are represented by a gray box in Fig. 2. Like a conventional VRS, in the temporary mode of the LWC VRS, the video input data captured by the camera are

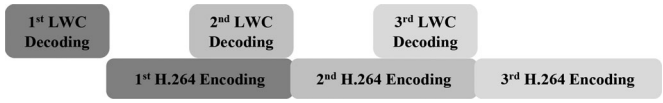

Fig. 3. Pipelined manner in the LWC-based VRS.

compressed by the LWC_E and temporarily stored in an SDRAM. When any temporary data are determined to be meaningful data that need to be stored for a long time, the system enters in the permanent mode. The temporary video data are decoded by the LWC_D and then recompressed by the H.264/AVC encoder.

There are two main reasons that the data already encoded by the LWC_E should be recompressed by the H.264/AVC encoder. First, the size of the temporary data is too large to be stored permanently due to the low compression ratio of the LWC_E. Second, the stream encoded by the LWC_E cannot be decoded and displayed by another device unless it has an exactly same LWC_D that is used in this system because the LWC is not video compression standard. The stream recompressed by the H.264/AVC video compression standard is stored in a NAND flash memory for long-term storage. Therefore, the video indexing or searching which is performed within the long-term memory can be applied in the same manner to the conventional system. In order to prevent extra latency by additional LWC decoding in the permanent mode, the LWC decoder and the H.264/AVC encoder are processed in a pipelined manner as shown in Fig. 3. Therefore, the latency is incurred only in the first stage of the pipeline. In a single HD (1280×720) frame, this initial latency is 0.009% of total cycles which are required for processing a single HD frame by the H.264/AVC encoder. In summary, the operations in the proposed LWC VRS are summarized as follows:

Temporary mode: Camera → LWC encoder → SDRAM
Permanent mode: SDRAM → LWC decoder → H.264/AVC encoder → NAND flash memory.

The proposed LWC VRS can operate with lower power consumption than a conventional VRS does because the trade-off between power consumption and compression efficiency is controlled by each mode (i.e., temporary mode or permanent mode) according to the importance of the data. In the permanent mode where an event is determined to be meaningful, high compression efficiency is more important than low power consumption in order to store as much data as possible in the limited storage space. In contrast, in the temporary mode, low power consumption takes precedence over compression efficiency because the video data are stored temporarily and are overwritten continuously. Thus, using LWC_E instead of the H.264/AVC encoder for compression of the meaningless events reduces the power consumption in the temporary mode. For the LWC in this study, discrete wavelet transform (DWT) coefficients that achieve high compression efficiency with low computational complexity are compressed by a set partitioning in hierarchical trees (SPIHT) [11]. In many compression methods such as the JPEG2000 standard, DWT coefficients are widely used to compress the image data [12]. In this paper, 1-D 3-level synthesis lifting DWT with integer Le Gall 5/3 filter is implemented for using the LWC [13]. A SPIHT compresses these DWT coefficients with low computation complexity.

There are two main reasons that the 1-D DWT + SPIHT are utilized for the LWC instead of the combination of discrete cosine transform (DCT) and context adaptive variable length coding (CAVLC) which exists in the H.264/AVC encoder. First, the existing DCT and CAVLC cannot be shared by the H.264/AVC encoder and the LWC module because the LWC encoder is always turned on for the temporary mode, whereas the LWC decoder and the H.264/AVC encoder should be performed in a pipelined manner for the permanent mode as shown in Fig. 3. Therefore, the LWC module and the H.264/AVC encoder should operate in an independent manner. Second, the 1-D DWT + SPIHT allows the generation of the bitstream that exactly meets the target compression ratio. This property reduces the buffer size for constructing a 16×16 macroblock (MB) of the H.264/AVC encoder for the recompression because it facilitates to read the necessary data for the H.264/AVC encoder from the external memory.

There are three main reasons that a 1-D LWC operates with lower power consumption than that of a H.264/AVC encoder. First, the LWC operates in a 1-D manner, whereas H.264/AVC compression performs block-based processing and operates in a two-dimensional manner. The 1-D LWC processes the input data coming from the camera on-the-fly manner so that it requires only a small amount of temporary buffer and avoids storing the video input from the camera in an external memory. Second, the 1-D LWC has low computational complexity because it utilizes only 1-D DWT and SPIHT without the need for complex prediction, entropy coding, and de-blocking filtering. This results in low internal power consumption of the computational modules. Third, the 1-D LWC does not access external memory during compression, whereas the H.264/AVC encoder frequently accesses external memory during inter-prediction; thus, a large amount of external access power is consumed. For these reasons, the 1-D LWC is especially suitable for low power consumption. The power reduction by 1-D LWC becomes even large when the compression module with the high power consumption such as the HEVC encoder is utilized for the main compression scheme. It should be noted that various video compression standard can be used for the main compression scheme because the main compression module and 1-D LWC operate in an independent manner.

B. Additional Power Reduction With Down-Sampling

In order to overcome the disadvantage of the proposed VRS which are previously described in Section I and to avoid quality degradation while achieving an additional power reduction, the proposed LWC VRS introduces two additional modules, a low pass filter (LPF) and a down-sampler (denoted hereafter by LWC + DS VRS). The LPF and the down-sampler are added to Fig. 2 and are represented by gray boxes in Fig. 4. The output of DWT in the LWC module is processed by an LPF and then intensively compressed by a SPIHT. Among the various LPF

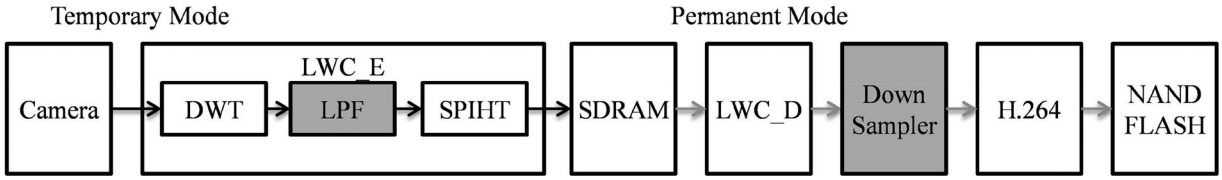

Fig. 4. Proposed LWC and down-sampling with LPF VRS.

algorithms, the method utilizing the DWT coefficients is selected to minimize hardware resource because a DWT module in the LWC VRS can be re-used. The video frames processed by an LPF can be easily scaled down by using down-sampling because these frames do not contain high frequency coefficients. Thus, the output of LWC_D is down-sampled prior to H.264/AVC compression. The down-sampling operation may significantly reduce the power consumption in the permanent mode. In the LWC VRS described in Section II-A, the power saving decreases as the proportion of the temporary modes that turn into permanent modes increases because LWC decoding and H.264/AVC recompression result in a large increase in the power consumption of the permanent mode. The use of LPF and down-sampling avoids this disadvantage. If down- sampling is applied before H.264/AVC recompression, the computational complexity and the external memory access for the video compression are reduced in proportion to the degree of down-scaling. Thus, both internal and external power consumptions for H.264/AVC recompression are reduced. Furthermore, the power consumption for long-term storage is also reduced because the down-sampled input to the H.264/AVC encoder generates a reduced bitstream. As a result, power consumption can be reduced even if most temporary modes are turned into permanent modes. This is because the proposed use of LPF and down-sampling with the LWC can reduce power consumption in both the temporary and permanent modes. In trading power consumption and R-D performance, both the frame width and frame height are decreased by half.

Extensive efforts have been made to develop a low-power H.264/AVC encoder. For example, simplified prediction schemes can reduce power consumption of an H.264/AVC encoder [14], [15]. However, the reducible range is limited for both internal and external power consumption. Adjusting a quantization parameter (QP) can reduce the generated stream size, much like that obtained from a down-sampling operation [16]. However, a QP change is not helpful when attempting to reduce internal and external power consumption. Thus, to reduce the internal power consumption, external power consumption, and output-stream size efficiently, the proposed down-sampling operation is suitable for a low-power VRS.

Even though the use of LWC and down-sampling with LPF markedly reduces power consumption, both schemes may cause a degradation in R-D performance. Fortunately, the degradation caused by both LWC and down-sampling with LPF is due to the loss of high frequency signals [17]. Thus, the losses from these two schemes overlap, and consequently, the amount of loss is limited. In contrast, the power savings derived from these two schemes are independent. The LWC reduces power consumption in the temporary mode and down-sampling with LPF reduces power consumption in the permanent mode. Therefore, a combined use of LWC and down-sampling with LPF is advantageous in the trade-off between the power consumption and R-D performance.

TABLE I
EXPERIMENT CONDITIONS FOR R-D ESTIMATION

Test Video Sequences	HD (1280 × 720) 90 Frames	Aspen Factory Pedestrian Area	Rush Hour Sunflower Tractor
H.264/AVC Encoding Configuration	Profile	Baseline	
	QP	20,24,28,32,36	
	Group of Pictures	IPPPP....	
LWC Compression Ratios		3/8, 1/4, 3/16	

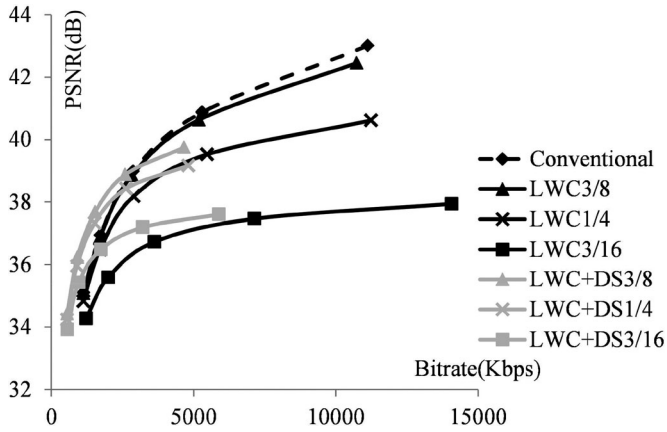

Fig. 5. Comparison of R-D performance for deciding the encoding condition.

C. Decision of Encoding Condition in the Proposed VRSs

This subsection presents the effect of the compression ratio of LWC on the R-D performance of the overall VRS. To this end, experiments are conducted to estimate the R-D performance with various compression ratios of LWC. Table I summarizes the running environment of the experiment which uses six HD video sequences with 90 frames in each sequence (see row 1 in Table I). The encoding configurations of the H.264/AVC encoder are presented in row 2 of Table I. For LWC, three compression ratios are used as shown in row 3.

Fig. 5 presents the R-D curves for the conventional, LWC, and LWC + DS VRSs obtained by using the encoding environment in Table I. The horizontal and vertical axises represent the bitrates and PSNRs, respectively. The dashed curve labeled

"Conventional" presents the results from the conventional VRS, which only uses H.264/AVC compression. The black curves labeled "LWC3/8," "LWC1/4," and "LWC3/16" denote the three compression ratios for the LWC in the LWC VRS, respectively. The LWC VRS results indicate that the R-D degradation is negligible compared to that in the conventional VRS at a LWC compression ratio of 3/8. The LWC compression ratios of 1/4 and 3/16 result in markedly degraded R-D performance. To achieve a moderate power saving with an insignificant R-D loss in the LWC VRS, a 3/8 LWC compression ratio is used. The gray curves labeled "LWC + DS3/8," "LWC + DS1/4," and "LWC + DS3/16" denote the three compression ratios used for the LWC with the additional operations of LPF and down-sampling. In this case, the R-D degradation for all three compression ratios is relatively large due to LPF and down-sampling operations. However, at very low bitrates, the R-D performance is better than that of the conventional VRS. The "LWC + DS3/8" and "LWC + DS1/4" show similar R-D performance levels, but the R-D performance for "LWC + DS3/16" is considerably degraded. The compression ratios that result in a remarkable R-D degradation are different in the LWC and LWC + DS VRSs because the down-sampling operation reduces the effect of the LWC on quality degradation. In this study, the proposed VRS which uses LPF and down-sampling with the LWC achieves a larger power saving than that from the LWC VRS even though the R-D performance is a little more degraded. Thus, it is more important to reduce the power consumed for temporary storage by selecting higher compression ratio. As a result, a 1/4 LWC compression ratio is used for the LWC + DS VRS. The power reductions of the proposed VRSs at the selected compression ratios are presented in Section IV-C.

III. Selection of an Appropriate Operating Condition

This section discusses a proper selection of the operating option of the proposed VRS. The selection should be made according to the use of the device and its system requirements by considering the trade-off between the power consumption and R-D performance.

The use of LPF + DS does not make much difference in power saving in the temporary mode, but, in the permanent mode, it significantly decreases the power consumption because it reduces the recompression power consumption of the H.264/AVC encoder by down-sampling. Although additional power for the down-sampling operation is needed, the power reduction in the H.264/AVC encoder is much larger thanks to the addition of the down-sampling operation. Therefore, the percentage of the temporary modes that are turned into the permanent modes (denoted hereafter by F_{RECORD}) has an important effect on the application of the LPF + DS. In moving devices such as an eyeglass camera, a car black box during driving, or a drone, F_{RECORD} is quite high because relatively many changes happen in the frame; thus, the power consumption in the permanent mode has a great effect on total power consumption. Therefore, the use of LPF + DS reduces power consumption in the permanent mode, leading to a moderate power saving even when F_{RECORD} is gradually increased. In stationary devices such as a surveillance camera or a black box in a parked car, relatively a small number of events may take place so that F_{RECORD} may be relatively small. Thus, power consumption in the temporary mode has a greater effect on the total power consumption than that in the permanent mode. In this case, the use of LPF + DS may not make a substantial decrease of power consumption even though it may cause an additional R-D loss in the permanent mode. Thus, the use of LPF + DS may not be beneficial for low F_{RECORD}. The above analysis shows that F_{RECORD} is a critical factor when deciding an appropriate operation condition.

The target bitrate also plays an important role when deciding the appropriate operation condition. The available bitrate varies according to the goal and requirement of the system. A relatively high bitrate can be acceptable when a memory space is sufficient, but a low bitrate should be used for a limited memory space. When the target bitrate is high, compression typically focuses on image quality so that relatively low QP values are used in H.264/AVC compression. The surveillance camera which operates at about 12 000 Kb/s is considered as a high bitrate application that focuses on the image quality. In this type of applications, the PSNR of the LWC + DS VRS is saturated and the image quality is not enhanced due to the R-D loss as a result of down-sampling. In contrast, the LWC VRS with a 3/8 compression ratio has good R-D performance that is similar to that in the conventional VRS and it also achieves power saving. When a memory space is insufficient or the output stream is immediately transmitted to a communication channel such as Wi-Fi wireless network, or universal serial bus, a low target bitrate is expected and relatively high QP values are used for H.264/AVC compression [18]. In Fig. 5, the left side of the horizontal axis represents the application at the low bitrates. The badge camera which operates at about 2000 Kb/s is considered as low bitrate applications. In this type of applications, the R-D gap between the LWC and LWC + DS becomes small as the bitrate decreases. In the very low bitrate range, the LWC + DS VRS offers the better R-D performance than both the conventional and LWC VRSs. This is because down-sampling is more efficient than adjusting QP at the very low bitrates [19]. Accordingly, the use of LPF + DS is beneficial for both image quality and power saving at the low bitrates. The above discussion shows that the target bitrate can also be a critical factor when selecting the appropriate operating condition of the proposed VRS.

Considering the factors explained above (i.e., user preference, F_{RECORD}, and target bitrate), a selection of the appropriate operating condition is proposed as shown in Fig. 6. If the user preference is chosen as "Quality Mode" (to ensure high image quality) in the first branch, the conventional VRS is selected. If the user preference is chosen as "Low-Power Mode" (to provide low power consumption), the appropriate VRS is selected according to F_{RECORD} and target bitrate characteristics. In the low-power mode, power saving has priority over image quality. In the second branch, if the target bitrate is smaller than a threshold bitrate (TH_B), the LWC + DS VRS utilizing the LPF + DS operations is selected because it shows both good power saving and good R-D performance at a low bitrate. Otherwise (i.e., when the target bitrate is high), the LPF + DS is not

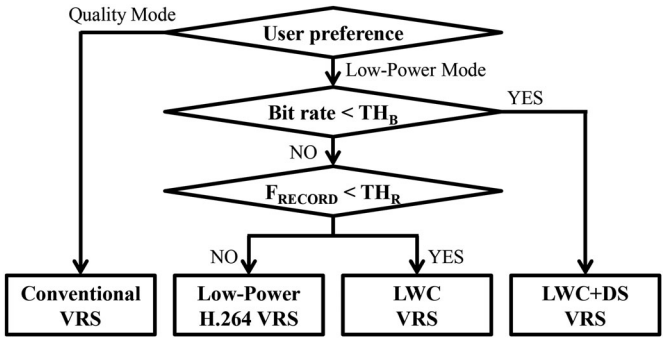

Fig. 6. Flow of selecting each VRS.

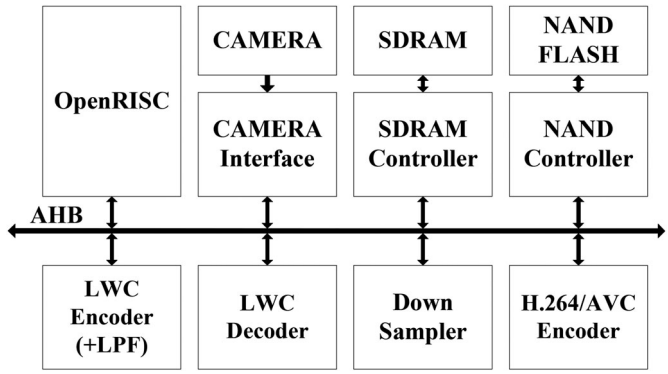

Fig. 7. Hardware structure of an integrated VRS.

very effective because it drops PSNR significantly even though it achieves considerable power savings and thus, F_{RECORD} value is checked in the third branch. If the current working condition F_{RECORD} value is smaller than a threshold F_{RECORD} (TH_R) value, the LWC VRS is selected. Note that the LWC VRS offers considerable power saving without LPF + DS operations at low F_{RECORD}. Otherwise (i.e., when F_{RECORD} is high), both the LWC VRS and LWC + DS VRS are unsuitable because the LWC VRS shows little power saving without LPF + DS operations at high F_{RECORD} and the LWC + DS VRS causes a significant quality degradation due to the saturation of the PSNR value at the high target bitrate. In this case, a VRS with the low-power H.264/AVC encoder which operates in the low complexity mode (denoted hereafter by low-power H.264 VRS) can be the best solution. In order to achieve the optimized power saving inside the H.264/AVC encoder, the low-power H.264 VRS is implemented based on the previous study where multiple power-scaling schemes are applied and the best combination of operation conditions is explored [20]. TH_B is chosen as 4000 Kb/s for the HD frame (The QP for the H.264/AVC encoder is 24), the bitrate that the PSNR value of the LWC + DS VRS is saturated, based on Fig. 5. TH_R is chosen as 50% by experimental results to achieve the best trade-off between the power consumption and the R-D performance in Section IV-E. The proposed selection algorithm provides various options for power saving which allow users to assess different VRS requirements and to find the best compression approach, considering both power saving and compression efficiency.

IV. Power Estimation of the Proposed VRSs

In this section, an integrated VRS is presented and the power saving obtained from the proposed integrated VRS is estimated and the effectiveness of the selection algorithm is evaluated.

A. Hardware Platform

The power consumption is estimated with the hardware platform for the implementation of an integrated VRS which is given in Fig. 7. The integrated VRS can support all VRSs (i.e., the conventional VRS, LWC VRS, LWC + DS VRS, and low-power H.264 VRS.) In this platform, an H.264/AVC encoder, a LWC encoder, a LWC decoder, and a down-sampler are implemented in Verilog independently and are connected to other devices through an advanced high-performance bus (AHB) architecture. A hardware-based real-time encoder [21] is used for H.264/AVC compression, whereas the combination of 1-D DWT and SPIHT [22] is utilized for the LWC encoder and decoder. Considering both power consumption and gate count, the down-sampler proposed by Joint Scalable Video Model reference software model [23] is simply designed to decrease both the frame width and frame height by half. A LPF is implemented inside the LWC encoder module. System configuration and control are processed by an OpenRISC processor [24]. The camera interface accepts video data from the camera and transmits the input data to each compression module. Two external memories (an SDRAM for temporary storage and a NAND flash memory for long-term storage) are supported. If a suitable VRS option is selected by OpenRISC, only necessary modules for the selected VRS are activated. The unused modules can be inactivated via clock-gating [25] or power gating [26] in order to minimize unnecessary power consumption.

B. Power Estimation Model

For estimation of the power consumption of the proposed VRS, the power consumption of every module (H.264/AVC encoder, LWC encoder, LWC decoder, down-sampler, SDRAM, and NAND flash memory) in the system is estimated by the proper design/simulation tools using the data from the precise hardware model. Note that the operation of the LPF is very simple because it is included in the operation of LWC; thus, the power consumption of the LPF is negligible. Let P_{264}, P_{LWCE}, P_{LWCD}, P_{DOWN}, P_{SDRAM}, and P_{FLASH} denote the power consumptions by the H.264/AVC encoder, the LWC encoder, the LWC decoder, the down-sampler, the SDRAM, and the NAND flash memory, respectively. Then, the total power consumption is formulated as follows:

$$P_{MODE} = P_{264} + P_{LWCE} + P_{LWCD} + P_{DOWN} + P_{SDRAM} + P_{FLASH} \quad (1)$$

where P_{MODE} represents the power consumption of either the temporary mode or the permanent mode. The power consumption for the event detection is excluded in the total power consumption because all VRSs use the event detection in the same manner and the power consumption for the event detection is also same. For the estimation of logic circuits, P_{264}, P_{LWCE}, P_{LWCD}, and P_{DOWN} are obtained with post-layout simulation

TABLE II
POWER CONSUMPTION BY HARDWARE MODULE

	P_{264}	P_{LWCE}	P_{LWCD}	P_{DOWN}
Power (mW)	97.88	10.89	15.36	13.64

TABLE III
EXTERNAL BANDWIDTH FOR EACH COMPRESSION TYPE

	H.264/AVC	LWC	LWC + DS
Compression ratio	1/100	3/8	1/4
One pixel size (bits)	12	16	16
Out stream size per second (Mbits)	3.24	162	108
Memory write per second (Mbits)	648	0	0
Memory read per second (Mbits)	972	0	0

using the netlist synthesized by Synopsys Design Compiler targeting a 0.13 μm process technology. These results are presented in Table II. The operating clock frequency is 162 MHz, which was selected to ensure that the frame-per-second rate is 30 for a HD size video for H.264/AVC encoder [21].

In order to estimate the power consumption for the external memory access, the number of memory accesses and the necessary memory size are simulated by ModelSim, an HDL simulation environment by Mentor Graphics. In Table III, the memory access information for the H.264/AVC encoder, the LWC encoder and the LWC decoder is presented. The second and third rows of Table III present the applied compression ratio and bits per pixel, respectively. The fourth row (Out-stream size per second) presents the generated bit size according to the compression ratio in each compression, whereas "Memory write per second" and "Memory read per second" in the fifth and sixth rows denote the SDRAM sizes for write and read accesses, respectively, when performing each compression. From Table III, the power consumption by SDRAM is derived by using the power calculator provided by Micron[1] whereas the power consumption for the NAND flash memory access is calculated by using the results presented in a previous study [27]; results that present the energy consumption for the program, erase, and read operations for one bit.

C. Power Estimation for the Temporary and Permanent Modes

In this section, the power consumptions for the temporary and permanent modes by the conventional VRS, the proposed VRSs, and the low-power H.264 VRS are estimated, and the results are summarized in Table IV. From the third to the eighth columns in Table IV, the power consumptions by individual modules and external memories are presented. The P_{SDRAM} and P_{FLASH} in the seventh and eighth columns are calculated by using an average out-stream size because the out-stream size differs according to the test sequence and the QP value. The P_{SDRAM} also includes the SDRAM accesses in H.264/AVC compression. For these estimates, the experiment conditions in Table I are used. The ninth column in Table IV presents the total power consumption of all modules (P_{MODE}), whereas the tenth column presents the power saving (P_{SAVING}) of the proposed VRSs compared to the power consumed by the conventional VRS. The power consumption in the temporary and permanent modes by the conventional VRS is given in the second and third rows of Table IV, respectively. It should be noted that the conventional VRS is a sub-part of the integrated hardware platform presented in Fig. 7 without the LWC encoder/decoder and the down-sampler. Therefore, the estimation of the conventional VRS is performed by eliminating the LWC encoder/decoder and the down-sampler hardware logics from the integrated hardware platform in Fig. 7. This allows fair comparison because the same conditions such as the semiconductor technology and experimental environment are used for both the conventional and proposed VRSs. In the temporary mode of the conventional VRS, only the H.264/AVC encoder and the SDRAM consume power, while the other modules remain idle. The idle modules are inactivated via the power gating [26]; thus the power consumptions in these modules are negligible. In the permanent mode of the conventional VRS, the power consumption is estimated for the data moving from SDRAM to NAND flash memory.

The fourth and fifth rows denoted by LWC VRS present the power consumption without LPF + DS operations. The fourth row shows the consumption in the temporary mode, in which only the LWC encoder and the SDRAM consume power. The fifth row shows the power consumption in the permanent mode in which the H.264/AVC encoder, the LWC decoder, the SDRAM, and the NAND flash memory consume power. When compared to the conventional VRS, the power consumption in the temporary mode is significantly reduced by 239.34 mW because the H.264/AVC encoder does not operate; thus, both internal and external power consumptions by the H.264/AVC encoder are reduced. In contrast, the power consumption in the permanent mode is increased by 236.8 mW because recompression via the H.264/AVC encoder is required in addition to LWC decompression. Although H.264/AVC encoding is performed in the temporary mode of the conventional VRS and in the permanent mode of the LWC VRS, the P_{SDRAM} values for those two encoding operations are different. That difference is because the external memory accesses to store and read an input frame for the H.264/AVC encoder are much smaller in the permanent mode of LWC VRS than in the temporary mode of the conventional VRS. In other words, in the permanent mode of LWC VRS, the input frame used for the H.264/AVC encoder is already stored in the SDRAM via LWC compression, thus the frame data size is much smaller. Therefore, it has an advantage as a frame memory compression is applied [28]. However, in the LWC VRS, the compression ratio of the LWC encoder is lower than that of the H.264/AVC encoder; consequently, more SDRAM space is required for temporary storage. An increased SDRAM size results in additional power consumption for the refresh and activation operations. Consequently, power consumption of the permanent mode in the LWC VRS is a little smaller than that of the temporary mode in the conventional VRS.

The sixth and seventh rows of Table IV denoted by LWC + DS VRS show the power consumption of the proposed VRS with LPF + DS operations. The sixth row shows the power consumption in the temporary mode, in which only the LWC encoder and the SDRAM consume power. The difference of

[1]Micron SDRAM Calculator.

TABLE IV
POWER CONSUMPTION OF EACH MODE FOR EACH VRS

Video Recording Systems	Mode	P_{264} (mW)	P_{LWCE} (mW)	P_{LWCD} (mW)	P_{DOWN} (mW)	P_{SDRAM} (mW)	P_{NAND} (mW)	P_{MODE} (mW)	P_{SAVING} (mW)
Conventional VRS	Temporary	97.88				236.34		334.22	–
	Permanent					65.83	5.72	71.55	–
LWC VRS	Temporary		10.89			83.99		94.88	239.34
	Permanent	97.88		15.36		189.54	5.57	308.35	−236.8
LWC + DS VRS	Temporary		10.89			81.07		91.96	242.26
	Permanent	24.47		15.36	13.64	107.4	4.71	165.58	−94.03
Low-power H.264 VRS	Temporary	60.94				165.23		226.17	108.05
	Permanent					65.88	6.72	72.6	−1.05

P_{SDRAM} between the LWC VRS and LWC + DS VRS is the result of their different compression ratios. As shown in Table III, LWC and LWC + DS use 3/8 and 1/4 compression ratios, respectively, for temporary storage; consequently, the data sizes needed for short-term storage are different. The seventh row of Table IV shows the power consumption in the permanent mode by the H.264/AVC encoder, the LWC decoder, the down-sampler, the SDRAM, and the NAND flash memory. When compared to the LWC VRS power consuming modules, additional power is consumed by the down-sampler module. However, the power consumptions for the H.264/AVC encoder and the SDRAM are reduced to about one quarter because the video frame size is scaled down to one quarter. As a result, the computation complexity, external memory accesses, and out-stream size are decreased in proportion to the rate of down-scaling. The power consumption in the temporary mode is significantly reduced by 242.26 mW compared to the conventional VRS. Although the power consumption in the permanent mode is increased by 94.03 mW due to recompression, the increase in power consumption is substantially reduced compared to that in the LWC VRS without LPF + DS operations.

The eighth and ninth rows of Table IV show the power consumption of the low-power H.264 VRS. The power consumption of the temporary mode in the eighth row is reduced by 108.05 mW compared to the conventional VRS due to simplified complexity; whereas the power consumption of the permanent mode in the ninth row is similar with that in the third row because the operations of the conventional VRS and the low-power H.264 VRS are almost the same.

D. Total Power Consumption According to F_{RECORD}

In Section IV-C, the power consumptions in the temporary and permanent modes are estimated independently. However, for an evenhanded comparison of the proposed VRS, the power consumptions in the two modes need to be combined. Recall that the permanent mode is activated only when short-term storage is changed to long-term storage. Thus, F_{RECORD} needs to be included in the calculation of total power consumption. The total power consumption, P_{TOTAL}, is formulated as follows:

$$P_{TOTAL} = P_{TEMPORARY} + P_{PERMANENT} \times F_{RECORD} \quad (2)$$

where $P_{TEMPORARY}$ and $P_{PERMANENT}$ denote the power consumption in the temporary and permanent modes, respectively. Each VRS has different $P_{TEMPORARY}$ and $P_{PERMANENT}$ values. Recall that F_{RECORD} is highly affected by the use of device and the system requirements as well as by the video sequence and event detection algorithm. To allow consideration of all possibilities, in this study, the percentages of F_{RECORD} ranged from 0% to 100%.

TABLE V
POWER CHANGES ACCORDING TO CHANGES IN F_{RECORD}

F_{RECORD} (%)	Power Consumption (mW)				Power Gain (%)		
	Conventional	LWC	LWC + DS	LP H.264	LWC	LWC + DS	LP H.264
0	334.2	94.9	92.0	226.2	71.6	72.5	32.3
5	337.8	110.3	100.2	229.8	67.3	70.3	32.0
10	341.4	125.7	108.5	233.4	63.2	68.2	31.6
20	348.5	156.6	125.1	240.7	55.1	64.1	30.9
25	352.1	172.0	133.4	244.3	51.2	62.1	30.6
30	355.7	187.4	141.6	248.0	47.3	60.2	30.3
40	362.8	218.2	158.2	255.2	39.9	56.4	29.7
50	370.0	249.1	174.8	262.5	32.7	52.8	29.1
60	377.2	279.9	191.3	269.7	25.8	49.3	28.5
70	384.3	310.7	207.9	277.0	19.1	45.9	27.9
75	387.9	326.1	216.1	280.6	15.9	44.3	27.7
80	391.5	341.6	224.4	284.3	12.7	42.7	27.4
90	398.6	372.4	241.0	291.5	6.6	39.5	26.9
100	405.8	403.2	257.5	298.8	0.6	36.5	26.4

Table V shows the total power consumptions derived from (2) over a wide range of F_{RECORD} values. From the second to the fifth columns of Table V, the power consumptions of the conventional VRS, the proposed VRSs, and the low-power H.264 VRS are presented, respectively. Three columns from the sixth to the eighth columns present the percentages of power saving (power gain) achieved by the proposed VRSs and the low-power H.264 VRS compared to the power used in conventional VRS. The experimental results show that the power consumptions of all VRSs increase as F_{RECORD} increases, but the rate of increase is different in each VRS. The LWC VRS reduces power consumption by up to 239.3 mW (71.6%) compared to the conventional VRS. However, for F_{RECORD} higher than 90%, the power gain by LWC VRS is lower than 10% due to H.264/AVC recompression for long-term storage in the permanent mode. The results in Table V indicate that, at all F_{RECORD} values, the use of LPF + DS operations consumes the lowest power consumption. Over the range of F_{RECORD} values, the LWC + DS VRS reduces power consumption from 148.3 mW (36.5%) to 242.2 mW (72.5%) compared to power levels in the conventional VRS. The low-power H.264 VRS achieves the power gain from 26.4% to 32.3% compared to the conventional VRS and it

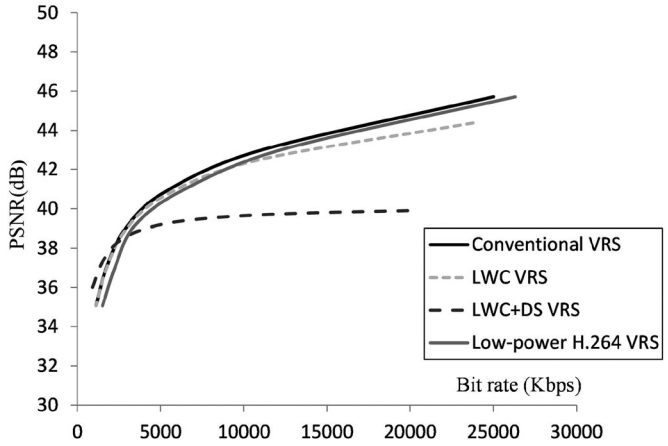

Fig. 8. Comparison of R-D performance in each VRS.

has little effect by the change of F_{RECORD} on the power gain because the operation of the low-power H.264 VRS is nearly same with the conventional VRS. These results indicate the advantage of an integrated hardware platform that can select the most suitable option according to the F_{RECORD} level.

E. Efficiency of the Proposed System

In this section, the efficiency of the proposed system and the selection scheme is evaluated in terms of the power reduction and R-D performance. The experimental data for the total power consumption are obtained from Table V. For the video quality, Fig. 8 presents the R-D curves for various VRSs. The horizontal and vertical axises represent the bitrates and PSNRs, respectively. The results of the conventional and proposed VRSs are obtained by Fig. 5 and the R-D performance of the low-power H.264 VRS is additionally simulated by using the encoding environment in Table I. LWC VRS achieves about the same video quality with the conventional VRS at the low bitrate, but the difference between them increases as the bitrate becomes higher. On the other hand, the low-power H.264 VRS offers a negligible quality degradation compared to the conventional VRS at the high bitrate, but the difference increases as the bitrate becomes small. The PSNR of the LWC + DS VRS is saturated and the image quality is not enhanced above a certain level due to the R-D loss caused by down-sampling.

As previously described in Section III, TH_R, the threshold used to decide whether the F_{RECORD} is high or low, is defined based on the trade-off between the power consumption and the R-D performance. Note that the LWC VRS and the low-power H.264 VRS are selectively utilized at the high bitrate according to F_{RECORD} instead of the LWC + DS VRS for avoiding the quality saturation at the high bitrate. As shown in Table V, the power saving by the low-power H.264 VRS exceeds that of the LWC VRS when F_{RECORD} is between 50% and 60%. Considering the trade-off between the power consumption and the video quality, the TH_R is set to 50% because the low-power H.264 VRS shows better video quality than the LWC VRS at the high bitrate as shown in Fig. 8.

By combining the power estimation in Table V and the R-D performance in Fig. 8, the relationship between the power saving and the image quality is evaluated. Tables VI and VII show the results with 10% of low F_{RECORD} and 70% of high F_{RECORD}, respectively. In these tables, the Bjontegaard Delta Peak Signal-to-Noise Ratio (BDPSNR) [29] and the power saving (PS) are presented according to the target bitrate. In addition, the ratio of the BDPSNR per the power saving (BDPSNR/PS) which represents the effectiveness of each VRS is also given. It should be noted that the R-D performances vary according to target bitrate whereas the power consumptions vary according to F_{RECORD}. The QP values for low bitrate are chosen as 24, 28, 32, and 36 to include a range of bitrates lower than 4000 Kb/s; whereas those for high bitrate are chosen as 12, 16, 20, and 24 to include a range of bitrates from 4000 to 25 000 Kb/s, at all VRSs except the LWC + DS VRS For comparing each VRS at the similar bitrate, the QP values for the LWC + DS VRS is smaller than that for other VRSs by 8 due to the effect of down-sampling. The VRSs with the bold character in these tables represent the best option for the given condition (i.e., F_{RECORD} and target bitrate) because they offer the highest BDPSNR/PS at the given condition. For the low target bitrate in Tables VI and VII, the LWC + DS VRS is the better choice than other VRSs because it achieves the highest power saving and best image quality. Both the power saving and the BDPSNR gain can be achieved by the LWC + DS VRS at the low target bitrate limitedly because down-sampling is more efficient than adjusting the QP value at the very low bitrate [19]. In most cases, the proposed systems achieve a power saving at the expense of the quality degradation. For the high target bitrate in Table VI, the LWC VRS is the best choice because it achieves the highest BDPSNR/PS and produces considerable power saving. For the high target bitrate in Table VII, the low-power H.264 VRS is appropriate for low-power mode systems because it offers a higher level of power saving and smaller R-D degradation than the LWC VRS. These results exactly match with the proposed optimal selection scheme in Fig. 6.

Figs. 9 and 10 show the still images of the reconstructed videos and their corresponding PSNRs and bitrates for each VRS in order to evaluate the efficiency of the proposed selection

TABLE VI
RELATIONSHIP BETWEEN THE BDPSNR AND THE POWER SAVING WHEN F_{RECORD} IS 10%

F_{RECORD} = 10%	Low Target Bitrate			High Target Bitrate		
	LWC	LWC + DS	LP H.264	LWC	LWC + DS	LP H.264
BDPSNR(dB)	−0.031	0.07	−0.313	−0.323	−2.202	−0.165
PS(%)	63.2	68.2	31.6	63.2	68.2	31.6
BDPSNR/PS	−0.049	0.103	−0.991	−0.511	−3.229	−0.522

TABLE VII
RELATIONSHIP BETWEEN THE BDPSNR AND THE POWER SAVING WHEN F_{RECORD} IS 70%

F_{RECORD} = 70%	Low Target Bitrate			High Target Bitrate		
	LWC	LWC + DS	LP H.264	LWC	LWC + DS	LP H.264
BDPSNR(dB)	−0.031	0.07	−0.313	−0.323	−2.202	−0.165
PS(%)	19.1	54.9	27.9	19.1	54.9	27.9
BDPSNR/PS	−0.162	0.128	−1.122	−1.691	−4.011	−0.591

Fig. 9. Still images of the reconstructed "Tractor" video sequences for the low bitrate. (a) Conventional VRS. (b) LWC VRS. (c) LWC + DS VRS. (d) Low-power H.264 VRS.

Fig. 10. Still images of the reconstructed "Tractor" video sequences for the high bitrate. (a) Conventional VRS. (b) LWC VRS. (c) LWC + DS VRS. (d) Low-power H.264 VRS.

scheme with comparison of subjective quality. Fig. 9 presents the reconstructed video sequences of four VRSs at the low bitrate (about 2200 Kb/s). Each sequence is decoded and played by a software decoder, MPlayer. "Tractor" video sequence in Table I is selected for the simulation and a part of the reconstructed video sequence which contains some characters is captured. The QP is chosen as 36 in the conventional, LWC, and low-power H.264 VRSs, whereas the QP is chosen as 28 in the LWC + DS VRS. Note that the small QPs are chosen for LWC + DS VRS because the down-sampler results in the similar bitrate to the increased QP value by 8. The results show that the difference among the conventional, LWC, and LWC + DS VRSs is invisible. The PSNR Y values of three VRSs are also very similar. In case of the low-power H.264 VRS, a quality degradation is visible with the 16 × 16 MB unit. It justifies the fact that the use of the down-sampler has little influence on the video quality at the low bitrate and thus, the choice of the down-sampler in the low bitrate is appropriate. Fig. 10 presents the reconstructed video sequences of four VRSs at high bitrate (about 20 000 Kb/s). Same video sequence of "Tractor" is used. The QP is chosen as 20 for three VRSs except the LWC + DS VRS, whereas the QP is chosen as 12 for the LWC + DS VRS. A quality degradation is visible in the LWC + DS VRS compared to other VRSs. Especially, it is hard to read the word in the LWC + DS VRS. The difference of the PSNR Y values between the LWC + DS VRS and other VRSs is also very large. However, the differences among the conventional, LWC, and low-power H.264 VRSs are invisible although the difference of the PSNR Y values between the conventional VRS and the other two VRSs is about 0.6 dB.

For further evaluation of the propose system, a previous study about the surveillance system in [30] is compared. A scheme proposed in [30] detects the content differences in the consecutive input frames by analyzing the color and moving correlation and reduces the unnecessary power consumption in the H.264/AVC encoder. To compare the proposed system and the surveillance system in [30] under the same condition, the surveillance system in [30] is implemented at the hardware platform in Fig. 7. Simulation results show that the proposed system achieves more than 18% of power saving compared to [30] although the proposed system leads to a negligible quality degradation by about 0.04 dB. This is because the use of the LWC instead of the H.264/AVC encoder in the proposed system achieves larger power saving than the application of the early skip mode decision in [30] and the down-sampler in the proposed system significantly reduces the power consumption of the H.264/AVC encoder for the permanent mode. The image quality is degraded because the proposed system utilizes supplementary LWC and down-sampler which cause the additional quality degradation.

V. Conclusion

The proposed LWC VRS utilizes LWC for temporary storage. The use of LWC instead of H.264/AVC compression achieves power saving, which increases as the percentage of short-term storage that is subsequently changed to long-term storage decreases. Additionally, a use of LPF and down-sampling can maintain a high level of power saving when almost video data are stored permanently thanks to a down-sampling operation which reduces the power consumed for long-term storage. In an integrated hardware platform, the two proposed systems and an additional system with a low-complexity H.264/AVC encoder are selectively applied to appropriate devices according to the proportion of long-term storage to short-term storage and the target bitrate. As a result, maximum power saving by up to 72.5% can be achieved with a minimum degradation of image quality compared with that obtained in a conventional VRS. In some recent smartphones, the video encoding operation contributes up to 40% of the total power consumption for video capture applications. This implies that the proposed system may save up to 29% of the power consumption of a mobile device.

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