A Dual-Channel Pipelined ADC With Sub-ADC Based on Flash–SAR Architecture

Young-Deuk Jeon, Jae-Won Nam, Kwi-Dong Kim, Tae Moon Roh, and Jong-Kee Kwon, *Member, IEEE*

***Abstract*—This brief presents a 10-bit dual-channel pipelined flash–successive approximation register (SAR) analog-to-digital converter (ADC) for high-speed applications. The proposed ADC consists of two channels for high operating speed, and each channel adopts a pipelined flash–SAR architecture for low power and a small area. The proposed flash–SAR ADC in the second stage is composed of a 1-bit flash ADC and a 6-bit SAR ADC considering the chip area, operation speed, and circuit complexity. The prototype ADC fabricated in a 45-nm CMOS process occupies 0.16 mm^2. The differential and integral nonlinearities of the ADC are less than 0.36 and 0.67 LSB, respectively. The ADC shows a signal-to-noise-and-distortion ratio of 54.6 dB and a spurious-free dynamic range of 64.0 dB with a 78-MHz input at 230 MS/s with a 1.1-V supply. The maximum operating frequency of the ADC is 260 MS/s at a 1.2-V supply. The power consumptions of the ADC with 230 and 260 MS/s are 13.9 and 17.8 mW, respectively.**

***Index Terms*—Analog-to-digital converter (ADC), flash, operational amplifier (op-amp) sharing, pipelined, reference buffer, successive approximation register (SAR).**

I. Introduction

RECENTLY, as the requirement of video signal processing and communication systems such as digital television and wireless receivers has been rapidly increased, low-power small-area 10-bit analog-to-digital converters (ADCs) with several hundreds of megahertz of sampling rate are considered to be one of the significant components. For these high-speed ADCs, a pipeline architecture using flash sub-ADCs is popularly employed to optimize the power and area [1]–[4].

On the other hand, with the scaling down of CMOS technology, successive approximation register (SAR) ADCs are widely used because of their high power efficiency and small area. In a 10-bit resolution, the operating frequency of conventional SAR ADCs is increased up to 100 MHz by asynchronous internal clocks, error compensation, capacitor switching techniques, and so on [5], [6]. Nevertheless, conventional SAR ADCs still have speed limitations due to their serial signal processing. Most high-speed SAR ADCs have a short sampling period of 10%–20% duty cycle, which can obtain sufficient SAR conversion (SC) time easily. However, buffers such as variable-gain amplifiers and analog filters driving SAR ADCs require a wide-bandwidth operational amplifier (op-amp), which is the most power-hungry block in analog front-end circuits.

To merge the efficiency of SAR ADCs and the high-speed operation of pipelined ADCs, a pipelined SAR architecture has been presented [7], [8]. Although this architecture is suitable for a small chip area and low power consumption compared to conventional pipelined ADCs, it is not easy to implement the pipelined SAR ADC with one channel for operating frequencies of 200 MHz or higher. Also, time-interleaved pipelined SAR ADCs for a high sampling rate demand calibration techniques to remove channel offset, interchannel gain error, and capacitor mismatch [9], [10].

In this brief, a dual-channel pipelined flash–SAR ADC without calibration is presented. For a high sampling rate, the dual-channel and flash–SAR architectures are adopted. The power consumption and area are decreased by an op-amp sharing technique. A proposed adaptable clock technique simplifies the clock generator, and a reference scheme with three buffers and a deglitch circuit minimizes channel mismatch and reference interference. Section II discusses the proposed pipelined flash–SAR architecture and the operating timing. Section III describes the detailed circuits to implement the proposed ADC. The experimental results are presented in Section IV. Finally, the conclusion is given in Section V.

II. Architecture of the Proposed Dual-Channel Pipelined Flash–SAR ADC

A. Architecture

Fig. 1 shows the block diagram of the proposed 10-bit pipelined ADC. It comprises two channels, and each channel sequentially processes an analog signal with two stages. To optimize the area and operating frequency, sub-ADCs are implemented by 4-bit SAR ADCs and 7-bit flash–SAR ADCs based on asynchronous decision [11]. The flash–SAR architecture is suitable for reducing the SC cycle for high operating frequencies. To further reduce the power and area, an op-amp is shared between the two channels. The remaining blocks commonly used include an error correction logic (ECL), three reference buffers with a deglitch technique, a current generator, and a four-phase clock generator. The ECL corrects the digital code by overlapping 1 bit between the first and second stages. To decrease channel mismatches and to preserve the reference accuracy in all operation modes, the three reference buffers are adopted. Two reference buffers are used for the first stage of two 4-bit SAR ADCs and the op-amp, and the remaining reference buffer is used for the second stage of two 7-bit flash–SAR ADCs. The proposed deglitch technique can reduce reference

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The authors are with the Convergence Components and Materials Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea (e-mail: ydjeon@etri.re.kr).

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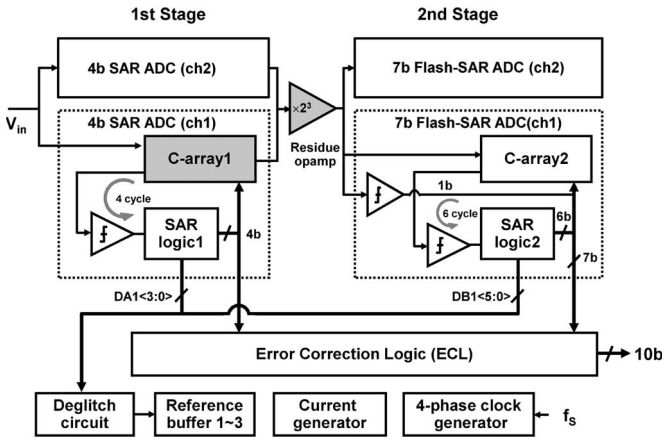

Fig. 1. Architecture of the proposed dual-channel pipelined flash–SAR ADC.

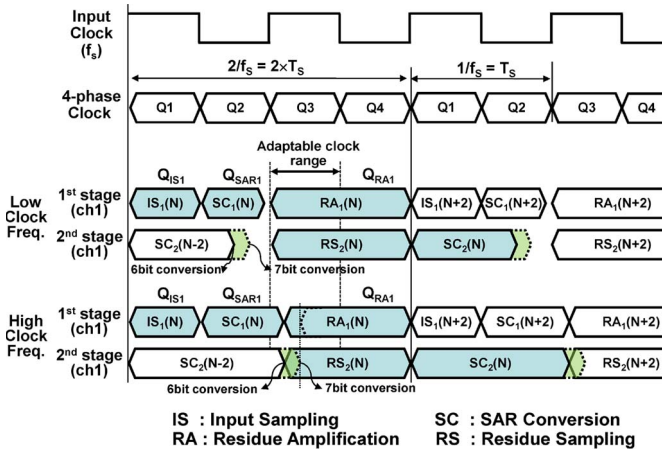

Fig. 2. Timing diagram of the proposed ADC (channel 1).

glitches generated by capacitor switching. The current generator to supply a constant current to the analog blocks such as comparators and op-amps is designed with a resistor and two N-channel MOSFET (NMOS) for a small area. The four-phase clock generator is needed for the dual-channel flash–SAR architecture.

B. Operation Timing

Fig. 2 shows a detailed timing diagram of channel 1 based on the adaptable clock technique to efficiently allocate the periods of the internal clocks. The operation of channel 2 is the same as that of channel 1 having the clock shifted by one cycle $(1/f_S)$ for ADC functions. The clocks for input sampling (IS), SC, residue amplification (RA), and residue sampling (RS) are internally generated by each stage.

The first stage is operated with three phases of IS_1, SC_1, and RA_1, and the second stage is operated with two phases of RS_2 and SC_2. First, the analog input is sampled by the first stage during $\mathrm{IS}_1(N)$ and the 4-bit SC is started at the rising edge of Q2. The internal clocks of $\mathrm{RA}_1(N)$ and $\mathrm{RS}_2(N)$ are designed to automatically transit to high state within Q3 after the first and second SCs are completely finished. Because the period of $\mathrm{SC}_1(N)$ for the 4-bit SAR ADC is fixed by the architecture and circuit parameters, the amplification time is variable according to the input clock frequency. To guarantee the operations of $\mathrm{RA}_1(N)$ and $\mathrm{RS}_2(N)$, the minimum $\mathrm{RA}_1(N)$ and $\mathrm{RS}_2(N)$ periods are designed with Q4, and $\mathrm{SC}_2(N)$ for the 7-bit ADC of the second stage is performed from the next Q1.

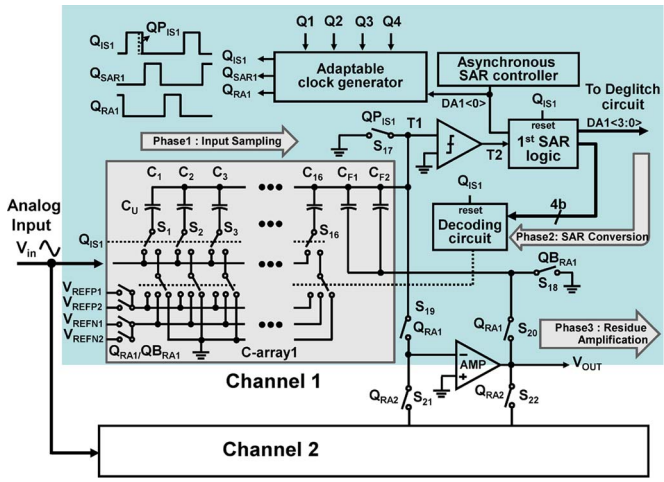

Fig. 3. First stage based on the 4-bit SAR architecture.

The 4- and 7-bit SC times of the proposed ADC are about 3.2 and 5.6 ns, respectively. At low clock frequencies, the sum of the $\mathrm{IS}_1(N)$ and $\mathrm{SC}_1(N)$ periods of the first stage is longer than the $\mathrm{SC}_2(N-2)$ period of the second stage due to a sufficient $\mathrm{IS}_1(N)$ period that is identical to Q1. Then, the $\mathrm{RA}_1(N)$ period is the same as the sum of Q3 and Q4 since the $\mathrm{SC}_1(N)$ and $\mathrm{SC}_2(N-2)$ operations are ended within Q2. On the other hand, at high clock frequencies over 200 MHz, the $\mathrm{SC}_2(N-2)$ period is longer than the sum of $\mathrm{IS}_1(N)$ and $\mathrm{SC}_1(N)$ because the average 1-bit decision time is about 0.8 ns. As a result, the $\mathrm{RA}_1(N)$ period is reduced under the sum of Q3 and Q4. The $\mathrm{RA}_1(N)$ period is about 4.0–4.1 ns considering the nonoverlap clock margin. The bottleneck of the ADC operating speed in the proposed architecture is the second stage. To solve this problem, the proposed ADC adopts the flash–SAR architecture in the second stage. The flash ADC decides 1 bit at the end of $\mathrm{RA}_1(N)$ and the SAR ADC decides 6 bits during $\mathrm{SC}_2(N)$. Therefore, the proposed ADC achieves a high sampling rate over 200 MHz.

III. Pipelined Flash–SAR ADC Implementation

A. First Stage Using 4-Bit SAR ADC

A block diagram of the first stage is shown in Fig. 3. Channel 1 of the first stage is composed of the C-array1 with 16 unit capacitors and two feedback capacitors, a comparator, a SAR logic, a SAR controller, an adaptable clock generator, a decoding circuit, and a shared op-amp. The function of the first stage is divided into an IS, an SC for 4-bit decision, and an RA. Generally, pipelined ADCs require a sample-and-hold amplifier (SHA) to reduce a sampling mismatch between a sub-ADC using a flash type and a multiplying digital-to-analog converter (MDAC). In the proposed ADC, the front-end SHA is not needed because the C-array1 is commonly used for the sub-ADC and MDAC functions. The unit capacitance and the total sampling capacitance of the C-array1 are 100 fF and 1.6 pF considering capacitor mismatch and kT/C noise, respectively. The reference switches connected to the bottom plate of the unit capacitor are controlled by the decoding circuit. Also, the op-amp sharing technique is applied between the two channels

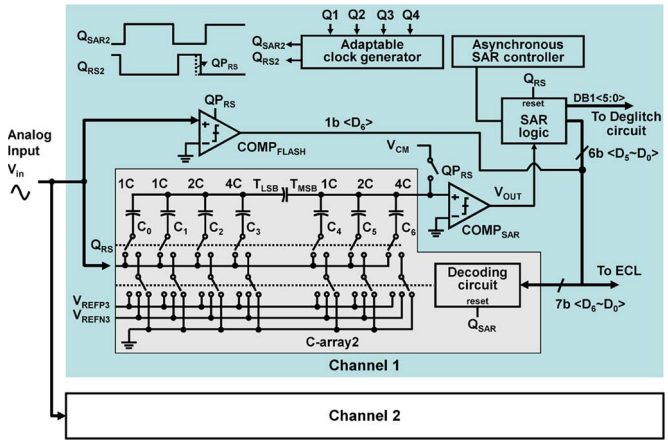

Fig. 4. Second stage based on the 7-bit flash–SAR architecture.

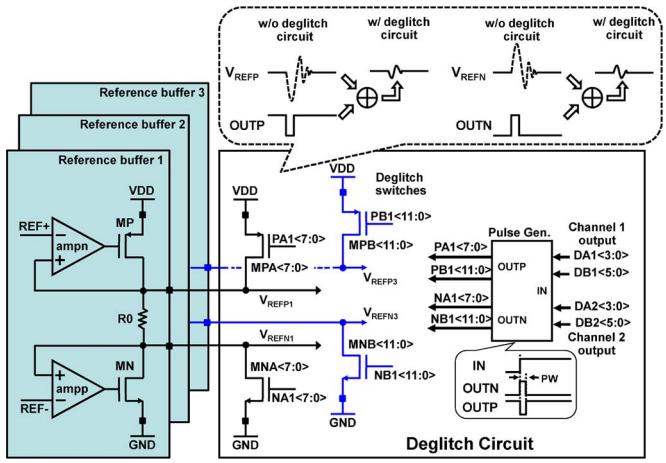

Fig. 5. Reference buffers with the deglitch technique.

to decrease the power and area. The residue op-amp uses a two-stage architecture that consists of a complementary folded-cascode op-amp to achieve high dc gain and a complementary input pair op-amp to obtain high transconductance and a wide output swing [1]. For an identical load condition of the shared op-amp in each channel, a common-mode feedback (CMFB) based on a switched-capacitor type is divided by two with opposite clock phases. The divided CMFB has half the capacitance of the conventional CMFB to maintain the total capacitance.

The comparator for the SC is composed of a preamplifier and a latch. The thermal noise of the comparator is nearly ignored due to its low resolution. The SAR controller generates the asynchronous clock for the iterative operation of the SAR ADC. The internal clocks of $Q_{\rm IS}$, $Q_{\rm SAR}$, and $Q_{\rm RA}$ are made by the adaptable clock generator with a combination of the four-phase clocks and the LSB bit-decision signal $\mathrm{DA1}\langle 0\rangle$.

B. Second Stage Using a 7-Bit Flash–SAR ADC

Fig. 4 shows the second stage including the 7-bit flash–SAR ADC to reduce the SC time. The MSB is determined by the 1-bit flash ADC and the remaining LSBs are decided by the 6-bit SAR ADC. Typically, since a flash ADC consists of $2^N - 1$ comparators, the 1-bit flash ADC requires only one comparator, which detects the zero crossing of the differential input. Therefore, any extra circuits such as a resistor array for subreference voltages and a thermal-to-binary decoder are not required. The C-array2 for the SC is implemented with a split-capacitor architecture using a $V_{\rm CM}$-based switching scheme to reduce the number of capacitors [6]. The total number of capacitors, including the split capacitor, is 16 and the unit capacitance is 55 fF. The split capacitor is larger than the unit capacitor due to the parasitic capacitance of the $T_{\rm LSB}$ node. To reduce the bottom parasitic capacitance of metal–oxide–metal capacitors, metal layer 1 is not used in the implementation of all capacitors.

The operation of the second stage is summarized as follows. At the end of $\mathrm{QP_{RS}}$, the comparator for the 1-bit flash ADC decides the MSB of D_6 and the MSB code is transferred to the decoding circuit of the C-array2 for the 6-bit SC. Then, the bottom plate of capacitor C_6 is connected to $V_{\rm REFP3}$ or $V_{\rm REFN3}$ and the remaining capacitors C_0–C_5 are connected to $V_{\rm CM}$ at the rising edge of $Q_{\rm SAR}$. The comparator for the SAR ADC sequentially decides from D_5 to D_0. Therefore, the conversion time of the 7-bit flash–SAR ADC is identical to that of the conventional 6-bit SAR ADC.

C. Three Reference Buffers With the Deglitch Technique

The three reference buffers with the deglitch technique are shown in Fig. 5. In the proposed ADC, the reference buffers have to drive two 4-bit SAR ADCs, two 7-bit flash–SAR ADCs, and the shared residue op-amp operated with the MDAC function. In particular, the reference voltages are settled in under 0.8 ns for the SAR ADCs with 7-bit accuracy. To satisfy the settling condition, the proposed ADC adopts the deglitch technique based on deglitch switches of MPA, MPB, MNA, and MNB as well as a pulse generator. When the reference switches connected to the bottom plates of the capacitors are turned on, the reference voltages make large peaks in an instant and the next are settled to the required voltage level. To stabilize the reference voltages in a short time, the conventional reference buffers dissipate the large static current flowing through $R0$. On the other hand, the reference buffers with the proposed deglitch technique can reduce the static current by means of the dynamic current control using the deglitch switches. Because the bit-decision signals of $\mathrm{DA1} \sim 2\langle 3:0\rangle$ and $\mathrm{DB1} \sim 2\langle 5:0\rangle$ and the digital output codes are simultaneously generated by the SAR ADCs, the reference glitches occur after the transition of the bit-decision signals caused by the delay time of the decoding circuit. The control signals of $\mathrm{PA1}\langle 7:0\rangle$, $\mathrm{PB1}\langle 11:0\rangle$, $\mathrm{NA1}\langle 7:0\rangle$, and $\mathrm{NB1}\langle 11:0\rangle$ with the fixed pulsewidth are simply made by the pulse generator. Therefore, the NMOS and P-channel MOSFET (PMOS) switches are turned on to supply a large amount of charge to $V_{\rm REFP}$ and $V_{\rm REFN}$ at the point of the reference switching. The deglitch switches are connected to VDD or GND since the large peaks of the reference voltages occur in the direction of a common-mode voltage. The size of each switch is decided by the pulsewidth and the number of the unit capacitor connected to the reference voltages.

Although the reference voltage settling is improved by the deglitch technique, it is difficult to implement the dual-channel pipelined SAR ADC using one reference buffer. In the RA period of channel 1, the reference voltage glitches generated by the SAR ADCs of channel 2 disturb the output of the op-amp for channel 1, as described in Fig. 6. To solve the interference of the reference voltages, one method is to use one

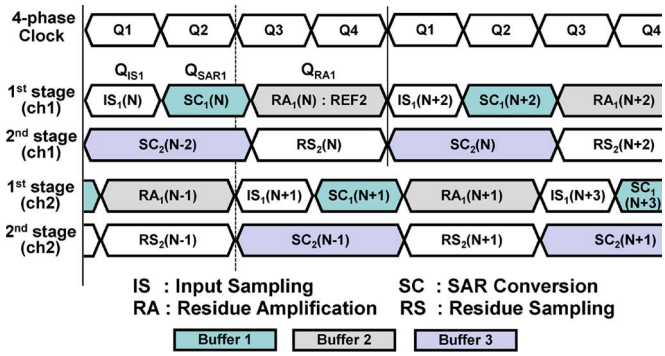

Fig. 6. Three-reference-buffer scheme of the proposed ADC.

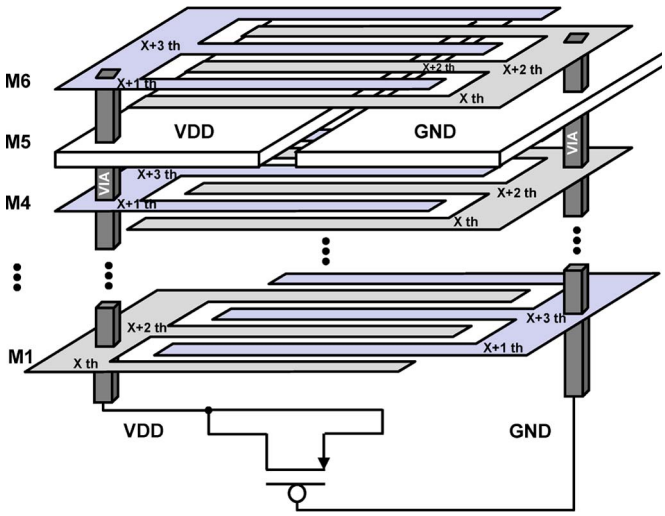

Fig. 7. Power capacitors based on the metal and PMOS.

reference buffer for each channel [12]. However, this method causes gain mismatch due to the difference in the reference voltages of the two channels. As shown in Fig. 6, the proposed reference scheme is based on three reference buffers to reduce the channel mismatch and interference. Reference buffer 1 is used during two 4-bit SCs and reference buffer 2 is used during the RA in the first stage. Finally, reference buffer 3 is used during two 7-bit flash–SAR conversions in the second stage. In this case, the channel mismatch can be removed, and the reference interference does not occur since the reference buffers are shared and divided by the function of the ADC.

D. Power Capacitors

Fig. 7 shows the power capacitors that are composed of metal-to-metal parasitic capacitors and a PMOS transistor. Metal layers 1–6 of a finger type are located on or under the power lines of VDD and GND. To maximize the parasitic capacitance, the fingers of VDD and GND are drawn with zigzag patterns according to even or odd metal layers. Also, the PMOS capacitors are drawn under the power lines of metal 1. As a result, the total parasitic capacitance between the supply and ground is about 26 pF within the ADC core area.

IV. Experimental Results

The prototype dual-channel pipelined flash–SAR ADC is fabricated in a 45-nm CMOS process, as shown in Fig. 8.

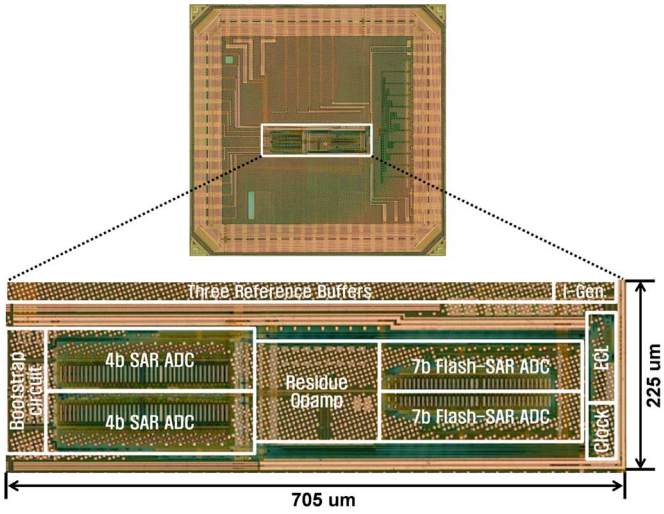

Fig. 8. Die photograph.

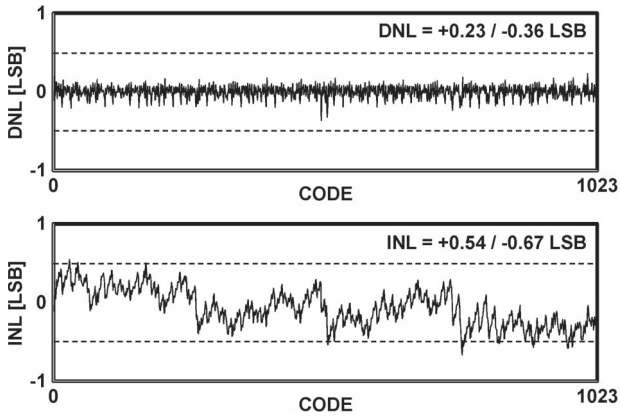

Fig. 9. Measured DNL and INL.

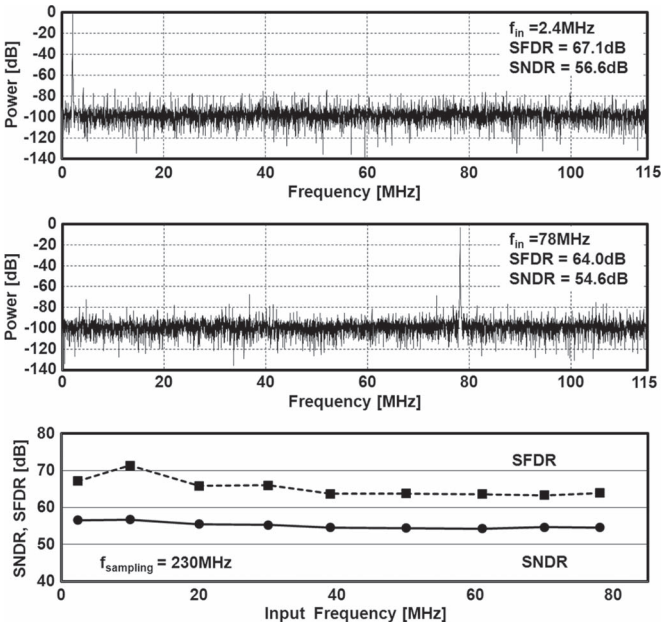

Fig. 10. Measured FFT plots and dynamic performance of the proposed ADC at 1.1 V.

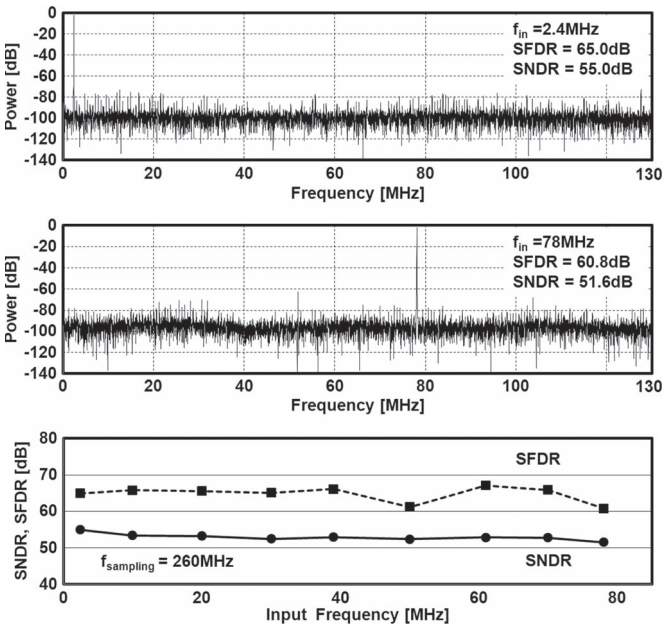

Fig. 11. Measured FFT plots and dynamic performance of the proposed ADC at 1.2 V. Spurious-free dynamic range (SFDR).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

		[1]	[9]	[10]	This Work	
Architecture		Pipeline	TI-Pipeline SAR	TI-Pipeline SAR	TI-Pipeline SAR	
Technology		90 nm	65 nm	40 nm	45 nm	
Resolution		10 bit	10 bit	11 bit	10 bit	
Supply		1.0 V	1.1 V	1.1 V	1.1 V	1.2 V
Speed		205 MS/s	160 MS/s	250 MS/s	230 MS/s	260 MS/s
DNL		0.5 LSB	0.46 LSB	0.8 LSB	0.36 LSB	
INL		0.5 LSB	1.7 LSB	1.5 LSB	0.67 LSB	
SNDR (@fin)		53. 9 dB @79MHz	52.2 @79MHz	56 dB @125MHz	54.6 dB @78MHz	51.6 dB @78MHz
Power	w/ Ref.	61 mW	-	-	13.9 mW	17.8 mW
	w/o Ref.	-	2.72 mW	1.7 mW	7.9 mW	10.4 mW
FOM	w/ Ref.	954 fJ/step	-	-	203 fJ/step	367 fJ/step
	w/o Ref.	-	52 fJ/step	13 fJ/step	115 fJ/step	215 fJ/step
Die area		1.0 mm^2	0.21 mm^2	0.066 mm^2	0.16 mm^2	
Calibration		No	Yes	Yes	No	

The active die area of the proposed ADC is 0.16 mm^2 ($= 0.705\ mm \times 0.225\ mm$) with the three reference buffers. To reduce channel mismatches, analog blocks are placed adjacent to each other. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) at a 10-bit accuracy are plotted in Fig. 9. The DNL and INL are $+0.23/-0.36$ LSB and $+0.54/-0.67$ LSB, respectively. Fig. 10 shows the measured fast Fourier transform (FFT) plots and dynamic performance of the ADC at a 1.1-V supply. The signal-to-noise-and-distortion ratio (SNDR) at a 2.4-MHz input frequency is 56.6 dB and remains above 54.6 dB up to a 78-MHz input frequency. In the supply voltage sweep results, the proposed ADC operates up to 260 MS/s at a 1.2-V supply, as shown in Fig. 11. At a 78-MHz input frequency, the SNDR is 51.6 dB, and the effective number of bits (ENOB) is over 8.8 bits. The improved operation speed of the proposed ADC is caused by the reduction of the comparator and logic delays in the SAR ADCs. The power consumption and figure of merit (FOM) of the ADC are summarized in Table I. The ADC dissipates about 13.9 mW at a 1.1-V supply. The analog power is 10.6 mW containing 6.0 mW from the three reference buffers and the digital power is 3.3 mW. At a 1.2-V supply, the ADC dissipates 17.8 mW, which consists of the analog power of 13.0 mW and the digital power of 4.8 mW. The FOMs of the proposed ADC, defined as $\text{Power}/(2{*}f_{\text{in}}{*}2^{\text{ENOB}})$, are 203 and 367 fJ/conversion step at a 78-MHz input with 230 and 260 MS/s, respectively.

V. CONCLUSION

A pipelined flash–SAR ADC employing a dual-channel architecture without calibration has been presented. To improve the sampling rate, the adaptable timing technique and the flash–SAR architecture with two channels are used. The channel mismatch is removed by the proposed reference scheme with three reference buffers. The prototype ADC fabricated in a 45-nm CMOS process occupies 0.16 mm^2 and dissipates 13.9 mW at 230 MS/s with a 1.1-V supply. The operating frequency of the ADC is increased up to 260 MS/s at a 1.2-V supply.

REFERENCES

[1] S.-C. Lee, Y.-D. Jeon, J.-K. Kwon, and J. Kim, "A 10-bit 205 MS/s 1.0-mm^2 90-nm CMOS pipeline ADC for flat panel display applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2688–2695, Dec. 2007.

[2] B. Hernes, J. Bjornsen, T. N. Andersen, A. Vinje, H. Korsvoll, F. Telsto, A. Briskemyr, C. Holdo, and O. Moldsvor, "A 92.5 mW 205 MS/s 10 b pipeline IF ADC implemented in 1.2 V/3.3 V 0.13 μm CMOS," in *Proc. IEEE ISSCC Tech. Dig.*, Feb. 2007, pp. 462–615.

[3] D. Kurose, T. Ito, T. Ueno, T. Yamaji, and T. Itakura, "55-mW 200-MSPS 10-bit pipeline ADCs for wireless receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1589–1595, Jul. 2006.

[4] Z. Cao and S. Yan, "A 52 mW 10 b 210 MS/s two-step ADC for digital-IF receivers in 0.13 μm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 309–312.

[5] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, C.-M. Huang, C.-H. Huang, L. Bu, and C.-C. Tsai, "A 10 b 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *Proc. IEEE ISSCC Tech. Dig.*, Feb. 2010, pp. 386–387.

[6] Y. Zhu, C.-H. Chan, U.-F. Chio, S.-W. Sin, U. Seng-Pan, R. P. Martins, and F. Maloberti, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[7] C. C. Lee and M. P. Flynn, "A SAR-assisted two-stage pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

[8] M. Furuta, M. Nozawa, and T. Itakura, "A 10-bit, 40-MS/s, 1.21 mW pipelined SAR ADC using single-ended 1.5-bit/cycle conversion technique," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1360–1370, Jun. 2011.

[9] Y. Zhu, C.-H. Chan, S.-W. Sin, U. Seng-Pan, R. P. Martins, and F. Maloberti, "A 35 fJ 10 b 160 MS/s pipelined-SAR ADC with decoupled flip-around MDAC and self-embedded offset cancellation," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2011, pp. 61–64.

[10] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11 b 250 MS/s 2× interleaved fully dynamic pipelined SAR ADC in 40 nm digital CMOS," in *Proc. IEEE ISSCC Tech. Dig.*, Feb. 2012, pp. 466–468.

[11] Y.-K. Cho, Y.-D. Jeon, J.-W. Nam, and J.-K. Kwon, "A 9-bit 80 MS/s successive approximation register analog-to-digital converter with a capacitor reduction technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 7, pp. 502–506, Jul. 2010.

[12] Y.-D. Jeon, Y.-K. Cho, J.-W. Nam, K.-D. kim, W.-Y. Lee, K.-T. Hong, and J.-K. Kwon, "A 9.15 mW 0.22 mm^2 10 b 204 MS/s pipelined SAR ADC in 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 473–476.