A 9-bit 80 MS/s Successive Approximation Register Analog-to-Digital Converter With a Capacitor Reduction Technique

Young-Kyun Cho, Young-Deuk Jeon, Jae-Won Nam, and Jong-Kee Kwon, *Member, IEEE*

***Abstract*—A 9-bit 80 MS/s successive approximation register analog-to-digital converter (ADC), which is suitable for low power and a small area, is presented. The 9-bit capacitor array consists of only 16 unit capacitors and a coupling capacitor due to the proposed binary-weighted split-capacitor arrays with a merged-capacitor switching technique. The proposed ADC includes a comparator with offset cancellation and uses digital calibration for error correction. The ADC is implemented in a 65-nm complimentary metal–oxide–semiconductor technology and occupies an active area of 0.068 mm^2 with a reference buffer. The differential and integral nonlinearities of the ADC are less than 0.37 and 0.40 LSB, respectively. The ADC shows a signal-to-noise-distortion ratio of 50.71 dB, a spurious-free dynamic range of 66.72 dB, and an effective number of bits of 8.13 bits with a 78 MHz sinusoidal input at 80 MS/s. The ADC consumes 3.4 mW with the reference buffer at a 1.0-V supply and achieves a figure of merit of 78 fJ/conversion step.**

***Index Terms*—Error correction, merged-capacitor switching (MCS), offset cancellation, split-capacitor array, successive approximation register (SAR) analog-to-digital converter (ADC).**

I. Introduction

HIGH-SPEED and medium-resolution Nyquist-rate analog-to-digital converters (ADCs) find a wide range of applications in many different areas, such as high-speed wireline and wireless communication systems [1], [2]. In these applications, low-power and small-area ADCs requiring conversion rates higher than 60 MS/s and a resolution in the range of 7–9 bits are considered an important building block [1]. Among many ADC architectures, successive approximation register (SAR) ADCs have proven to be very efficient for meeting the above requirement of high speed, medium resolution, and low power consumption [3]–[5]. Meanwhile, the total capacitances in SAR ADCs based on a capacitive digital-to-analog converter (DAC) [7] increase exponentially with the number of bits, and the minimum value of unit capacitor is limited by thermal noise. Large capacitances consume excessive area and more power with longer settling times. In addition, the control logic becomes more complicated due to the increased numbers of capacitors and switches. Therefore, considerable efforts have to take place in reducing the complexity and the area of the DAC without sacrificing robustness.

In this brief, we present a 9-bit 80 MS/s SAR ADC using binary-weighted split-capacitor arrays with a merged-capacitor switching (MCS) technique in a 65-nm CMOS. The capacitor array consists of only 16 unit capacitors and a coupling capacitor, which reduces the required number of unit capacitors compared to that in earlier studies [7]–[9]. This brief is organized as follows. Section II introduces the proposed ADC architecture, Section III describes the circuit implementation, Section IV shows measurement results, and Section V is the conclusion.

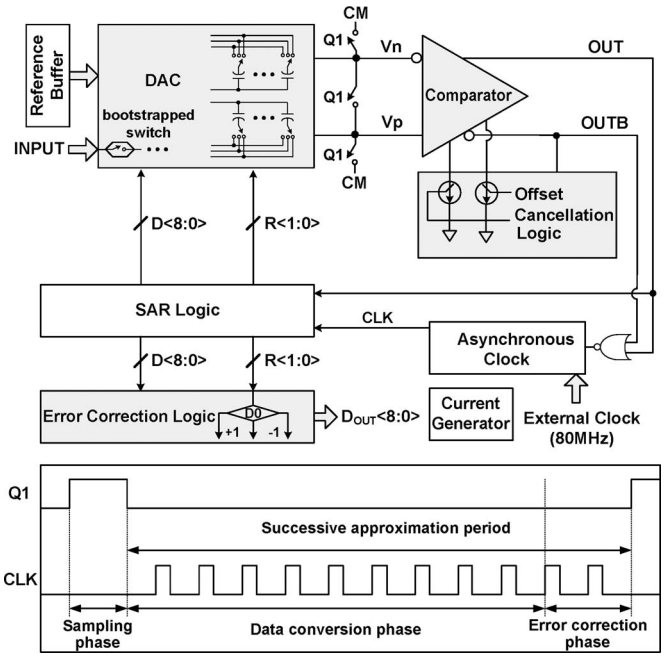

Fig. 1. Block diagram of the proposed SAR ADC.

II. Architecture of the Proposed SAR ADC

The block diagram of the proposed SAR ADC operating at a 1.0-V supply is described in Fig. 1. The main components of the SAR ADC are a DAC with bootstrapped switches, a

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The authors are with the Convergence Components and Materials Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea (e-mail: ykcho@etri.re.kr).

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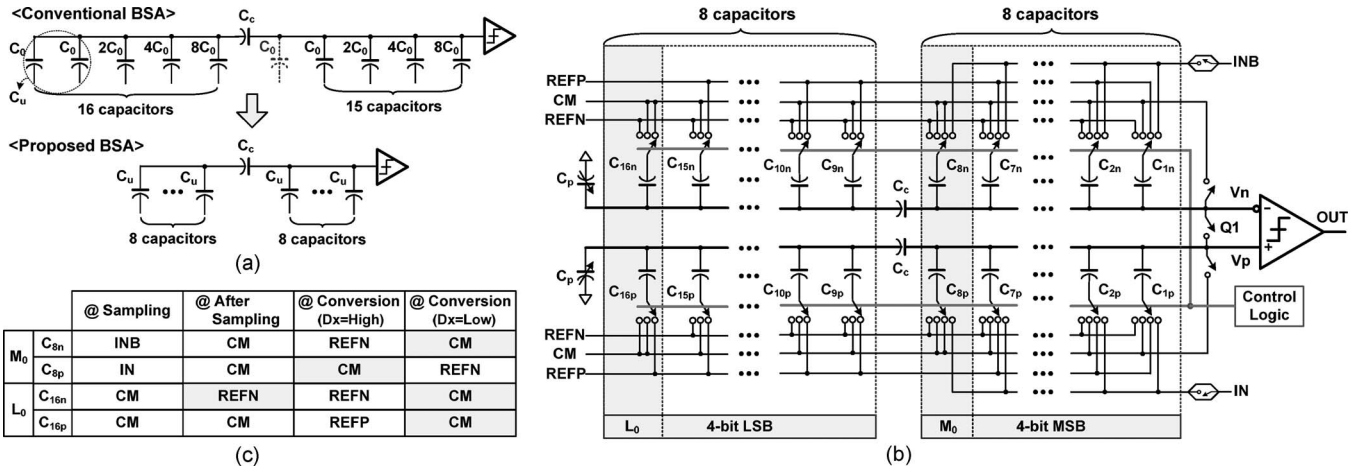

(c)

		@ Sampling	@ After Sampling	@ Conversion (Dx=High)	@ Conversion (Dx=Low)
M_0	C_{8n}	INB	CM	REFN	CM
	C_{8p}	IN	CM	CM	REFN
L_0	C_{16n}	CM	REFN	REFN	CM
	C_{16p}	CM	CM	REFP	CM

Fig. 2. Structure and operation of the proposed DAC. (a) Capacitor merging in the split-capacitor array. (b) Proposed 9-bit DAC structure. (c) Switching operation of the DAC.

regenerative comparator with an offset cancellation logic, an asynchronous clock [6], an SAR logic, an error correction logic (ECL), a current generator, and an on-chip reference buffer. The split-capacitor network with the MCS technique is used to sample the input signal and serves as a DAC for creating and subtracting reference voltages. Bootstrapped n-type metal–oxide–semiconductor switches [10] are located in the DAC and directly connected to the input signal. The control signal of the switch is boosted to achieve an appropriate on-resistance at a 1.0-V supply voltage and minimize signal distortion. The clock signal of 80 MHz was applied to an asynchronous clock. An asynchronous timing technique is employed to improve the internal operation speed up to 1.05 GHz and power efficiency. The current generator used instead of a bandgap reference adopts a modified Widlar current source for a low supply voltage and a small area. In addition, the ADC has incorporated a high-performance on-chip reference buffer that reduces the need for external components, thereby reducing system complexity and circuitry area.

The entire conversion is divided into three parts. The first phase is for input sampling assigned to 16% of the whole period. Data conversion is then performed during the next phase, and error correction follows as the last phase. Using a binary search algorithm, the DAC output voltage successively approximates a common mode voltage (*CM*).

III. ADC Architecture Implementation

A. Split-Capacitor DAC With an MCS Technique

Conventional split-capacitor arrays in Fig. 2(a) require 15 and 16 unit capacitors in the MSB and LSB sides, respectively. The MSB side of the split-capacitor arrays cannot adopt an MCS technique [11] due to the odd number of capacitors. To apply the merged-capacitor technique, a unit capacitor C_0 (shown in the dotted line) is added, and the input voltages are sampled only on the MSB side for maintaining the sampling value. Thus, the proposed split-capacitor arrays with the MCS technique merge two unit capacitors into one both in the MSB and LSB sides, and the number of unit capacitors required in the proposed split-capacitor arrays is reduced by about 50%. In addition, the unit capacitor size may be doubled to obtain the better capacitor matching accuracy, while speed and power consumption remain constant. The proposed split-capacitor array consists of only 16 unit capacitors (C_u) and a coupling capacitor (C_c), which reduces the required number of unit capacitors by 64% in a 9-bit resolution compared to that in [8]. The DAC using the binary-weighted split-capacitor arrays (BSA) with an MCS (BSA-MCS) technique is shown in Fig. 2(b). The unit capacitance $(C_{1n,p} \sim C_{16n,p})$ is 80 fF, the coupling capacitance is 64 fF, and the total sampling capacitance of the DAC is 640 fF. Two-bit parasitic capacitors (C_p) were placed to compensate the mismatch of the coupling capacitor. The adjustment range of C_p is from 0 to $0.6C_u$ with a minimum step of $0.2C_u$. A common centroid layout was used to implement the capacitor array, and dummy capacitors around the core capacitor array were placed for capacitor matching and symmetry layout.

The operation of the proposed DAC employing the BSA-MCS technique is identical to that of the conventional DAC. The only difference is that the capacitors M_0 and L_0 in Fig. 2(b) are switched individually during the sampling and conversion period. As mentioned above, the unit capacitor is added to the MSB capacitor array to apply the MCS technique. Due to the added capacitor, the offset voltage inevitably gives rise to the DAC during the subsequent approximation period. It should be designed that the offset voltage is held constant during each conversion step in order to avoid the detrimental effects of the circuit behavior. Thus, the bottom plates of capacitors M_0 and L_0 are separately switched to CM for the constant offset voltage. The offset voltage, which is equally distributed during the quantization intervals, does not affect the performance of the ADC. The table in Fig. 2(c) illustrates the switching operation of capacitors M_0 and L_0 for the BSA-MCS technique.

The detailed operation of the DAC is carried out as follows. At a sampling phase, the input voltages are sampled only on the MSB side to maintain the sampling value. After the sampling phase, all capacitor switches in the DAC are connected to CM without the C_{16n} capacitor by the BSA-MCS technique. Then, the comparator compares the input voltage denoted by

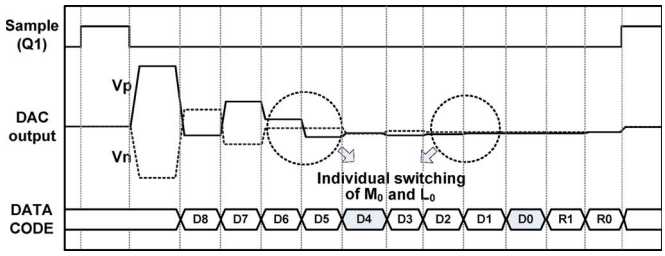

Fig. 3. Output waveforms of the proposed DAC.

the difference of positive input voltage (IN) and negative input voltage (INB) with 0 and decides the MSB code, i.e., D8. Hence, the MSB behaves like a sign bit, which reduces further the capacitors by 1 bit [5]. In this state, the DAC shows an offset voltage of $1/272 \cdot V_{\mathrm{REF}}$. V_{REF} is the difference of the positive reference voltage (*REFP*) and the negative reference voltage (*REFN*). After this phase, the operation of the DAC is identical to that of the conventional DAC without the switching operation of the fifth code of D4 and the LSB code of D0 decision. Individual switching of $C_{8n,p}$ and $C_{16n,p}$ capacitors is performed at the output code decision states of D4 and D0. In these states, the switches do not operate differentially to maintain the constant offset voltage. The output waveform of the DAC is shown in Fig. 3. Nondifferential output waveforms of the DAC shown in dotted circles are achieved due to the individual switching operation.

For a more general case, the DAC employing the BSA-MCS technique shows a $2(k+1)+1$ bit resolution with a k-bit capacitor array in the MSB and LSB sides. Then, the offset voltage of the DAC can be calculated as

$$V_{\mathrm{offset}} = \frac{2}{2^{k+1} \cdot (2^{k+1}+1)} \cdot (\mathrm{CM} - \mathrm{REFN}). \tag{1}$$

CM is given as

$$\mathrm{CM} = \frac{\mathrm{REFP} + \mathrm{REFN}}{2}. \tag{2}$$

According to (2), the offset voltage is given as

$$V_{\mathrm{offset}} = \frac{1}{2^{k+1} \cdot (2^{k+1}+1)} \cdot V_{\mathrm{REF}}. \tag{3}$$

Due to the BSA-MCS technique, the offset voltage is equally distributed to every conversion state and does not affect the operation of the DAC.

B. Comparator With Offset Cancellation

The foreground offset voltage cancellation scheme of the SAR ADC is shown in Fig. 4(a). During the sampling phase, the DAC sample CM and the inputs of the comparator are shorted to CM. The offset calibration takes place during the data conversion phase in which all of the capacitor switches in the DAC are connected to CM except for a C_{16n} capacitor according to the BSA-MCS technique. The output of the comparator (OUT), therefore, shows the offset of the comparator and the DAC. Then, it is fed into a 4-bit up/down counter. The 3-bit LSBs of the counter control the compensation current in equal

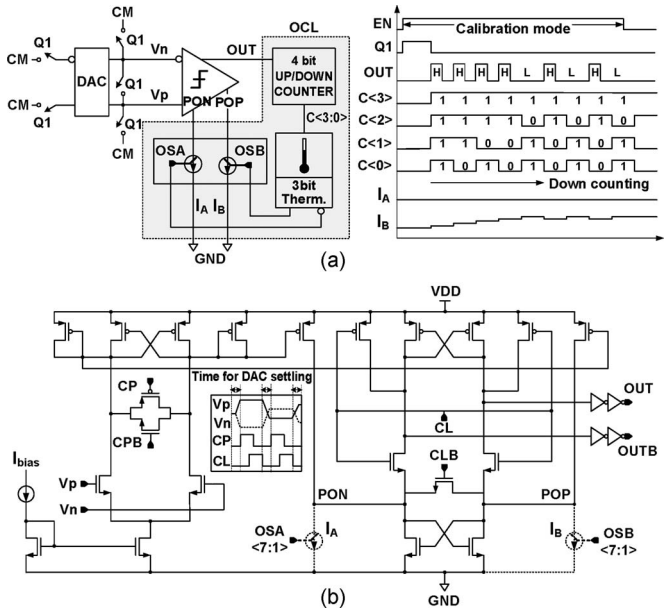

Fig. 4. Foreground offset cancellation scheme with the comparator. (a) Block and timing diagrams of the offset cancellation. (b) Comparator circuit.

steps, which is connected to the internal node of the comparator, and the 1-bit MSB is used to hold the final value of the 3-bit control signal to prevent a reversal. The operation of the offset cancellation scheme is as follows. If the comparator input has a positive offset voltage, OUT is indicated as high and pulls down the current source I_B according to the down counting. Thus, the node voltage of POP falls, and OUT is indicated as low. This feedback loop effectively cancels the offset voltage of the ADC.

As shown in Fig. 4(b), the dynamic comparator is composed of a preamplifier and a regenerative latch. The preamplifier circuit has a gain of 15 dB with 500 MHz −3-dB bandwidth. The input signal of the comparator can be amplified to about 80% of the settling value. To reduce the comparator recovery time during the preamplification period, the clock scheme of reset switches is proposed. The clock period of the comparator is divided into three phases for the settling of the DAC, preamplifying of the signal (CP), and regeneration of the latch (CL). Different from the conventional clock scheme, the proposed technique uses the time for the DAC settling after the clock signal of the latch. Then, the comparator does not amplify the crossed input signal from the DAC, which helps in reducing the comparator recovery time.

C. ECL

An error correction technique is proposed to prevent the effects of dynamic noise sources such as reference or signal glitches and supply variation. It simply performs a sequence of the LSB redecision and bit-inversion operation after a conventional successive approximation using an additional unit capacitor [not shown in Fig. 1(b)]. The redecision operation is performed with the same switching condition of capacitors at the LSB code decision, and the bit-inversion operation is carried out with the switching of the additional capacitor based

Original Code						Calibration Function
Code	D2	D1	D0	R1	R0	
Ideal case I	0	1	0	0	1	No error
@ R1 error	0	1	0	1	1	No calibration
@ D0 error	0	1	1	0	1	D<2:0> - 1
@ D1 error	0	0	1	1	1	D<2:0> + 1

D0		R1	R0
1	+ 1	1	1
	- 1	0	1

(a)

Original Code						Calibration Function
Code	D2	D1	D0	R1	R0	
Ideal case II	0	1	1	1	0	No error
@ R1 error	0	1	1	0	0	No calibration
@ D0 error	0	1	0	1	0	D<2:0> + 1
@ D2 error	1	0	0	0	0	D<2:0> - 1

D0		R1	R0
0	+ 1	1	0
	- 1	0	0

(b)

Fig. 5. Three-bit examples of the error correction technique. (a) In case of $\mathrm{D0} = 1$. (b) In case of $\mathrm{D0} = 0$.

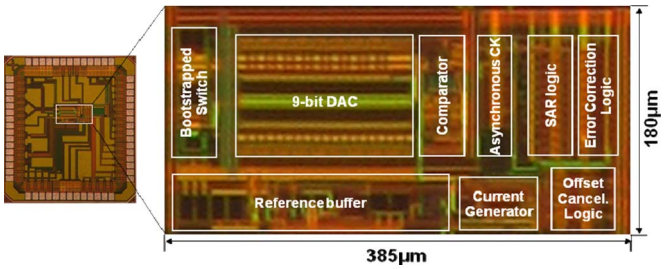

Fig. 6. Die photograph of the prototype ADC.

on the redecision code. Thus, in the ideal case (no error), the redecision code (R1) is identical to the LSB code (D0), and the bit-inversion code (R0) gives a different result to R1.

Fig. 5 shows 3-bit examples of the error correction scheme. If $\mathrm{D0} \neq \mathrm{R1}$ and $\mathrm{R1} = \mathrm{R0}$, the error has occurred in R1, and no action is required. A single decrement or increment of D0 is carried out when $\mathrm{D0} \neq \mathrm{R1}$ and $\mathrm{R1} \neq \mathrm{R0}$. In this case, the error most likely has occurred in D0 because R1 and R0 each have the correct value. If the error took place during previous comparisons of D0, the output digital code will show $\mathrm{D0} = \mathrm{R1} = \mathrm{R0}$. To correct the output code, digital addition or subtraction must be performed on the original code; this was done in an earlier method [13]. Unlike the conventional case, this error correction algorithm is effective for comparison errors not only on MSBs but also on the LSB.

IV. Experimental Results

The proposed ADC is implemented in a 65-nm 1P6M CMOS process with metal–oxide–metal capacitors. Fig. 6 shows the die photo and its active area. The active area of the ADC occupies 0.068 mm^2 with the reference buffer and the current generator. At 80 MS/s, the ADC consumes 3.4 mW from a 1.0-V supply, including 1.7 mW (50%) from the reference buffer and the current generator. The DAC and the comparator use about 21% of the power, and clocks, SAR logic, and ECL use about 29%.

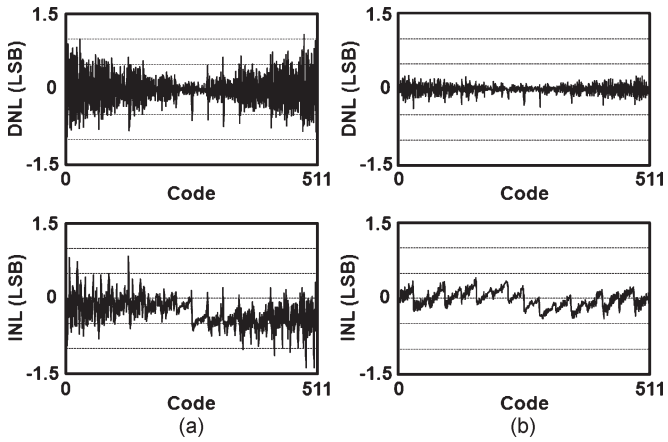

Fig. 7. Measured DNL and INL (a) before calibration and (b) after calibration.

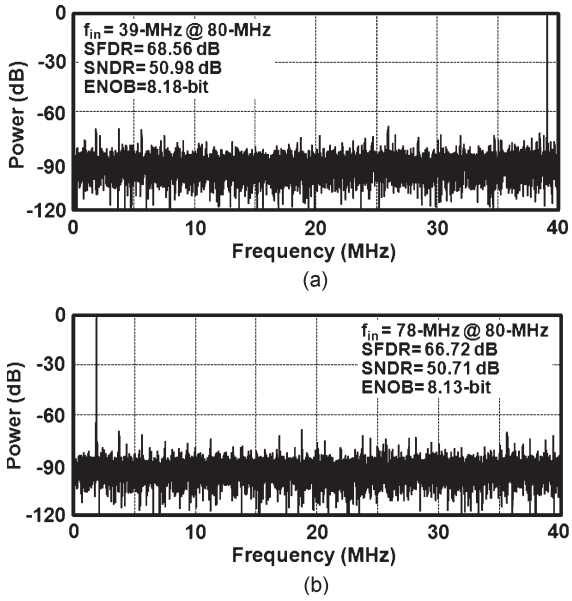

Fig. 8. Measured FFT plots. (a) $f_{\mathrm{in}} = 39$ MHz at $f_s = 80$ MS/s. (b) $f_{\mathrm{in}} = 78$ MHz at $f_s = 80$ MS/s.

Fig. 7 shows measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC before and after error correction at a 9-bit accuracy. The error correction improves the DNL from $+1.10/-0.94$ to $+0.27/-0.37$ LSB, and INL from $+0.84/-1.38$ to $+0.40/-0.40$ LSB. The output spectrum before error correction typically shows larger spurs and harmonics. After error correction, the signal-to-noise-distortion ratio (SNDR) and the measured spurious-free dynamic range (SFDR) are improved by about 3 and 5 dB, respectively.

The measured fast Fourier transform (FFT) spectrums after error correction for input frequencies of 39 and 78 MHz (our test equipment limit) at 80 MS/s are shown in Fig. 8. At the Nyquist frequency, the SFDR is 68.56 dB, and the SNDR is 50.98 dB. At an input frequency of 78 MHz, the ADC achieves an SFDR and an SNDR of 66.72/50.71 dB, and an effective number of bits (ENOB) of 8.13 bits. The overall dynamic performance is summarized in Fig. 9. The dynamic performance is not degraded, as the signal frequency is increased up to two times the Nyquist input bandwidth. The histogram of the

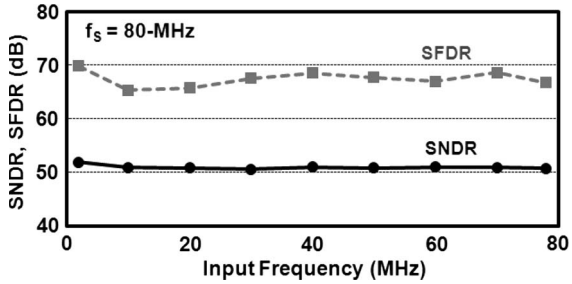

Fig. 9. Dynamic performances versus input frequency.

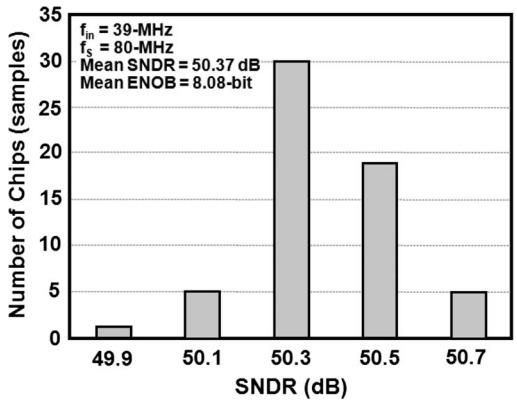

Fig. 10. SNDR distribution of 60 integrated-circuit samples.

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS

Parameters		[9]	[13]	[14]	This work
Process (nm)		65	90	130	65
Resolution (bit)		8	9	10	9
Supply voltage (V)		1.2	1.0	1.2	1.0
Sample rate (MS/s)		50	40	50	80
Input bandwidth (MHz)		50	31	50	78
DNL (LSB)		±0.30	±0.70	±1.00	±0.37
INL (LSB)		±0.30	±0.65	±2.20	±0.40
SFDR (dB)		-	-	60.09	66.72
SNDR (dB)		44.50	~50.28	50.94	50.71
Power (mW)	w/o ref	1.83	0.82	0.92	1.7
	w/ ref	-	-	-	3.4
Area (mm^2)	w/o ref	0.03	0.09	0.08	0.05
	w/ ref	-	-	-	0.07
FOM (fJ/conv. step)	w/o ref	133	50	32	39
	w/ ref	-	-	-	78

measured SNDR of the ADC is shown in Fig. 10. The total sample size is 60. The reliability of the prototype chips is achieved as a mean ENOB of 8.08 bits and a standard deviation of 0.15 bit with a Nyquist input signal at an 80 MHz sampling frequency. A common figure of merit (FOM) [12] is used to compare the ADC performance, which is given as

$$\text{FOM} = \frac{P_w}{2^{\text{ENOB}} \times 2 \times f_{\text{BW}}} \tag{4}$$

where f_{BW} is the effective resolution bandwidth, and P_w is the power consumption of the ADC. The FOMs of the ADC with and without the reference buffer are 78 and 39 fJ/conversion step, respectively. The measured performance summary and comparison are given in Table I.

V. CONCLUSION

A 9-bit 80 MS/s SAR ADC with a capacitor reduction technique has been presented. The MCS technique used in split-capacitor arrays reduces the required number of unit capacitors by about 50% compared with conventional ones. The proposed technique effectively enhances the speed, the power consumption, and the chip area of the ADC. Also, the presented ADC includes a comparator with offset cancellation and uses digital calibration for error correction. The prototype ADC with a 78 MHz input at 80 MS/s achieves 8.13 ENOB and an SFDR of 66.72 dB at a 1.0-V supply voltage and dissipates 3.4 mW with the reference buffer. Experimental results have demonstrated that the proposed ADC circuit is suitable for high-speed wireline and wireless communications.

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