Three-Phase Single-Stage Bidirectional CCM Soft-Switching AC–DC Converter With Minimum Switch Count

Jaeyeon Lee, Hyeonju Jeong, Tat-Thang LE, *Member, IEEE*, and Sewan Choi, *Fellow, IEEE*

***Abstract*—In this article, a three-phase single-stage bidirectional ac–dc converter with low component count is proposed. The single-stage structure is configured by integrating a three-phase ac–dc converter and a three-phase dual active bridge converter. The power factor correction and bidirectional power control are performed by adjusting the modulation index of sinusoidal pulse width modulation (SPWM) and phase-shift angle between the primary and secondary bridges. The low-frequency components generated by SPWM are absorbed by fundamental blocking capacitors connected in series with transformer windings, resulting in true high-frequency isolation. The proposed converter can achieve soft-switching of all switching devices even in continuous conduction mode. A 110 Vac, 3 kW, 100 kHz prototype is implemented to validate the proposed concept and demonstrated 95.34% peak efficiency.**

***Index Terms*—Bidirectional operation, high-frequency isolation, single-stage conversion, soft switching.**

I. Introduction

DUE to the increase in energy consumption, the decrease in fossil fuel reserves, and the problem of environmental pollution, there is an increasing need for sustainable and eco-friendly renewable energy sources [1], [2], [3]. Industries such as eco-friendly automobiles or dc microgrid based on distributed resources such as photovoltaic power, wind power, and fuel cells have attracted attention [4], [5]. In these applications, the isolated bidirectional ac–dc converter is used to connect an ac voltage to dc voltage such as batteries for charging and discharging operation [6], [7].

Usually, these ac–dc conversion systems have the two-stage structure, which is composed of a power factor correction (PFC) stage and an isolated dc–dc stage. As the PFC stage, a three-phase pulse-width modulation (PWM) converter is usually used for regulating the dc-link voltage while satisfying input power quality in terms of power factor and total harmonic distortion [8]. As the dc–dc stage, bidirectional isolated dc–dc converters such as the dual active bridge converter or CLLC resonant converter *(CLLC)* resonant converter can be used for regulating output dc voltage or current [9]. However, total system efficiency will be degraded due to twice power conversion and high components count. Also, in the PFC stage, high frequency operation is restricted by hard-switching in continuous conduction mode continuous-conduction-mode (CCM) operation, so there is a limit in reducing ac filter volume.

In response to these concerns, the single-stage structure employing high-frequency isolation has been researched and introduced for overcoming the aforementioned drawbacks of the two-stage structure. The single-stage structure is advantageous in achieving high efficiency and high power density due to its low component count and simple structure.

Matrix-based three-phase DAB converters have been proposed for single-stage three-phase power conversion systems [10]. Improvements over control and modulation strategies of the matrix-based DAB converter have been introduced [6], [11], [12], [13], [14], [15], [16]. However, use of many bidirectional switches increases conduction loss and complexity of control and implementation [17], [18]. Various types of three-phase single-stage ac–dc converters have been researched. A single-stage ac–dc converter with three-state switching cell employs the interleaving technique to reduce current stress of switches. However, it has high switch count and the primary side switches are not able to achieve soft switching [19]. In [20], [21], and [22], three-phase T-type based ac–dc converters using SVPWM are proposed. High current stress associated with single-phase transformer [20] was relieved in [21] by applying three-phase transformer with the asymmetrical operation, and switch count was reduced in [22]. However, soft switching was not mentioned in the T-type-based single-stage ac–dc converters. In [23], isolated bidirectional single-stage converter with soft switching was proposed but needs additional active snubber to suppress the voltage spikes. A reduced switch count converter [24] and integration of PFC inductor with transformer for high power density [25] were proposed, but soft switching of switches cannot be achieved in both primary and secondary sides.

This article proposes a three-phase single-stage bidirectional ac–dc converter with simple structure [26]. The proposed converter has 12 switches, and all switching devices achieve ZVS

Manuscript received 17 April 2022; revised 9 July 2022 and 17 August 2022; accepted 11 September 2022. Date of publication 15 September 2022; date of current version 18 November 2022. This work was supported by the Korea Institute of Energy Technology Evaluation and Planning grant funded by the Korea government under Grant 20212020800020. Recommended for publication by Associate Editor J. Lam. *(Corresponding author: Sewan Choi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3206896.

Digital Object Identifier 10.1109/TPEL.2022.3206896

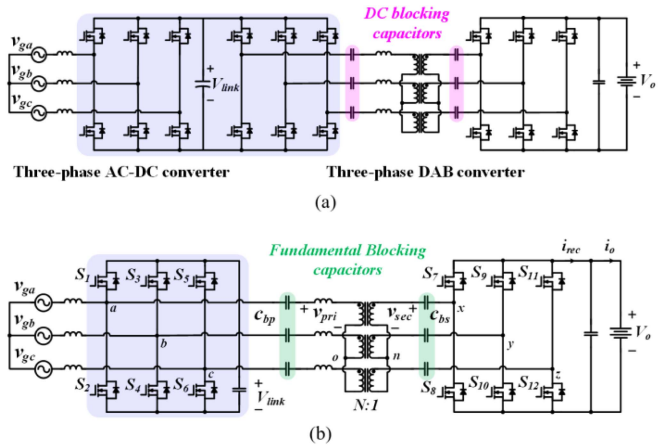

Fig. 1. Topology derivation. (a) Conventional 2-stage structure. (b) Proposed single-stage converter.

turn-ON under CCM operation. A sinusoidal PWM plus phase shift control method is applied to regulate power flow and dc-link voltage. The fundamental components generated by sinusoidal PWM are absorbed by fundamental blocking capacitors, thereby enabling high frequency isolation. The operation principle and modulation strategy of the proposed converter are described in detail.

II. Proposed Single Stage Converter

Fig. 1(a) shows a two-stage structure consisting of the conventional three-phase ac–dc converter and three-phase DAB converter. The proposed single-stage converter is derived by integrating the three-phase ac–dc converter with the primary side of the three-phase DAB converter, as shown in Fig. 1(b). The capacitor C_{bp} and C_{bs} absorb the fundamental component of voltage generated by sinusoidal pulse width modulation (SPWM) so that only high switching frequency component is applied to the transformer, thereby enabling high frequency isolation. Also, due to inherent characteristic of the DAB converter, all switching devices of both the primary and secondary sides achieve ZVS turn-ON.

A. Operating Principles

The SPWM is applied to the primary side converter for regulating the dc-link voltage while shaping the grid current for PFC. The same PWM switching method that was applied to the primary side converter is applied to the secondary side converter, which minimizes the circulating current [19]. The amount and direction of power flow of the proposed converter are controlled by phase-shift angle ϕ of the secondary converter referred to the primary converter. According to the direction of power flow, the operating mode of the proposed converter is divided into two modes: rectifier mode (power flow from ac to dc side $\phi > 0$) and inverter mode (power flow from dc to ac side $\phi < 0$).

For the sake of simplicity, the proposed converter of Fig. 1 can be expressed by the single-phase equivalent circuit as illustrated in Fig. 2. Fig. 2(a) shows the single-phase equivalent circuit at whole frequency range for phase "a" of the proposed converter

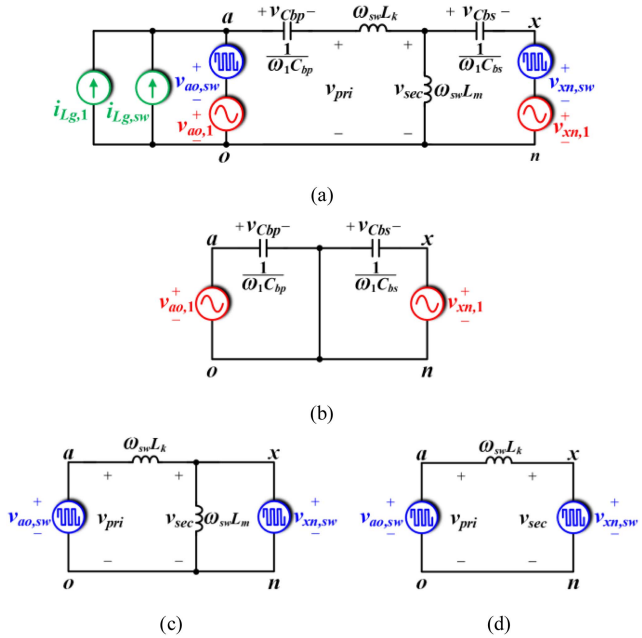

Fig. 2. Single-phase equivalent circuit of phase "a" of the proposed converter. (a) Whole frequency range. (b) Fundamental frequency. (c) Switching frequency. (d) Approximated equivalent circuit.

assuming that the turn ratio of the transformer is unity. The terminal voltages "v_{ao}" and "v_{xn}" across the LC tank consisting of the fundamental blocking capacitors, leakage inductor, and magnetizing inductor are determined by the PWM switching method of the primary and secondary side converters, respectively, and are expressed as sum of their respective fundamental and switching frequency components. The ac grid current i_{Lg} is connected in parallel to the terminal "ao," but does not affect the operation of the LC tank due to its current source nature.

At fundamental frequency, since the impedances of capacitors C_{bp} and C_{bs} are much larger than those of inductors L_k and L_m, only the fundamental components of v_{ao} and v_{xn} are applied to capacitors C_{bp} and C_{bs}, respectively, as shown in Fig. 2(b). It is noted that capacitors C_{bp} and C_{bs} function as fundamental blocking capacitor.

At switching frequency, on the other hand, since the impedances of capacitors C_{bp} and C_{bs} are much smaller than those of inductors L_k and L_m, the capacitors are regarded as short circuit. As a result, the equivalent circuit of the proposed converter can be expressed, as shown in Fig. 2(c), and the proposed converter is capable of achieving high frequency isolation so that the transformer keeps in a small size.

Also, since the impedance of inductor L_m is much larger than that of L_k, magnetizing inductor current is negligible, and magnetizing inductor L_m can be regarded as open circuit, as shown Fig. 2(d). Therefore, like the DAB dc–dc converter, the power transfer of the proposed converter is determined by the phase-shift angle between voltages v_{pri} and v_{sec}.

Based on aforementioned analysis, the theoretical approximate operating waveforms of the proposed converter are shown in Fig. 3. Due to the characteristics of the single-stage ac–dc converter, there are many operation modes. The explanation of

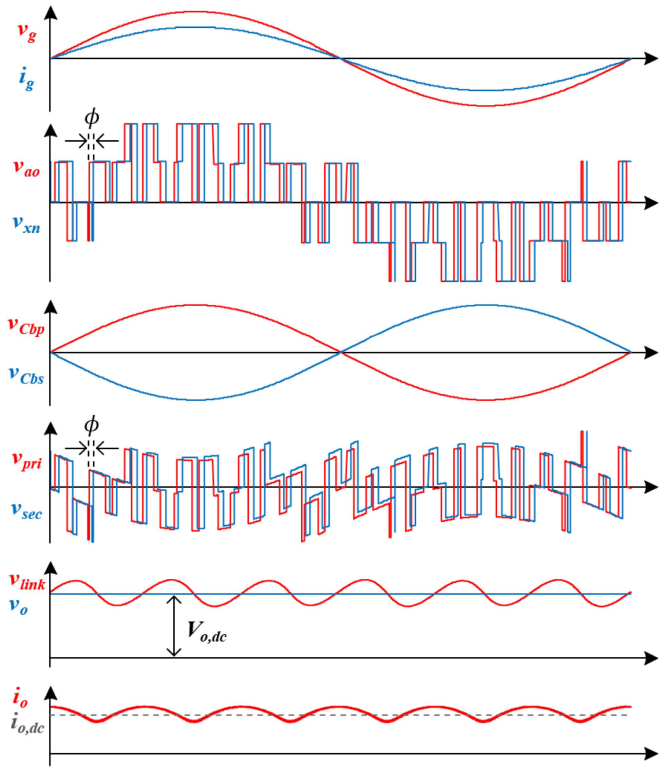

Fig. 3. Operating waveforms under unity power factor and rectifier mode.

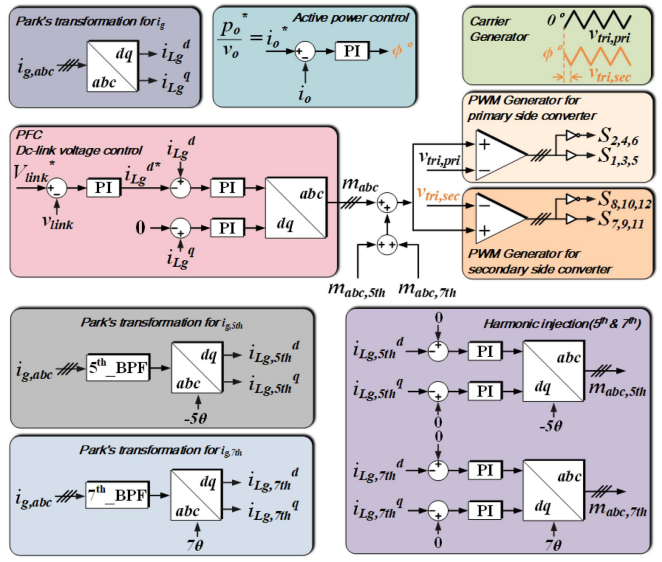

Fig. 4. Control scheme for the proposed single-stage converter.

each operation mode for the three representative points (maximum grid, zero crossing, and minimum grid voltage points) is detailed in Fig. 6 and Section II-C.

B. Modulation Strategy and Control Method

The control objective of the proposed converter is to regulate the power flow while shaping the grid current for PFC. Fig. 4 shows the control block diagram for the proposed converter.

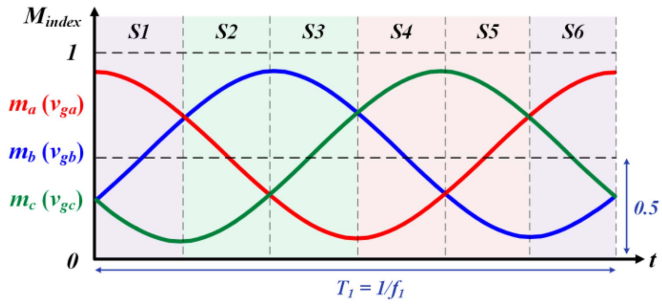

Fig. 5. Waveforms of the proposed converter's three-phase modulation reference (= Duty range: $0 \sim 1$) associated with phase "A".

The dc-link voltage control employs a well-known dual-loop controller to regulate the dc-link voltage (outer-loop) and shape the grid current (inner-loop) simultaneously. The reference value $V_{\mathrm{link}}{}^*$ is obtained by multiplying secondary voltage v_o and turn ratio of the transformer N in order to minimize the circulating current. The dc-link voltage is variably controlled by monitoring the secondary voltage v_o, and the output value obtained through the PI controller of outer-loop is the grid current reference. The *abc-dq* transformation is applied to the sensed three-phase grid current, and the difference with the output value of the outer loop is used for the PI controller. As in a three-phase PFC application, the output value of the inner loop is added to the feedforward duty and converted into an inverse *abc-dq* transform to form the modulating signal m_{abc}. The modulating signals m_{abc} that are generated by the dc-link voltage control part are applied to PWM generators for primary and secondary side switches. The active power (output current i_o) is regulated by phase shifting the carrier signal for the secondary side converter with respect to that for the primary side converter. Additionally, in order to remove the harmonic components generated in the three-phase grid system, the fifth and seventh harmonic components are extracted and inversely injected into the fundamental modulation. This can also be seen in *dq*-axis controller of conventional inverter that are commonly used.

C. Power Equation

This section introduces the power equation of the proposed converter. The output power P_o of the proposed converter is the multiplication of the average voltage and average current of the battery. The average value of rectified current i_{rec} is equal to the sum of average currents of the upper switches of the secondary side. Therefore, the output power P_o is expressed as follows:

$$P_o = V_o I_{rec} = V_o(I_{S7} + I_{S9} + I_{S11}) = 3V_o I_{S7}. \quad (1)$$

To obtain the power equation, the current flowing the switch *S7* must be known. Fig. 5 shows the waveforms of the proposed converter's three-phase modulation references with regards to phase A. Sector (S1 and S6), Sector (S2 and S5), and Sector (S3 and S4) illustrate that the position of phase A is located in the top, the middle, and the bottom of the three-phase modulation references, respectively. The switching patterns belonging to each sector are shown in Fig. 6. In addition, the turn ratio is $\approx$ 1:1, and is shown based on the rectifier mode ($\varphi > 0$, In

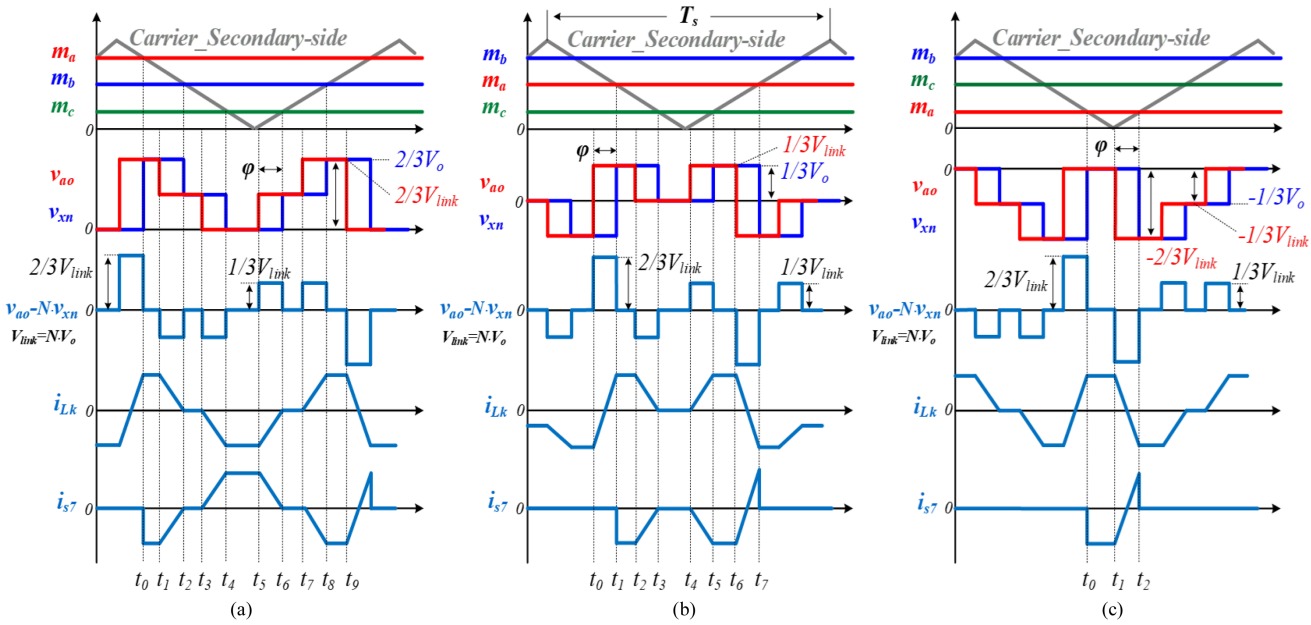

Fig. 6. Key waveforms of the primary side leakage inductor current i_{Lk} and the upper switch current i_{S7} of secondary side (under rectifier mode and Turn ratio = 1:1). (a) Waveforms of Sector S1. (b) Waveforms of Sector S2. (c) Waveforms of Sector S3.

reverse mode, the sign of the phase-shift angle is opposite). Also, the secondary side carrier and the modulation index for the three-phase grid system are shown for representing the upper switch current i_{s7} of secondary side. In order to simplify the analysis of the steady-state operation, it is assumed that only the fundamental frequency component is filtered by fundamental blocking capacitors.

The switching pattern and waveforms of sector S1 and S3 are shown in Fig. 6(a), (c), and Appendix, respectively. The average currents of switch *S7* associated with, respectively, Sector S1 and S3 can be obtained by

$$\begin{aligned} I_{S7,S1} &= -\frac{N}{T_s}\int_{t0}^{t9} i_{Lk}(t)dt \\ &= -\frac{N}{L_k}\left(\frac{\varphi}{2\pi}\right)\frac{V_{\text{link}}}{3}\left(D_{A,S1}-D_{B,S1}-D_{C,S1}+\frac{\varphi}{2\pi}\right)T_s \end{aligned} \tag{2}$$

$$\begin{aligned} I_{S7,S3} &= -\frac{N}{T_s}\int_{t0}^{t2} i_{Lk}(t)dt \\ &= -\frac{N}{L_k}\left(\frac{\varphi}{2\pi}\right)\frac{1}{3}V_{\text{link}}\cdot t_{01} \end{aligned} \tag{3}$$

where $D_{A,S1}$, $D_{B,S1}$, and $D_{C,S1}$ are average values of modulation A, B, and C, respectively, during interval S1. Also, $D_{C,S3}$ is average value of modulation C during interval S3.

Likewise, in Fig. 6(b) and Appendix, the slope of i_{Lk} is determined by difference between v_{ao} and v_{xn}. Current i_{Lk} at each time interval are given as

$$i_{Lk}(t) = \begin{cases} \frac{1}{3}\frac{V_{\text{link}}}{L_k}(t-t_4), & t_4 \le t < t_5 \\ \frac{1}{3}\frac{V_{\text{link}}}{L_k}\cdot\left(\frac{\varphi}{2\pi}\right)\cdot T_s, & t_5 \le t < t_6 \end{cases} \tag{4}$$

where each time interval can be obtained and shown in Fig. 6(b) and Appendix. Therefore, the average current of switch *S7* associated with Sector S2 can be obtained by

$$\begin{aligned} I_{S7,S2} &= -\frac{N}{T_s}\int_{t1}^{t7} i_{Lk}(t)dt \\ &= -\frac{N}{L_k}\left(\frac{\varphi}{2\pi}\right)\frac{2}{3}V_{\text{link}}(t_{56}+0.5t_{45}). \end{aligned} \tag{5}$$

where $D_{A,S2}$ and $D_{B,S2}$ are average values of modulation A and B, respectively, during interval S2.

Therefore, from (1), (3), (4), and (5) the output power P_o can be obtained by

$$P_o = V_o \cdot abs\left(\frac{N}{f_s\cdot L_k}\frac{|\varphi|}{2\pi}\frac{1}{3}V_{\text{link}}\left(1-\frac{|\varphi|}{2\pi}-2D_{B,S2}\right)\right) \tag{6}$$

where $D_{B,S2}$ is the average duty cycle of phase B in Sector S2

$$D_{B,S2} = \frac{3}{\pi}\int_{-\pi/6}^{\pi/6} 0.5\cdot\frac{2V_{g,pk}}{V_{\text{link}}}\cdot\sin(x-120^\circ)+0.5\,dx. \tag{7}$$

The power equation is a quadratic function of the phase shift angle φ. Using (6), the power curve of the proposed converter with respect to the phase-shift angle φ is plotted in Fig. 7. Note that the power is inversely proportional to L_k and f_s. In the rectifier (inverter) mode, the maximum power $P_{\max}$ (-$P_{\max}$) occurs at $\varphi_{\max}$ (-$\varphi_{\max}$).

D. Soft-Switching Characteristics

Due to the characteristics of single-stage ac–dc converter, there are many complex operation modes. However, it is possible to determine whether the soft-switching is achieved for the entire range through the representative operation modes for each range.

The leakage inductor L_k is a critical design parameter that affects soft-switching, current rating, and maximum transferred

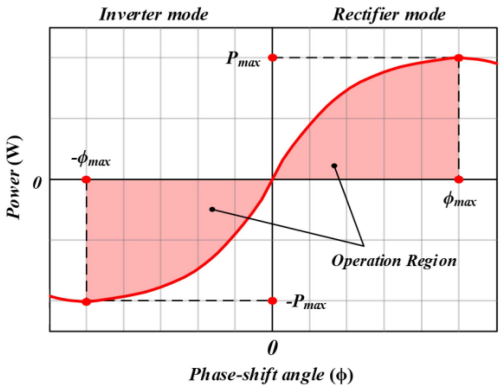

Fig. 7. Power curves versus phase-shift angle.

power. The secondary side switches in the proposed single-stage topology shown in Fig. 1 always achieve ZVS turn-ON in both rectifier and inverter modes under full load operation, such as a DAB dc–dc converter. It means that the proposed topology reduces the transformer series current by variably controlling the primary side PFC stage's dc-link voltage to the same level as the converter's output voltage and achieves ZVS turn-ON for all switches on the secondary side. Therefore, the soft-switching of the secondary side switches is achieved by the transformer series current generated by phase-shift angle, whereas the soft-switching of the primary side switches is determined by the transformer series current and the grid filter inductor current.

As shown in Fig. 8(a), the lower switches current of the primary side is the difference between grid filter inductor current i_g and leakage inductor current i_{Lk} that determine the soft-switching. Also, the lower switches of primary side are prone to failure of ZVS turn-ON at peak grid current points [A and B points of Fig. 8(a)] under light load. Using (2)–(7), Appendix and Fig. 6, three-dimensional graph of i_{Lk} - i_g versus phase-shift angle and leakage inductance L_k is shown in Fig. 8(b). While the upper switches of the primary side always achieve ZVS turn-ON like the switch that does synchronous rectification of the boost converter. Therefore, the design procedure is established at peak grid current point (Sector S1) under rated power based on the switch (the lower side switch when grid current is positive or the upper side switch when grid current is negative) that is prone to soft-switching failure. Due to the symmetrical operation of rectifier and inverter modes, the ZVS turn-ON condition for lower switch S_2 when grid current is positive is the same as that of upper switch S_1 when the grid current is negative. Therefore, only the ZVS condition of S_2 in the rectifier mode is considered for the design of leakage inductance. In the rectifier mode, using (2)–(7), Appendix and Fig. 6, the ZVS turn-ON current for S_2 can be obtained by

$$i_{S2} = i_{Lg}(t) - i_{Lk}(t) = \frac{\sqrt{2} \cdot P_o}{3 \cdot V_g} - i_{Lk}(t_4). \tag{8}$$

From (8) and current rating of switch S_7, the ZVS turn-ON current for S_2 and current rating of S_7 according to leakage inductance L_k, can be plotted, as shown in Fig. 8(c). It can be seen that increasing L_k makes the ZVS turn-ON easier, but increases the current rating of S_7. Therefore, considering the current rating

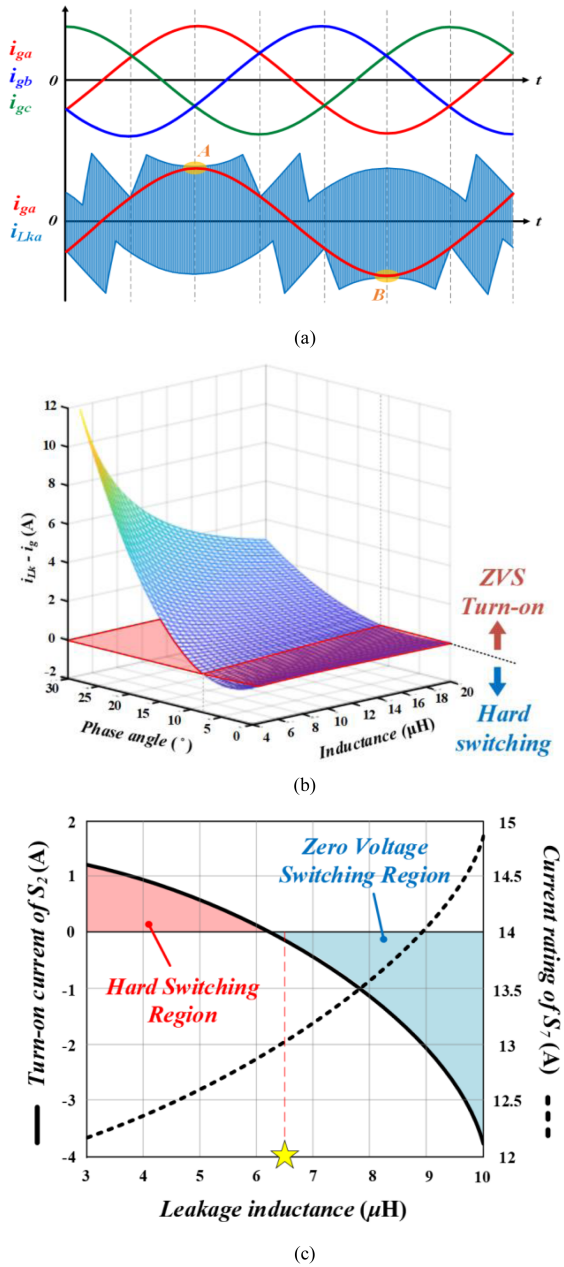

Fig. 8. (a) Representative waveforms i_{Lk} and i_g to determine the soft-switching. (b) $i_{Lk} - i_g$ versus phase-shift angle and leakage inductance L_k. (c) Turn-ON current of lower switches of the primary side versus leakage inductance at positive grid current and current rating of switches of the secondary side under $P_o = 3$ kW, $V_o = 400$ V.

and soft-switching range, the leakage inductance L_k is selected to be 6.5 μH.

III. Design Guideline for Passive Components

In this section, a design guideline of the proposed converter is presented. The following converter specifications are considered in the design: battery voltage $V_o = 400$ V, link voltage $V_{\text{link}} = 400$ V, input voltage $V_g = 110$ Vac, output power $P_o = 3$ kW, and switching frequency $f_s = 100$ kHz.

TABLE I
SWITCHING FREQUENCY MODULATION INDEX ACCORDING TO FUNDAMENTAL FREQUENCY MODULATION [32]

Harmonic \ m_a	0.2	0.4	0.4	0.8	1.0
1 Fundamental	0.2	0.4	0.6	0.8	1.0
Switching freq. ($m_{a,sw}$)	1.242	1.15	1.006	0.818	0.601

Note: $m_a = v_{grid,peak} / \frac{1}{2} v_{link}$

A. Filter Inductor

The grid side ac–dc converter generates harmonics at the switching frequency and nearby frequencies due to PWM operation. In order to satisfy IEEE 1547 [27] regulations, the switching frequency ripple is designed to 5%, then the value of filter inductor L_g is calculated to be 210 μH referring to [28]

$$L_g = \frac{3 \cdot m_{a,sw} \cdot V_{\text{link}} \cdot V_g}{2\sqrt{2} \cdot \omega_{sw} \cdot r_{Lg} \cdot P_o} \tag{9}$$

where $m_{a,sw}$ is the switching frequency modulation index according to fundamental frequency modulation m_a that shown in Table I [32].

B. Leakage Inductor

In Section II-D, leakage inductor value L_k was chosen to be 6.5 μH from Fig. 8(c), considering current rating of switch and ZVS turn-ON under rated power and peak grid current point.

C. Fundamental Blocking Capacitor and Magnetizing Inductor

For design of fundamental blocking capacitors C_{bp} and C_{bs}, the proposed converter shown in Fig. 1 can be expressed by equivalent resonant circuit, as illustrated in Fig. 2. From Fig. 2, the transfer function of equivalent circuit and bode-plot of resonant circuit's closed-loop system are shown in Fig. 9. Using the Fig. 9(a), the input voltage V_{ao} to output current I_{Cbs} can be obtained by

$$\frac{I_{Cbs}(s)}{V_{ao}(s)} = \frac{1}{s^4 (L_k C_{bp} C_{bs} L_m) + s^2 (L_m C_{bs} + L_m C_{bp} + L_k C_{bp}) + 1}. \tag{10}$$

From (10), we know that the proposed converter has two resonant frequencies and can be expressed by

$$f_{r1} = \frac{1}{2\pi\sqrt{L_m \cdot (C_{bp} + C_{bs})}} \tag{11}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{L_k \cdot (C_{bp} // C_{bs})}}. \tag{12}$$

In order to satisfy IEEE 519 [29] and CISPR 25 [30] regulations, the resonant frequencies f_{r1} and f_{r2} are selected to be 3 kHz and 73 kHz, which are 50 times the grid frequency and half of the starting frequency value of the EMI frequency range (150 kHz–30 MHz), respectively.

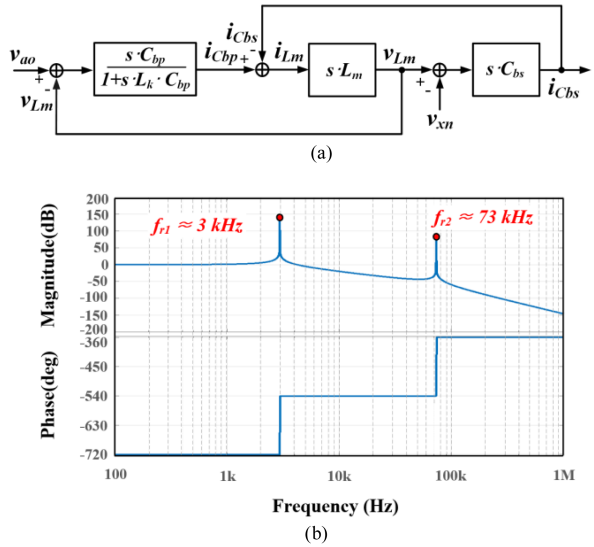

Fig. 9. Transfer function model of transformer and fundamental blocking capacitors. (a) Block diagram of equivalent circuit. (b) Bode-plot of (a).

TABLE II
COMPARISON OF CONVENTIONAL TWO-STAGE AND PROPOSED SINGLE-STAGE

	Conventional two-stage		Proposed single-stage
Topology	Three-phase AC–DC	Dual active bridge	L-type half-bridge based DAB
Control method	SPWM/SVPWM	Phase-shift	SPWM + Phase-shift
Switch counts / RMS current ratio	6 EA/1.0	8–12 EA/1.0	12 EA/ ≈ 1.5
Switching freq.	≤ 100 kHz	100–200 kHz	≥ 100 kHz
Switching characteristic	ZVS Turn-on under grid half-cycle	ZVS Turn-on under full load	Fully ZVS Turn-on under full load
Peak efficiency	97–98 %	97–98 %	≥ 95 %

Therefore, from Section III and (11) and (12), the fundamental blocking capacitance C_{bp}//C_{bs} and the magnetizing inductance L_m calculated to be 0.75 μF and 1000 μH. Also, C_{bp} and C_{bs} are selected as 1.5 μF and 1.5 μF, respectively.

Note that the magnetizing inductance L_m of the transformer does not play a role in the ZVS turn-ON but has an effect on the resonant frequency f_{r1}.

IV. COMPARATIVE RESULTS

As shown in Table II, the single stage is compared with a three-phase two-level inverter and a single-phase DAB converter, which are typical circuits of the conventional two-stage system. The switch current rating of the proposed topology has approximately 1.5 times compared to the DAB converter switch. However, this is a characteristic of a single-stage circuit, and in the proposed topology, the switch current rating increases due

TABLE III
COMPARISON RESULTS BETWEEN THE PROPOSED CONVERTER AND THE STATE-OF-THE-ART SINGLE-STATE CONVERTERS

Converter	Proposed converter	[19]	[22]	[24]	[25]	[42]
Topology	L-type half-bridge based DAB	Current-fed push-pull based DAB	T-type plus 2-level inverters	Push-pull based diode bridge plus 2-level inverter	Boost half-bridge based DAB	L-type half-bridge based LLC
Bidirectional operation	Possible	Possible	Possible	Possible	Possible	Impossible
Voltage range (Input–Output)	110 Vac /350–450 Vdc	220 Vac/380 Vdc	260 Vac/196 Vdc	33–83Vac /135Vdc	230 Vac/400 Vdc	190–380 Vac /300 Vdc
Switching device counts (Mosfet /Diode)	**12EA/-**	24EA/-	24EA/-	8EA/12EA	12EA/-	12EA/6EA
Link / output capacitor configuration	Both 1-series	Both 1-series	No cap / 1-series	No cap / 1-series	Both 2-Series	Both 1-series
Switching freq. / Rated power	**100 kHz /3 kW**	50 kHz/5 kW	20 kHz/2.4 kW	5 kHz/0.45 kW	35 kHz/8 kW	100 kHz/2 kW
Switching characteristic	**Fully soft-switching**	Pri. side: Hard-switched Sec. side: Soft-switching	Hard-switched	Partial soft-switching	Partial soft-switching	Fully soft-switching
Control scheme	SPWM /Phase-shift angle	SPWM /Phase-shift angle	SVPWM (Unsymmetrical under bidirectional operation)	SVPWM /Phase-shift angle	SPWM /Phase-shift angle	SPWM
Peak efficiency	**95.34 %**	93 %	93 %	90 %	Unable to confirm the efficiency graph	96.3 %

to the sum of the grid inductor current and the leakage inductor current. Even if the current rating increases, the hard-switching problem of the conventional inverter has been solved by using the current (grid inductor current + leakage inductor current) to achieve the soft switching of all switches during the grid one-cycle. Accordingly, in terms of efficiency, the single-stage efficiency can be further increased compared to the integrated efficiency of two stage. And by reducing the number of stages, it has an advantage in terms of the total hardware footprint. Moreover, the single stage can reduce the burden of implementing control that need to take care of both PFC and DAB converter.

The proposed converter is compared to the state-of-the-art single-stage three-phase isolated bidirectional ac–dc converters. The comparison results are summarized in Table III.

Almeida et al. [19] presented the single-stage isolated ac–dc converter with three-state switching cell applying the interleaving technique to reduce the current stress of switches under CCM operation. Due to the use of two control variables, the converter is able to operate in a wide voltage range. Also, a three-phase T-type based single-stage isolated ac–dc converter with symmetric Y-Δ transformers is presented in [22]. Since this converter uses only one transformer and does not need dc-link capacitor unlike most of the single-stage converter, the volume of passive components can be reduced. However, both [19] and [22] have a critical disadvantage of using many switch elements. Besides, the control method of [22] is not symmetrical under bidirectional power flow (not using the phase-shift method), which results in increasing the complexity of the system. On the other hand, the proposed converter, which is L-type half-bridge-based DAB has a simple structure with low switch counts and control strategy.

In [24], the system, which removed dc-link capacitor and reduced active switch count is proposed. Also, the integration of PFC inductor with high-frequency transformer for high power density was proposed in [25]. Both of the converters use low switch counts, but soft-switching is partially achieved in both primary and secondary sides under grid period. Therefore, the converters are operated with limited switching frequency due to the hard switching characteristic. Also, the structure of the dc-link and the output capacitor is a two-series structure. Therefore, in order to obtain the same capacitance used in the proposed topology, at least 2series + 2parallel structures must be used, which inevitably increases the volume. Moreover, Krismer et al. [25] mentioned that the maximum efficiency is 98.5%, but the data on the efficiency graph according to the load and the experimental waveform operated at the rated power cannot be confirmed [25], [36], [37], [38]. Li et al. [42] presented the single-stage converter that is an interleaved L-type half-bridge based on *LLC*. In this topology, all switches involved in power operation achieve fully soft-switching during one-cycle of grid frequency. Thus, this allows high switching frequency ($\geq$100 kHz) operation and achieves the peak efficiency of 96.3% for the system. However, the use of many switches and diodes increase the overall footprint of the system and ancillary gate-driver circuitry, even if the switch conduction loss can be halved by the interleaved switching-method. In addition, the secondary side of topology is composed of diode bridge, making it unsuitable for bidirectional operation.

It is noted that the proposed converter is able to achieve soft-switching increasing the switching frequency over 100 kHz. Moreover, it is sufficiently possible to achieve high power

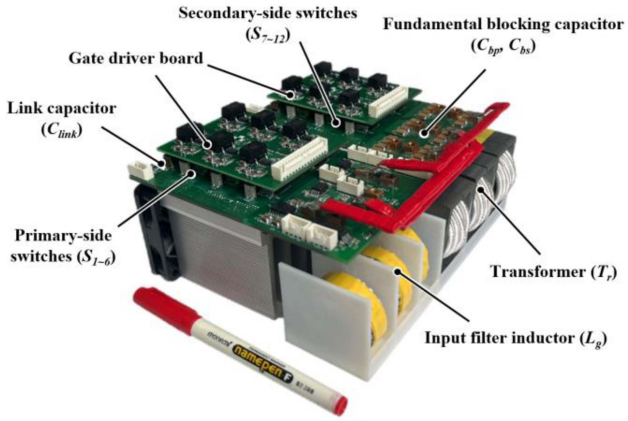

Fig. 10. Photograph of the proposed single-stage converter prototype. (3 kW, 100 kHz, 1.77 kW/L, 170 mm × 147 mm × 68 mm).

TABLE IV
PARAMETER'S RATING AND COMPONENTS

Parameters	Rating		Components
Input filter inductor L_g	*Inductance*	210 μH	High flux CH358125 (CHANGSUNG)
	V_{peak}	402 V	
	I_{rms}	9.2 A	
Switch $S_{1\sim12}$	V_{peak}	465 V	NVBG020N090SC1 (ONSEMI)
	I_{rms}	14.8 A	
DC-Link capacitor C_{link}	*Capacitance*	40 μF	CKG57NX7T2W155M 26EA, (TDK)
	V_{peak}	465 V	
	I_{rms}	10.7 A	
Transformer T_r	L_m *Inductance*	1 mH	Customized core (SAMWHA)
	L_k *Inductance*	6.5 μH	
	Turn ratio	1:1	
Blocking capacitor C_{bp} and C_{bs}	*Capacitance*	1.54 μF	C2220C224KBRACAUTO 7EA, (TDK)
	V_{peak}	210 V	
	I_{rms}	17.8 A	
Output capacitor C_o	*Capacitance*	20 μF	CKG57NX7T2W155M 13EA, (TDK)
	V_{peak}	453 V	
	I_{rms}	11.8 A	

density. Compared to the abovementioned literatures, the proposed converter has shown a good performance due to low component counts and simple structure. Also, by regulating the two control variables, the proposed converter is able to achieve soft-switching and reduce rms current in CCM operation under the wide voltage range.

V. EXPERIMENTAL RESULTS

In order to verify the performance and the theoretical claims of the proposed converter, a 3 kW laboratory prototype was built, as shown in Fig. 10. The proposed experimental results are obtained according to following specification:

1) ac line voltage: $v_g = 110$ Vac;
2) ac voltage frequency: $f_g = 60$ Hz;
3) dc voltage range: 350–450 V;
4) rated output power: 3 kW;
5) switching frequency: $f_s = 100$ kHz.

Components ratings and selected devices of the proposed converter are listed in Table IV. The proposed converter is tested to verify the operating principle, and the experimental results are provided.

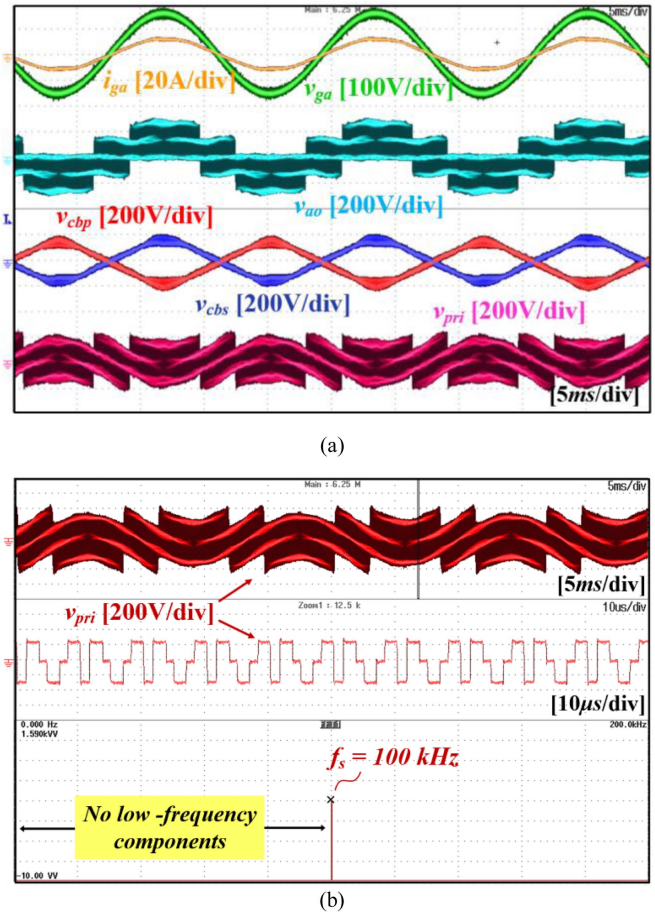

Fig. 11. Experimental waveforms of rectifier mode at V_o= 400 V under 3 kW full load operation condition. (a) Voltages v_{ao}, v_{Cbp}, v_{Cbs}, and v_{pri}. (b) Voltage waveform v_{pri} and FFT of HF transformer.

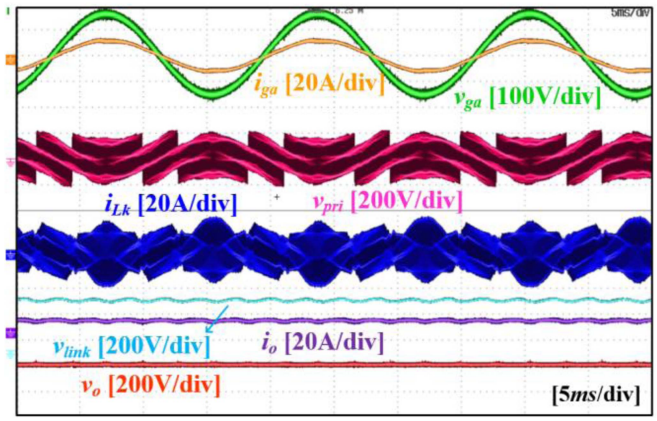

Fig. 12. Experimental waveforms of Rectifier mode at V_o= 400 V under 3 kW full load operation condition: $v_{\rm link}$, i_g, i_o, and i_{Lk}.

Fig. 11(a) shows the experimental waveforms of the proposed bidirectional ac–dc converter at full load for rectifier mode. A near unity power factor of 0.993 and low grid current THD of 3.4% are achieved. As shown in Fig. 11(a), voltages v_{Cbp} and v_{Cbs} contain low frequency components including mainly fundamental component. Therefore, as we can see from Fig. 11(b),

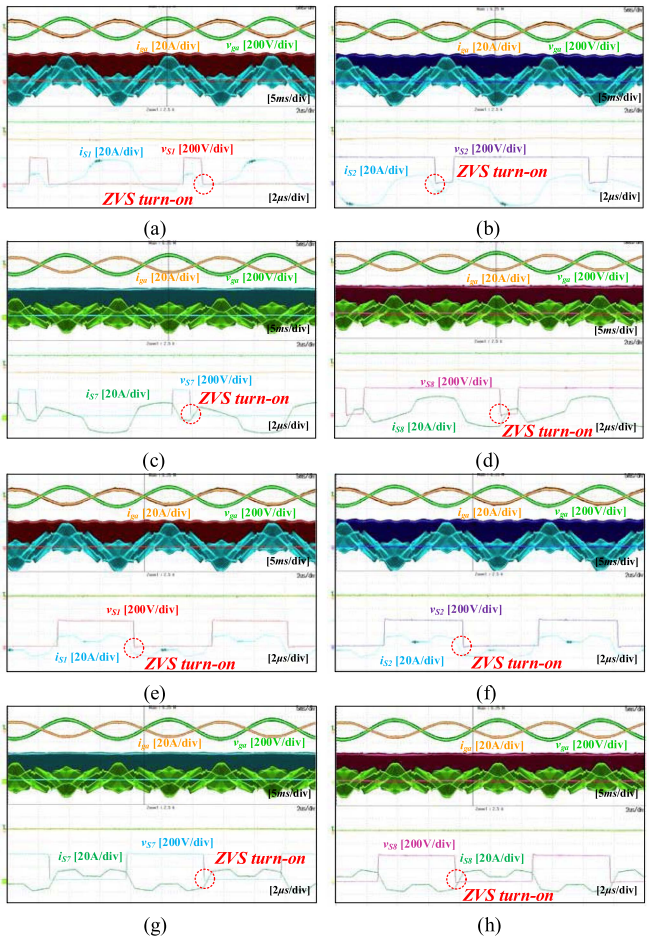

Fig. 13. Experimental waveforms showing ZVS turn ON of switches under V_o = 400 V and P_o = 3 kW operation condition. (a) Switch S_1. (b) Switch S_2. (c) Switch S_7. (d) Switch S_8 at peak grid point. (e) Switch S_1. (f) Switch S_2. (g) Switch S_7. (h) Switch S_8 at zero grid point.

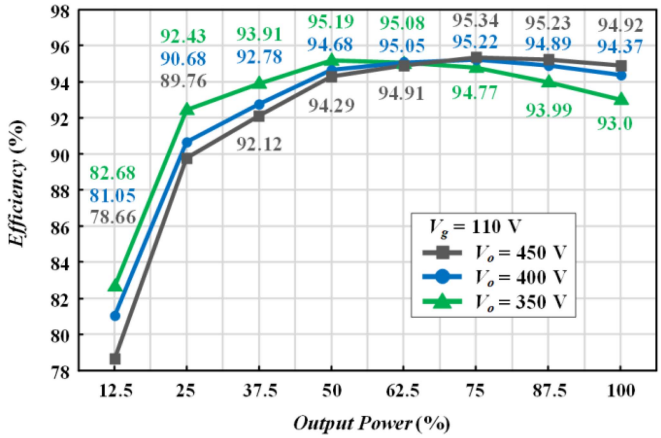

Fig. 14. Measured efficiency of proposed single-stage converter.

the primary voltage of the transformer does not contain any low frequency component, resulting in high-frequency isolation. Fig. 12 shows that the dc-link voltage varies according to the battery voltage, and the battery current i_o mainly includes dc

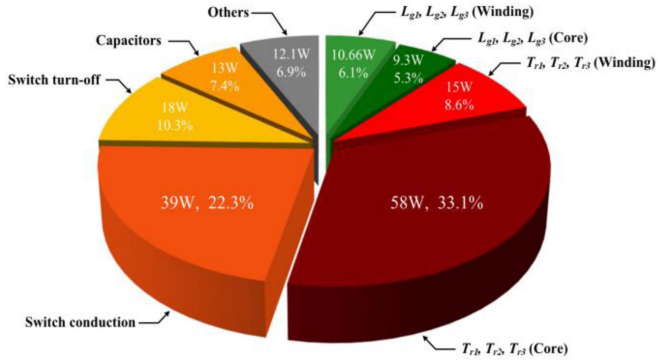

Fig. 15. Loss analysis of proposed single-stage converter at V_g = 110 Vac, V_o = 400 V, P_o = 3 kW, and f_s = 100 kHz. Total loss 175 W.

and sixth harmonic components. The sixth harmonic component (greater than about 10 Hz) in i_o has little effect on the performance of the battery over time [30], [31].

Fig. 13 shows that $S_{1\&2}$ and $S_{7\&8}$ are turned ON with ZVS at peak grid and zero grid points, respectively. Hence, the ZVS turn-ON is maintained in the whole grid period. The other switches perform the same characteristics.

Fig. 14 shows the efficiency curves of the proposed single-stage converter. The measured peak efficiencies of the proposed converter according to different battery voltage 350 V, 400 V, and 450 V are 95.19%, 95.22% and 95.34%, respectively. It should be noted that the efficiencies are greater than 94% at above half power level regardless of the battery voltage.

Fig. 15 shows loss analysis of the proposed converter at full load when V_o = 400 V. The total loss of the proposed converter is 175 W. A large portion of the losses comes from transformer loss (core loss: 58 W, winding loss: 15 W) and switches loss (switching loss: 18 W, conduction loss: 39 W), which are 41.9% and 32.8% of the total loss, respectively.

VI. Conclusion

In this article, a three-phase single-stage bidirectional ac–dc converter with high-frequency isolation is proposed. The key idea was to construct a single-stage structure by intergrating the three-phase ac–dc converter with DAB converter, which helps reduce the component count. The fundamental blocking capacitor absorbs the low-frequency components generated by SPWM. In order to enlarge the ZVS range under the wide voltage, the link voltage v_{ljnk} is regulated to be equal to the output voltage v_o. Moreover, there is no need of electrolytic capacitor, which helps increase the life span and power density of the converter. Experimental results from a 110 Vac, 100 kHz, 3 kW prototype are provided to validate the proposed concept. Using the WT3000, the proposed single-stage converter achieved a peak efficiency of 95.34% and high efficiency under overall load range.

Appendix

Interval formula of Fig. 6(a)–(c), shown at the top of the next page.

$$(a)\begin{cases} t_5-t_4=\left(D_{B,S1}-\left(\frac{\varphi}{360}\right)\right)\cdot T_s \\ t_6-t_5=\left(\frac{\varphi}{360}\right)\cdot T_s \\ t_7-t_6=\left(\frac{D_{C,S1}-D_{B,S1}}{2}-\frac{\varphi}{360}\right)\cdot T_s \\ t_8-t_7=\left(\frac{\varphi}{360}\right)\cdot T_s \\ t_9-t_8=\left(\frac{D_{A,S1}-D_{B,S1}}{2}-\frac{\varphi}{360}\right)\cdot T_s \end{cases} \quad (b)\begin{cases} t_5-t_4=\left(\frac{\varphi}{360}\right)\cdot T_s \\ t_6-t_5=\left(\frac{D_{A,S2}-D_{B,S2}}{2}-\frac{\varphi}{360}\right)\cdot T_s \end{cases}$$

$$(c)\begin{cases} t_1-t_0=\left(D_{A,S3}-\left(\frac{\varphi}{360}\right)\right)\cdot T_s \\ t_2-t_1=\left(\frac{\varphi}{360}\right)\cdot T_s\,\frac{\varphi}{360})\cdot T_s \end{cases}$$

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