An Improved Current-Fed ZVS Isolated Boost Converter for Fuel Cell Applications

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***Abstract*—This paper proposes an improved current-fed zero-voltage switching isolated boost converter suitable for fuel cell applications. Preserving the inherent advantages of the current-fed converter which include smaller input current ripple, lower diode voltage rating, and lower transformer turns ratio, the proposed converter does not require any clamping and start-up circuits unlike the conventional current-fed converters. The voltage ratings of the primary switches and secondary diodes of the proposed converter are significantly reduced. Some alternative schemes of the proposed converter without the voltage–second unbalance are presented. These characteristics of the proposed converter lead to a high overall efficiency over wider load range. Experimental results on a 1 kW prototype are provided to validate the proposed concept.**

***Index Terms*—Current-fed, fuel cells, isolated boost converter, three-phase dc–dc converter, zero-voltage switching (ZVS).**

I. Introduction

SINCE THE dc voltage generated from the fuel cell is usually low and unregulated, it should be boosted and regulated by a front-end dc–dc converter. High-frequency transformers are also involved in the front-end dc–dc converter for high-boost ratio, galvanic isolation, and safety purpose. In summary, the front-end converter required for the fuel cell power generation is characterized by an isolated boost dc–dc converter.

The isolated boost dc–dc converter for the fuel cell applications could be either voltage-fed or current-fed type. The advantages and disadvantages of the two types are detailed in [1] and [2]. Compared to the voltage-fed topology, the current-fed topology exhibits smaller input current ripple, lower diode voltage rating, and lower transformer turns-ratio, in general [3]. Especially, lower transformer turns ratio leads to smaller duty cycle and transformer copper losses, which are important for efficient operation at high power levels. Direct and precise control of the fuel cell current is also possible with the current-fed topology. Therefore, it can be pointed out that the current-fed topology is better suited for the fuel cell applications [1].

Manuscript received December 22, 2009; revised March 5, 2010; accepted April 4, 2010. Date of current version September 17, 2010. Recommended for publication by Associate Editor C. K. Kong.

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Digital Object Identifier 10.1109/TPEL.2010.2048044

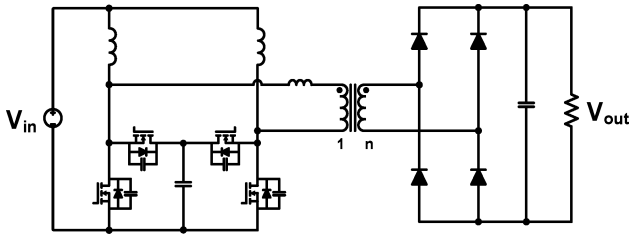

Fig. 1. Conventional L-type half-bridge converter.

There are three basic topologies of isolated current-fed dc–dc converters, namely, full-bridge, push–pull, and L-type half-bridge. Among them, the L-type half-bridge converter, which is shown in Fig. 1, has several advantages over the other topologies.

1) Switch conduction losses are lowest as in the push–pull converter.
2) Transformer utilization is the best in the full-bridge converter.
3) Input current ripple is lowest due to the interleaved operation.
4) Since the transformer turns-ratio of the L-type half-bridge converter is halved, the voltage and the current ratings of the primary winding of the transformer are doubled and halved, respectively.

Therefore, the L-type half-bridge is more suitable to low voltage, high current applications such as front-end dc–dc converters for the fuel cell applications [4].

However, the L-type half-bridge, which is one of the current-fed topologies, has larger switch voltage rating compared to the voltage-fed topology. The L-type half-bridge converter also suffers from high voltage spikes across the switch caused by the leakage inductance of the transformer. Several passive and active clamping methods have been proposed to reduce the voltage spike, but they require additional components and losses.

In this paper, an improved current-fed zero-voltage switching (ZVS) isolated boost converter is proposed for the fuel cell applications. Preserving the advantages of the current-fed converter which include smaller input current ripple, lower diode voltage rating, and lower transformer turns-ratio, the voltage ratings of the primary switches and secondary diodes of the proposed converter are reduced to half of those of the L-type half-bridge converter. Also, the proposed converter does not require clamping and start-up circuits unlike most of the conventional current-fed converter based on full-bridge, push–pull, or half-bridge topologies in which duty ratio is restricted to greater than 0.5, resulting in need of an additional start-up circuitry to prevent the inrush current during the start-up. The operating principle of the proposed converter will be discussed

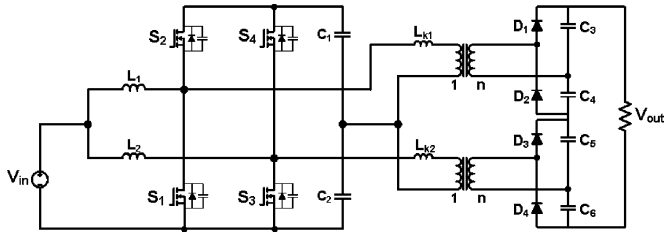

Fig. 2. Proposed isolated boost converter.

in detail. The proposed converter will be compared to the L-type half-bridge converter and experimental results on a 1 kW prototype will also be provided to validate the proposed concept.

II. Operating Principles

As shown in Fig. 2, the proposed isolated boost converter consists of two input filter inductors, four MOSFET switches, two auxiliary capacitors at the low voltage side, and two series connected voltage-doubler rectifiers at the high-voltage side. The topology is basically two high-frequency transformers and two voltage-doubler rectifiers, which are employed for isolation, step-up, and rectification, are connected in series so that the diode-voltage rating becomes half of the output voltage. The ideal voltage-transfer ratio of the proposed converter neglecting the voltage drop across the leakage inductor can be obtained by

$$\frac{V_{\rm out}}{V_{\rm in}} = \frac{2n}{1-D}, \qquad (0 < D < 1). \tag{1}$$

The voltage-transfer ratio of the proposed converter is twice that of the conventional L-type half-bridge converter meaning that the required transformer turn ratio for step-up is reduced to half. This reduces the number of turns of the transformer winding resulting in reduced copper losses and leakage inductance of the transformer. The two legs at the low-voltage side are interleaved with 180° phase shift resulting in reduced input current ripples, and the upper and lower switches of each leg are operated with asymmetrical complementary switching to regulate the output voltage. Fig. 3 shows key waveforms of the proposed converter for illustration of the operating principle. The converter has six operating states within each operating half cycle.

A. Operational Modes

Fig. 4 shows equivalent circuits of the six operating states. It is assumed that the input filter inductance is large enough so that it can be treated as a constant current source during a switching period. It is also assumed that the auxiliary and output capacitances are large enough so that they can be treated as a constant voltage source during a switching period. The average voltages of the auxiliary and output capacitors can be obtained by

$$V_{c1} = \frac{D}{1-D}V_{\rm in}, \qquad V_{c2} = V_{\rm in}, \tag{2}$$

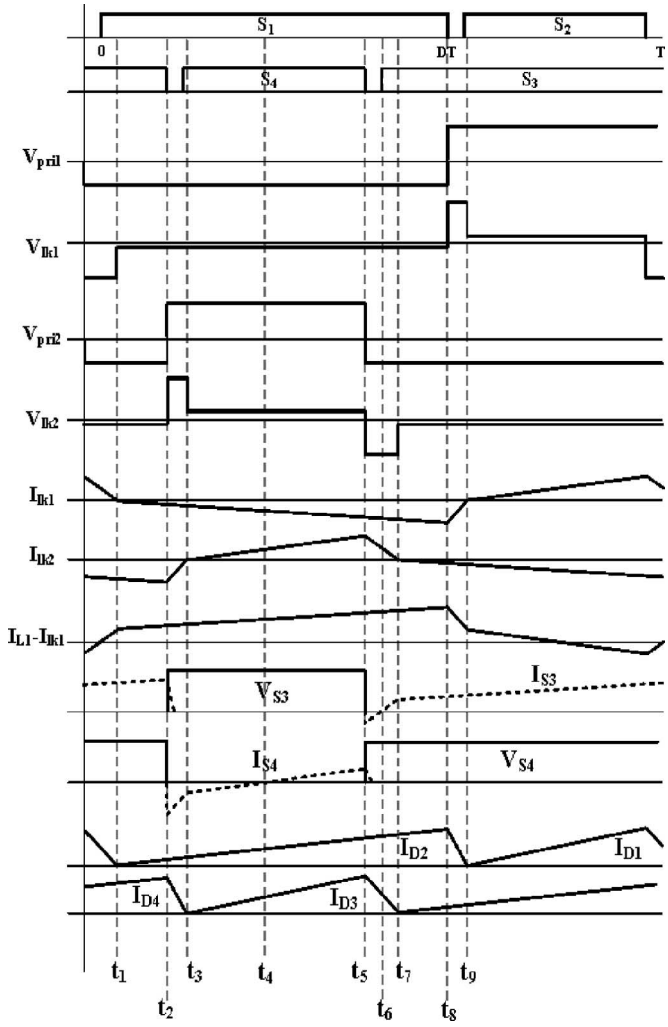

Fig. 3. Key waveforms of the proposed converter.

$$V_{c3} = V_{c5} = \frac{V_{\rm out}}{2}D, \qquad V_{c4} = V_{c6} = \frac{V_{\rm out}}{2}(1-D). \tag{3}$$

1) State 1 [t_1–t_2]: Switches S_1 and S_3 are conducting and each switch carries both the input-inductor current and the leakage-inductor current. The voltage across the leakage inductor of the transformer is a difference between an auxiliary capacitor voltage (V_{c1} or V_{c2}) and an output-capacitor voltage (V_{c3}, V_{c4}, V_{c5}, or V_{c6}) referred to the primary. During this state, the voltages across the leakage inductors can be obtained by

$$V_{\rm lk1} = V_{\rm lk2} = -V_{\rm in} + \frac{V_{\rm out}(1-D)}{2n}. \tag{4}$$

Since voltages across the leakage inductors $V_{\rm lk1}$ and $V_{\rm lk2}$ are small negative values, the leakage-inductor currents are slowly increasing in the direction shown in the equivalent circuit.

2) State 2 [t_2–t_3]: Switch S_3 is turned OFF at t_2, and then parasitic capacitors of switches S_3 and S_4 are charged to $V_{\rm in}/(1-D)V$ and discharged to 0 V, respectively, by current $I_{L2} + I_{\rm lk2}$. After completion of discharge operation, the body diode of S_4 is turned ON, and the current flowing through the body diode of S_4 rapidly decreases since voltage $V_{\rm lk2}$ becomes

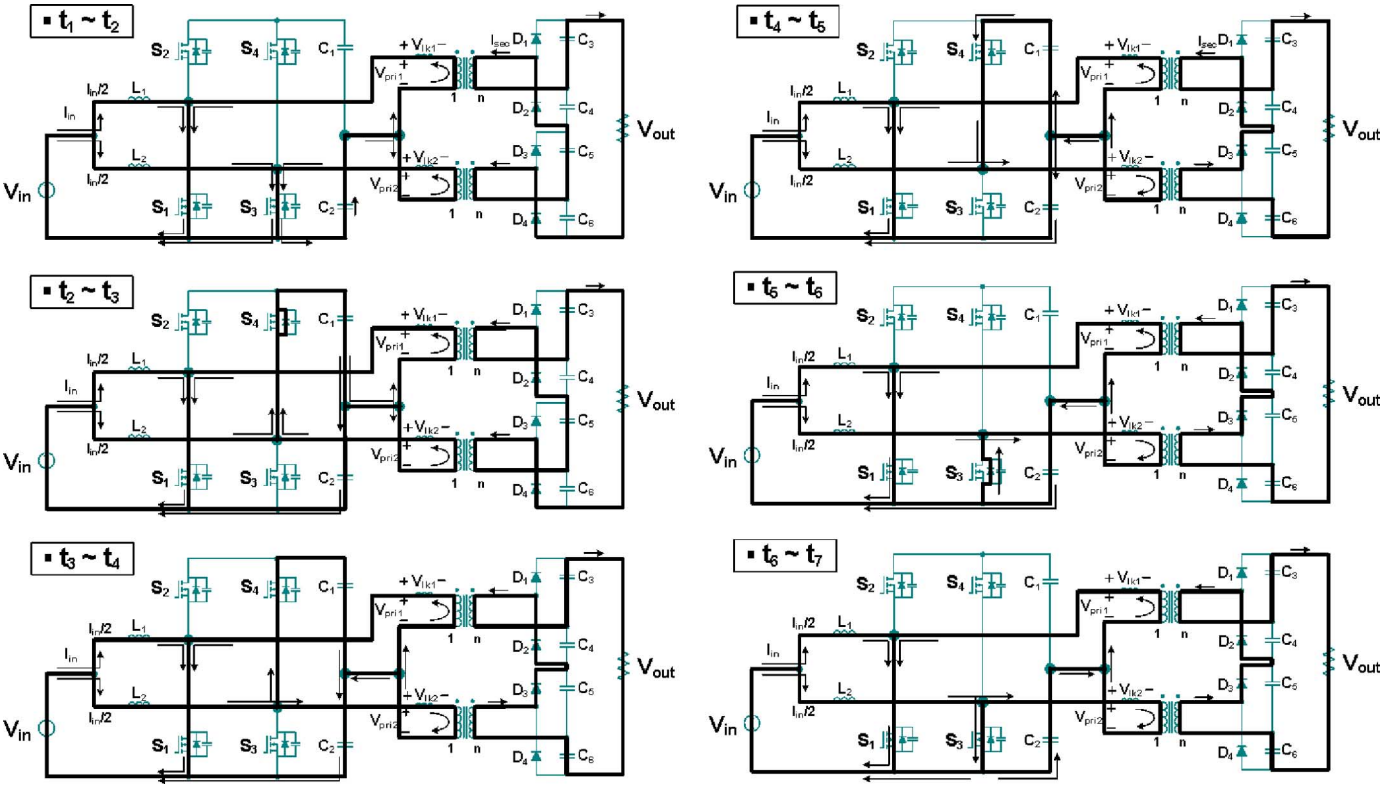

Fig. 4. Operation states of the proposed converter.

large positive as follows:

$$V_{\mathrm{lk2}} = \frac{D}{1-D}V_{\mathrm{in}} + \frac{V_{\mathrm{out}}(1-D)}{2n}. \tag{5}$$

The main channel of S_4 starts conducting at the time the gate signal is applied to S_4. This state ends when current I_{lk2} reaches 0 A.

3) State 3 [t_3–t_4]: Since current I_{lk2} reverses its direction, the diode D_3 is turned ON, and then current I_{lk2} starts slowly increasing due to the small positive value applied across the leakage inductance L_{k2} as follows:

$$V_{\mathrm{lk2}} = \frac{D}{1-D}V_{\mathrm{in}} - \frac{V_{\mathrm{out}}D}{2n}. \tag{6}$$

This state ends when current I_{lk2} becomes equal to I_{L2}, i.e., switch current I_{s4} reaches 0.

4) State 4 [t_4–t_5]: At t_4, the current I_{s4} reverses its direction, and then S_4 is turned ON with ZVS. Current I_{lk2} is continuously increasing with the slope determined at state 3.

5) State 5 [t_5–t_6]: Switch S_4 is turned OFF at t_5, and then parasitic capacitors of switches S_3 and S_4 are discharged to 0 V and charged to $V_{\mathrm{in}}/(1-D)V$, respectively, by current $I_{\mathrm{lk2}} - I_{L2}$. After completion of discharge operation, the body diode of S_3 is turned ON, and the current flowing through the body diode of S_3 rapidly decreases since voltage V_{lk2} becomes large negative as follows:

$$V_{\mathrm{lk2}} = -V_{\mathrm{in}} - \frac{V_{\mathrm{out}}D}{2n}. \tag{7}$$

The main channel of S_3 starts conducting at the time the gate signal is applied to S_3. This state ends when current I_{lk2} becomes equal to I_{L2}, i.e., switch current I_{s3} reaches 0.

6) State 6 [t_6–t_7]: At t_6, the current I_{s3} reverses its direction, and S_3 is turned ON with ZVS. Current I_{lk2} is continuously increasing with the slope determined at state 5. This state ends when current I_{lk2} reaches 0 A. This is the end of a half cycle. The other half cycle begins at time t_7 and is repeated except with the correspondingly opposite set of legs.

B. ZVS Conditions

As explained in state 2, the parasitic capacitor of upper switch S_4 is discharged by the current magnitude $I_1 = I_{L2} + I_{\mathrm{lk2}}$ at time t_2, as shown in Fig. 5. To ensure the ZVS turn ON of switch S_4, the following condition should be satisfied:

$$\frac{1}{2}L_2 I_{L2(\max)}^2 + \frac{1}{2}L_{k2} I_{\mathrm{lk2}(\max)}^2 > C_{\mathrm{oss}}\left(\frac{V_{\mathrm{in}}}{1-D}\right)^2 \tag{8}$$

where

$$I_{L2(\max)} = \frac{1}{2}\left(\frac{P_o}{V_{\mathrm{in}}} + \frac{V_{\mathrm{in}}D}{L_1 f_s}\right) \tag{9}$$

$$I_{\mathrm{lk2}(\max)} = \frac{D\left(V_{\mathrm{in}} - (V_{\mathrm{out}}(1-D)/2n)\right)}{L_{k2} f_s}. \tag{10}$$

Since the design can easily be done such that (8) is satisfied, the ZVS for upper switches S_2 and S_4 is said to be achieved over the whole load range.

As explained in state 5, the parasitic capacitor of lower switch S_3 is discharged by current magnitude $I_2 = I_{\mathrm{lk2}} - I_{L2}$ at time

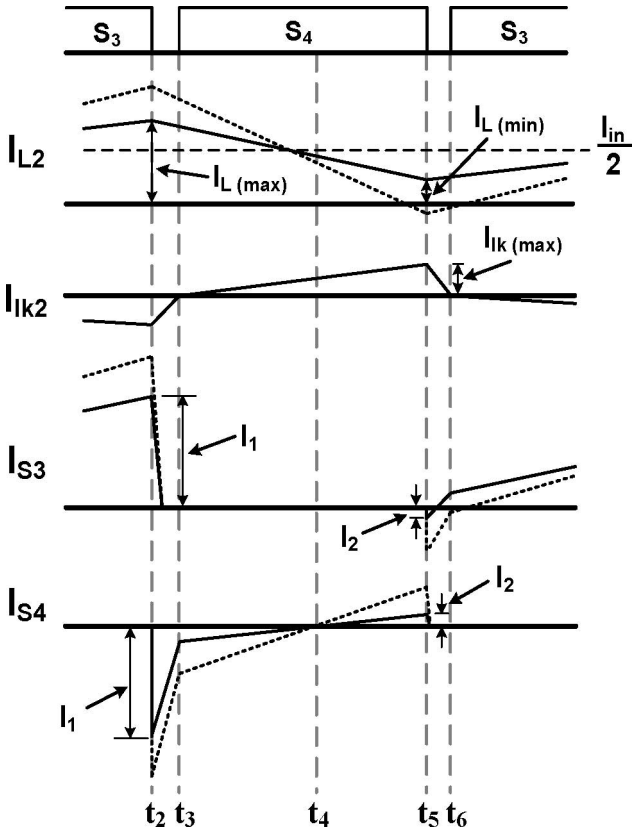

Fig. 5. Detailed current waveforms illustrating enlargement of ZVS region by reduction of input filter inductance.

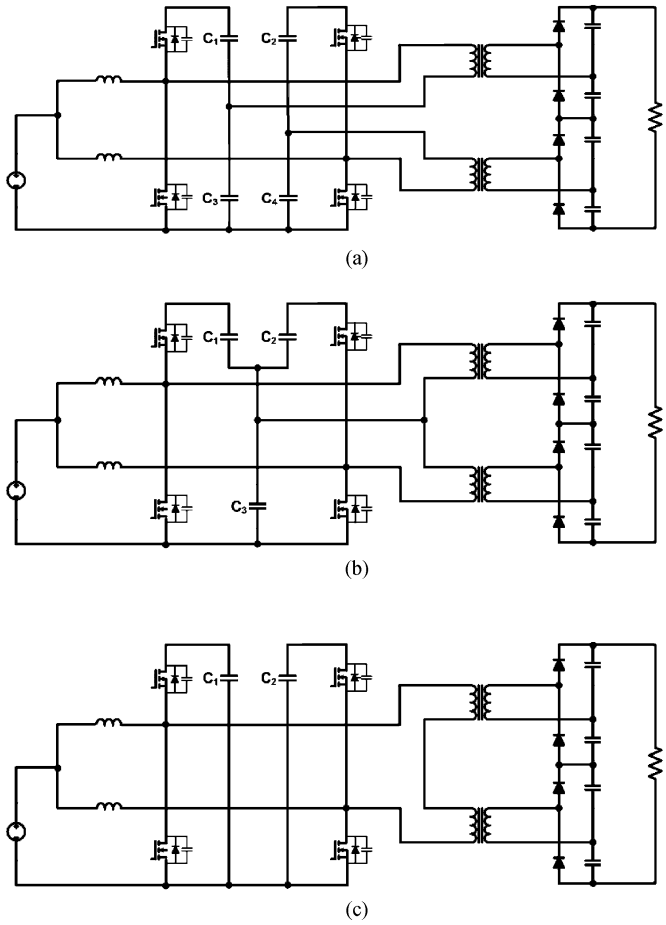

Fig. 6. Alternative schemes of the proposed converter for voltage–second balance of each phase.

t_5. To ensure the ZVS turn ON of switch S_3, the following condition should be satisfied:

$$\frac{1}{2}L_{k2}I_{\mathrm{lk2(max)}}^2 - \frac{1}{2}L_2 I_{L2(\min)}^2 > C_{\mathrm{oss}}\left(\frac{V_{\mathrm{in}}}{1-D}\right)^2 \quad (11)$$

where

$$I_{\mathrm{lk2(max)}} = \frac{D(1-D)\left(\left(V_{\mathrm{in}}/(1-D)\right) - \left(V_{\mathrm{out}}/2n\right)\right)}{L_{k2}f_s} \quad (12)$$

$$I_{L2(\min)} = \frac{1}{2}\left(\frac{P_o}{V_{\mathrm{in}}} - \frac{V_{\mathrm{in}}D}{L_2 f_s}\right). \quad (13)$$

Equation (11) may not be satisfied under the conditions of small transformer-leakage inductance, large input filter inductance and/or heavy load. Increasing transformer leakage inductance to enlarge the ZVS region makes the duty cycle loss large resulting in increased turn ratio. Instead, the input filter inductance can be reduced, and hence current magnitude I_2 can be increased resulting in enlarged ZVS region. Decreasing the input filter inductance increases the current rating of the power devices, and therefore, the input-filter inductance should be properly chosen considering a trade-off between the ZVS region and the device current ratings. To further enlarge the ZVS region, discontinuous conduction mode (DCM) operation on the input-filter inductor may be employed as shown in Fig. 5 meaning that negative current flows on the input-filter inductor. However, this may not be a problem since the design can be done such that the negative filter-inductor current does not cause the negative input current owing to the interleaved operation of the two input filter inductor currents. It should be noted that the ZVS region can be optimized by properly designing the input filter inductance. Further, the proposed converter does not need additional clamping and/or snubber circuits at both the primary and the secondary sides since the ZVS turn ON by complementary switching does not interrupt the current flowing through the leakage inductor.

The turn-OFF switching loss may not be negligible, even though a MOSFET is used as a switch, since the current conducting through it could be considerably large in this low-voltage high-current application. A small external capacitor can be added across the switch to reduce the increased rate of the switch voltage so that the turn-OFF switching loss can be reduced.

C. Alternative Schemes

The primary side of the proposed isolated dc–dc converter is a conventional interleaved boost converter with two phases except the upper switches that replace the diodes. The two-phase interleaved converter is operated in continuous conduction mode (CCM), and the current sharing between the two parallel paths should be taken into account. In practice, the mismatch in duty cycles is inevitable due to the parameter's difference of the

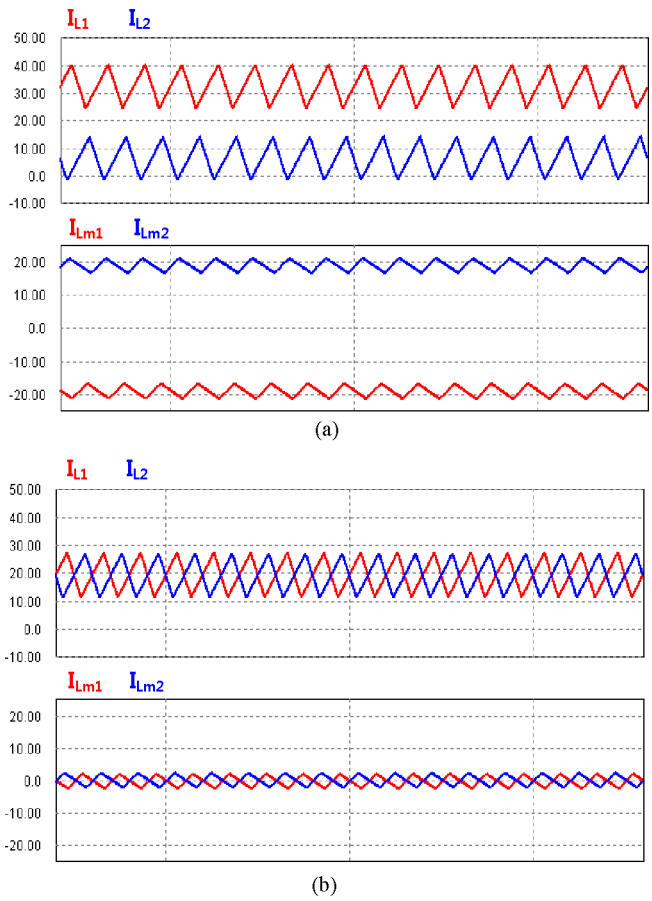

Fig. 7. Simulation results illustrating the voltage–second balance issue of the proposed converter with 1% difference in duty cycle (a) original scheme (see Fig. 2) and (b) alternative scheme [see Fig. 6(b)].

drive circuits and the power switches. According to the voltage–second balance, when different duty cycles are applied to two phases of the paralleled converter, the phase with a smaller duty cycle will go into DCM, while the other phase will be operated in CCM taking up the rest of the load current [9]. Therefore, the proposed scheme of Fig. 2 also may have this problem. Some current sharing control using a couple of current sensors may have to be taken in order to remedy unbalance between two phase legs. However, there are some applications where the voltage control is sufficient if the fast dynamic response is not necessarily required. Fig. 6 shows some alternative schemes of the proposed converter in which current sharing control is not necessary since the aforementioned problem arising from the voltage–second unbalance does not occur even under the duty cycle mismatch or difference in circuit parameters. This is done by using separate output capacitors for each phase, and therefore, the voltage–second balance can always be satisfied in the steady-state condition.

Fig. 7(a) and (b) shows the simulation results of the original proposed scheme (see Fig. 2) and the alternative scheme [see Fig. 6(b)], respectively, when the gate signal with 1% difference in duty cycle is applied. In Fig. 7(a), due to the voltage–second unbalance of a phase, the two-inductor currents exhibit severe unbalance with one phase operated in CCM and the other phase

TABLE I
ENERGY VOLUME OF AUXILIARY CAPACITORS FOR EACH SCHEMES

	Type	I (Fig. 2)	II (Fig. 6 (c))	III (Fig. 6 (b))	IV (Fig. 6 (a))
C_1	Equation	$C\cdot\left(\frac{D}{1-D}\cdot V_{in}\right)^2$	$C\cdot\left(\frac{V_{in}}{1-D}\right)^2$	$C\cdot\left(\frac{D}{1-D}\cdot V_{in}\right)^2$	$C\cdot\left(\frac{D}{1-D}\cdot V_{in}\right)^2$
	PU	0.06	0.18	0.06	0.06
C_2	Equation	$C\cdot V_{in}^2$	$C\cdot\left(\frac{V_{in}}{1-D}\right)^2$	$C\cdot\left(\frac{D}{1-D}\cdot V_{in}\right)^2$	$C\cdot\left(\frac{D}{1-D}\cdot V_{in}\right)^2$
	PU	0.12	0.18	0.06	0.06
C_3	Equation	-	-	$C\cdot V_{in}^2$	$2\cdot C\cdot V_{in}^2$
	PU	-	-	0.12	0.25
C_4	Equation	-	-	-	$2\cdot C\cdot V_{in}^2$
	PU	-	-	-	0.25

TABLE II
COMPONENT RATINGS COMPARISON

Components	Design items		Conventional Converter (Fig. 1)	Proposed Converter (Fig. 2)
Switch	V_{pk}		140 V	90 V
	I_{pk}	Main	60 A	51 A
		Clamp	35 A	
	$P_o/(V_{pk}\cdot I_{pk}\cdot q)$		0.037	0.054
Diode	V_{pk}		400 V	208 V
	I_{pk}		11 A	16 A
	$P_o/(V_{pk}\cdot I_{pk}\cdot q)$		0.056	0.15
Transformer	Turns ratio		1 : 3.5	1 : 2.5
	Primary	V_{rms}	76 V	36.8 V
		I_{rms}	15 A	16.2 A
	Secondary	V_{rms}	265 V	92.2 V
		I_{rms}	4.3 A	6.42 A
	kVA		1140 VA	590 VA x 2
Output Capacitor	Capacitance		5.5 uF	7 uF x 4
	V_{pk}		400 V	139 V
	$CV^2(PU)$		1	0.54
Input Inductor	Inductance		17 uH x 2	13 uH x 2
	I_{rms}		25 A	25 A
	$LI^2(PU)$		1	0.76
Auxiliary Capacitor	Capacitance		7 uF	14 uF x 2
	V_{pk}		140 V	63 V
	$CV^2(PU)$		1	0.81

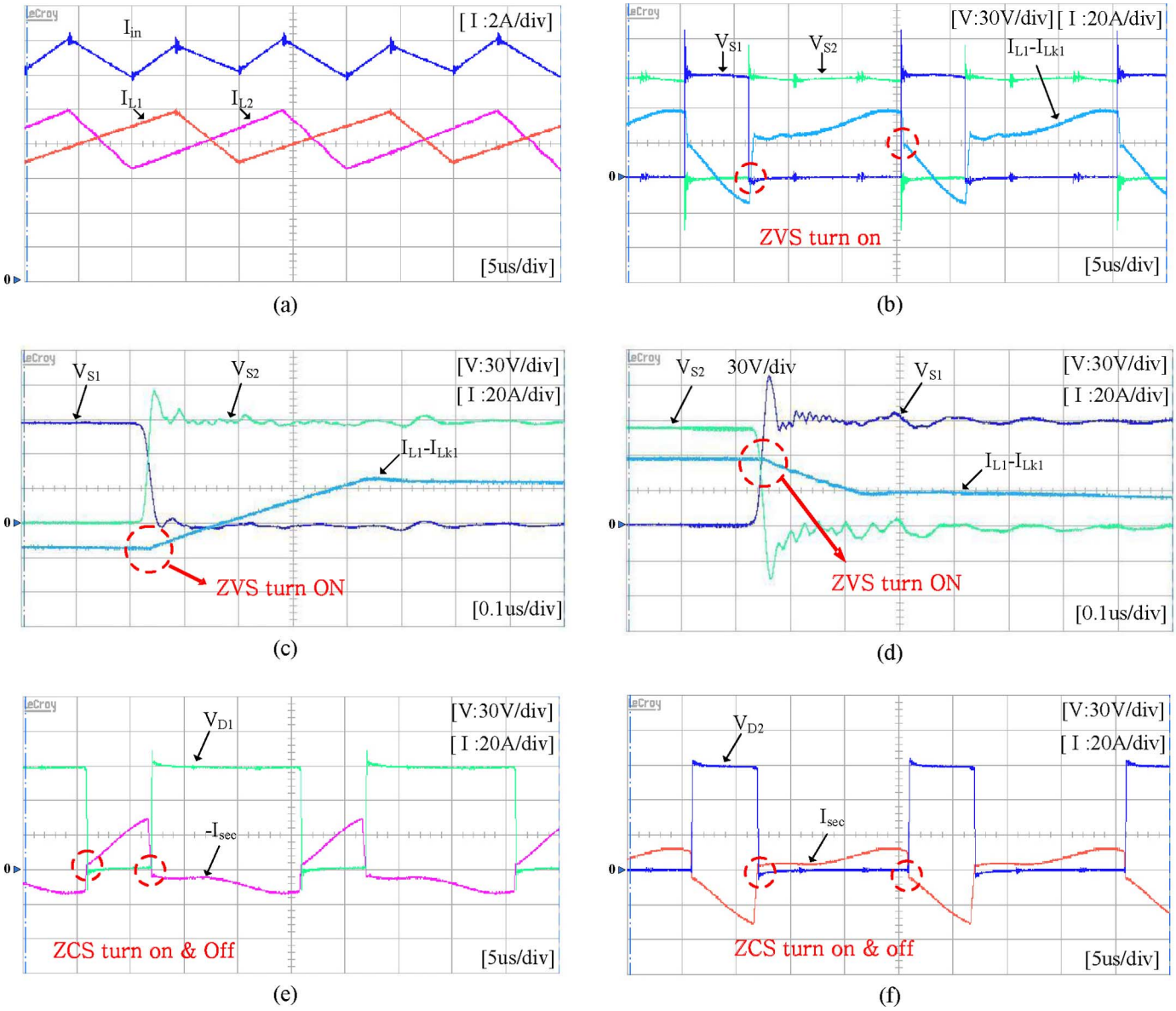

Fig. 8. Experimental waveforms (a) input and inductor currents showing interleaving effect, (b) drain source voltages of S_1, S_2 and $I_{L1} - I_{Lk1}$ (c) extended waveform of (b) showing ZVS turn ON of switch S_1, (d) extended waveform of (b) showing ZVS turn ON of switch S_2, (e) ZCS of diode D_1, and (f) ZCS of diode D_2.

operated in DCM. It should also be noted that the voltage–second unbalance causes not only the unbalanced current in each phase but also a considerable dc offset in magnetizing current of the transformer. However, in Fig. 7(b), it is shown that the unbalance in inductor current is negligible, and also there was no dc offset in magnetizing current.

Table I shows energy volumes of the auxiliary capacitors used in each scheme. Among the alternative schemes, Fig. 6(b) is a choice of topology since it is the best in terms of capacitor energy volume.

III. Performance Comparison

In order to perform a comparison between the proposed converter and the L-type half-bridge converter, both converters have been designed according to the following specifications:

$$P_o = 1\text{ kW}, \quad V_{\text{in}} = 26\text{–}50\text{ V}, \quad V_{\text{out}} = 400\text{ V}$$
$$\Delta I_{\text{in}} = 10\%, \quad \Delta V_{\text{out}} = 3\%, \quad f_s = 50\text{ kHz}.$$

In order to perform a realistic comparative evaluation, the effective duty cycle is determined first, considering switch dead time and duty cycle loss caused by transformer-leakage inductance as follows:

$$D_{\text{eff}} = 1 + D_{\text{deadtime}} - \left(\frac{2nV_{\text{in}}}{V_{\text{out}} + 2nL_k\,(d/dt)\,i_{\text{lk}}} \right). \quad (14)$$

The transformer turns ratio is obtained based on the effective duty cycle, and then the component ratings are calculated. The component ratings of the two converters, according to the design specification, are compared in Table II.

The switch-voltage rating of the proposed converter is half of that of the L-type half-bridge converter so that the MOSFETs with lower $R_{\mathrm{ds(ON)}}$ can be chosen for the proposed converter resulting in significantly reduced conduction losses. The diode-voltage rating of the proposed converter is also half of that of the L-type half-bridge converter due to the series connection of the two voltage-doubler rectifiers. Due to reduced diode-voltage rating, Schottky diodes with low reverse recovery time and forward voltage drop can be used, and therefore, the losses associated with rectifier diodes can be greatly reduced. The proposed converter employs two high frequency transformers connected in series. The total kilovoltampere rating of the proposed converter is almost the same as that of the L-type half-bridge converter, which can slightly increase the total transformer volume, but two transformers not only exhibit better thermal distribution, but also allow low profile. It is also noted that the proposed converter could have smaller size and weight of the passive components such as input inductors, output capacitors, and auxiliary capacitors. The proposed converter employs four output capacitors, but total energy volume of the capacitors are smaller for the proposed converter due to halved capacitor peak voltage.

In general, in order to prevent the inrush current during start-up, a soft-starting technique without any additional circuit can be applied to the voltage-fed converter. This is because the duty cycle of the voltage-fed converter can gradually be increased from 0. Since the duty cycle of the proposed converter also ranges from 0 to 1, no start-up circuitry is required for the proposed converter unlike the conventional isolated current-fed converter based on the push–pull, half-bridge, or full-bridge topologies where some additional start-up circuitry is required to apply the soft starting due to restriction of the duty cycle which should be larger than 0.5. The output voltage of the proposed converter can be regulated by the general voltage such as PI control with output voltage feedback. The dynamic characteristic of the output voltage regulation can also be improved by the current mode control such as peak current control or average current control with additional current feedback.

The quasi-square-wave ZVS turn-OFF technique can be applied to the proposed converter, whereas it cannot be applied to the L-type half-bridge converter.

IV. Experimental Results

A 1 kW laboratory prototype of the proposed converter has been built and tested to verify the operating principle. The system parameters used in the experiment are the same as those in Section III. The transformer is built using PQ40/40 core with the number of turns N_p:N_s = 8:20. The transformer-leakage inductance is 1 μH. A primary switch is implemented with three International Rectifier IRFB4668PbF (200 V, 130 A, 8 mΩ) MOSFETs in parallel.

Schottky diodes of ON Semiconductor MBR40250 (250 V, 40 A) are used for secondary rectifier. Fig. 8 shows experimental waveforms obtained at 1 kW load.

The interleaved inductor and input current are shown in Fig. 8(a). Fig. 8(b) shows the drain-source voltage of switches S_1 and S_2 and current I_{L1}–I_{Lk1}. The extended waveforms of Fig. 8(b) are shown in Fig. 8(c) and (d). It can be seen from Fig. 8(c) and (d) that both lower switch S_1 and upper switch S_2 are being turned ON with ZVS. Fig. 8(e) and (f) shows zero-current switching (ZCS) turn ON and OFF of upper diode D_1 and lower diode D_2, respectively. The measured efficiency of the proposed converter is shown in Fig. 9. The maximum efficiency of 97.8% was measured at 400 W load. The full load efficiency was 94.4%. The photograph of the proposed converter is shown in Fig. 10.

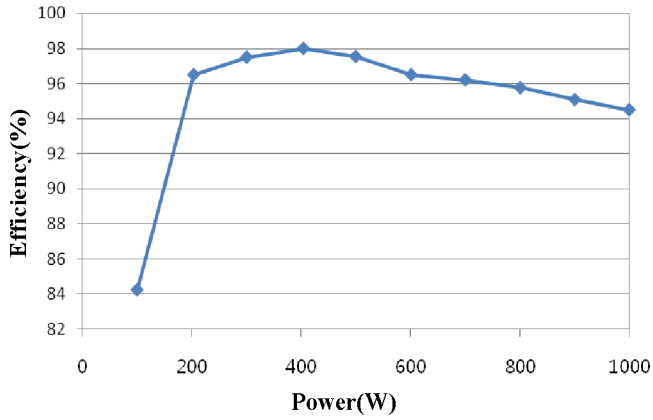

Fig. 9. Measured efficiency (P_o = 1 kW, V_{in} = 26 V, and V_{out} = 400 V).

Fig. 10. Photograph of the proposed converter.

V. Conclusion

In this paper, a new current-fed isolated boost converter has been proposed for low voltage and high current application such as fuel cells. Preserving the advantages of the conventional current-fed converter, which include smaller input current ripple, lower diode voltage rating, and lower transformer turns ratio, the proposed converter has the following advantages over the conventional current-fed converter.

1) Significantly reduced voltage ratings (halved compared to L-type half-bridge) of the switches and diodes, which allow the use of devices with lower $R_{\mathrm{ds(ON)}}$ and t_{rr}, respectively.

2) Reduced size and weight of the passive components such as input filter inductors, auxiliary capacitors, and output capacitors.
3) No clamping or snubber circuits required due to the ZVS operation without interruption of leakage inductor current.
4) No start-up circuitry required for implementation of the soft starting because of duty cycle range between 0 and 1.

These characteristics of the proposed converter lead to higher overall efficiency over wide load range. Experimental results on a 1 kW prototype have been provided to validate the proposed concept.

REFERENCES

[1] X. Kong, L. T. Choi, and A. M. Khambadkone, "Analysis and control of isolated current-fed full bridge converter in fuel cell system," in *Proc. IEEE IECON*, Nov. 2004, vol. 3, pp. 2825–2830.

[2] K. Wang, C. Y. Lin, L. Zhu, D. Qu, F. C. Lee, and J. S. Lai, "Bi-directional DC to DC converters for fuel cell systems," *IEEE Trans. Power Electron.*, vol. 1, pp. 47–51, Oct. 1998.

[3] V. Yakushev, V. Meleshin, and S. Fraidlin, "Full-bridge isolated current fed converter with active clamp," in *Proc. IEEE APEC 1999*, Mar., vol. 1, pp. 560–566.

[4] P. J. Wolfs, "A current-sourced DC–DC converter derived via the duality principle from the half-bridge converter," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 139–144, Feb. 1993.

[5] J. S. Lai, M. Shenck, and K. Stanton, in *Proc. Fuel Cell Seminar*, 2004.

[6] D. Choi, B. Lee, S. Choi, C. Won, and D. Yoo, "A novel power conversion circuit for cost-effective battery-fuel cell hybrid systems," *J. Power Sources*, vol. 152, pp. 245–255, Dec. 2005.

[7] J. S. Lai and D. J. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicles," *Proc. IEEE*, vol. 95, no. 4, pp. 766–777, Apr. 2007.

[8] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional DC–DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[9] D. Wang, X. He, and R. Zhao, "ZVT interleaved boost converters with built-in voltage doubler and current auto-balance characteristic," *IEEE Trans. Ind. Electron.*, vol. 23, no. 6, pp. 2847–2854, Nov. 2008.

[10] M. Zahran, "Design, implementation and testing of HF transformers for satellite EPS applications," *J. Power Electron.*, vol. 8, no. 3, pp. 217–227, Jul. 2008.

[11] S. K. Kwon and K. F. A. Sayed, "Boost-half bridge single power stage PWM DC–DC converters for PEM-fuel cell stacks," *J. Power Electron.*, vol. 8, no. 3, pp. 239–247, Jul. 2008.

[12] C.-E. Kim, G.-W. Moon, and S.-K. Han, "Voltage doubler rectified boost-integrated half bridge (VDRBHB) converter for digital car audio amplifiers," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2321–2330, Nov. 2007.

[13] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phase-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.

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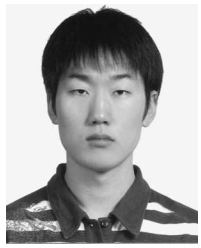

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