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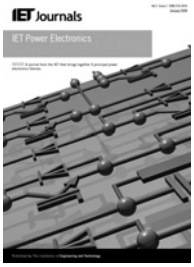

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Analysis, design and experimental results of a floating-output interleaved-input boost-derived DC–DC high-gain transformer-less converter

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Abstract: In transformer-less energy systems sourced from low and unregulated voltage generated by a fuel cell or photovoltaic source, the voltage gain of the power electronic conditioning stage is required to be as high as possible. Although component parasitic elements limit the practically realisable voltage gain of any converter topology, this becomes a critical issue in the case of the basic step-up converter. In this study, a high-gain interleaved boost-derived converter topology is discussed. The proposed converter topology offers modularity, lower ripple for both input current and output voltage, and lower voltage and current ratings of the various circuit elements when compared to the basic boost converter. Analysis, design and key converter waveforms operating in the continuous conduction mode are provided along with design guidelines. Experimental results taken from a 1 kW laboratory prototype operating at 60 kHz are presented to confirm the validity of the analysis and design considerations.

1 Introduction

Renewable and sustainable energy sources such as photovoltaic (PV) and fuel cells (FCs) require power electronic conditioning [1]. The output of the FC or PV cells is typically an unregulated low-level DC voltage that needs to be stepped up to a regulated higher level, for many potential practical applications, and boost converter stages are employed for this purpose. In many applications, the use of a transformer can provide increased output/input voltage gain, as required, as well as isolation and full-bridge based topologies can be used [2]. However, there are a number of applications where transformer-less power electronic energy converter systems could potentially offer significant advantages, including cost and converter size reduction.

For instance, transformer-less grid-connected power electronic energy systems based on PV energy sources have received research effort for some time now [3–8]. DC bus voltages of approximately 200 and 400 V are needed for AC output power at voltage levels of 110 V, 60 Hz or 220 V, 50 Hz, respectively. In the case where a transformer is used for isolation, the transformer ratio can be used as part of the design to boost the voltage of the DC–DC conversion stage to a higher level. When the transformer is omitted, the level of the output voltage is determined only by the duty cycle of the boost converter. In fact, the component parasitic elements limit the practically realisable voltage gain of the boost converter [9]. Also, the actual duty cycle of the basic boost converter is restricted since the current stress of the main switch and diode and the voltage surge associated with diode reverse recovery become severe

as the duty cycle becomes high. Therefore the practically realisable voltage gain of the basic boost converter is not higher than 4 in most cases and it is getting smaller as the required output voltage and power are increased. Therefore high-gain converter topologies are needed to ensure that the input/output voltage levels are practically achievable.

When using multiple energy sources, the use of multilevel converter topologies such as the neutral-point clamped inverter [3] or other topologies can be exploited [4, 5] or for single-source solutions high-gain topologies are needed. For instance, such a high-gain topology was reported in [9] where the converter was based on series-combined connected boost and buck-boost DC–DC converter for power conditioning of the DC voltage provided by the PV energy source [9]. Other combination may be based on buck-boost type of chopper circuits [10, 11]. For grid-connected applications, certain topologies are exposed to leakage currents and this needs to be taken into account when selecting the converter topology [6–8]. Similar issues apply to FC sourced grid-connected energy sources [12].

Transformer-less DC–DC converter topologies with large conversion ratios have been the subject of research in the past few decades, with some interesting topologies presented in the 1980s [13]. The circuits were extensions of the Ćuk converter, and specifically the step-up Ćuk converter incorporated N capacitors that are charged in parallel and discharged in series. However, each extra capacitor requires two extra transistors and one extra diode [13].

An interleaved boost DC–DC converter with large conversion ratio was presented in [14, 15]. The proposed circuit was an extension of the interleaved boost converter incorporating a multistage capacitor multiplier. A 24 Vdc input to 200 Vdc output converter processing 400 W of power, operating at 40 kHz while having efficiency of 95% at full load was reported [14, 15]. A boost switched-capacitor converter with high voltage ratio was also reported in [16]. A switched-capacitor stage was used along with a classical boost converter for achieving high voltage gain. In particular, a 12–120 Vdc output converter processing 35 W of power, operating at 100 kHz, was reported in [17]. A transformer-less DC–DC converter was reported in [18]. In this case, the required high gain of the converter was derived by the parallel connection of two building blocks at the input, which are connected in series at the output. Specifically, the first block is the three-level boost and the two-level buck-boost. The main characteristics of the topology proposed in [18] include single source at the input, transformer-less operation with a gain five times higher than the per unit gain and a DC-link that is split, which offers possibility of independent control [18]. However, this topology exhibits high input current ripples because a boost converter and a buck-boost converter are connected in parallel at the input. The implementation of the controller is also complicated because two different duty cycles, one for each converter, should be generated.

The concept of interleaving at the input also provides an improved performance against high ripple current flowing from the source, and numerous topologies have been discussed in [19–25]. The conventional interleaved converter does not offer higher voltage gain other than the classical boost converter gain and, although the input currents are interleaved, there is only one output capacitor. The proposed converter is interleaved in the input but it also adds two output voltages at the output, and there are two capacitors at the output. The disadvantage of the proposed converter is that it does not offer clear benefits at low values of duty cycles. The classical interleaved converter would not have an issue operating at low duty cycle values.

Other interesting topologies aiming at high gain were reported in [26–35]. For instance, a topology where two boost-converters were connected in parallel at the input from a single source was proposed in [29, 34]. This topology was based on two boost converters and hence it is also known as double-boost converter [34]. In [34] only simulation and theoretical analysis were included. Experimental results, exploring this topology were initially presented in [29] and recently in [35].

The objective of this paper is to generalise the theory associated with paralleling boost type of conventional converters in order to derive new topologies of floating-output that offer a number of advantages including interleaving as well as higher gain for the overall converter. Moreover, the paper offers an analysis and design of the simplest floating-output interleaved-input DC–DC high-gain transformer-less converter topology and its operation is confirmed experimentally with a 1 kW, 60 kHz laboratory prototype.

The paper is organised as follows. Section 2 provides a short discussion for the conventional boost converter topologies and how connections can be used to derive new floating-output topologies including single-switch and multiple converter topologies. Section 3 concentrates on the simplest high-gain interleaved converter topology and provides description of the various modes of operation for the continuous conduction case and key converter operating waveforms. In Section 4 design guidelines for the high-gain interleaved converter are presented and used to design the laboratory prototype. A comparison between the proposed converter and the conventional single-switch boost converter and the conventional two interleaved boost converter is also provided in this Section. Simulated and experimental results are provided in Section 5 and conclusions are summarised in Section 6.

2 Boost derived non-floating/floating output converter topologies

2.1 Single-switch boost converter topologies

The basic boost converter topology is shown in Fig. 1*a*. Fig. 1*b* shows the topology where the inductor is placed on the negative DC-link rail and hence, the output capacitor is floating. This topology requires a positive voltage source at the input and produces a positive floating voltage at the output.

When converter connections are explored for achieving a higher conversion ratio, the floating topologies may have their own place for practical applications and this is the purpose of introducing floating converter versions here. There are more versions for the floating boost converter as shown in Figs. 1*c* and *d*.

2.2 Multiple-converter topologies

In this section, the paper explores connection of converters based on the basic boost topology. For example, connecting two non-floating boost converters in parallel at the input derives the well-known interleaved boost single DC voltage sourced converter as shown in Fig. 2*a* and the floating version is shown in Fig. 2*b*. However, if one wishes to use a single source to power two boost converters but not of the same type, that is, one floating and one non-floating, the derived converter topology is shown in Fig. 3. Analysis and design of a four-leg interleaved converter topology based on the non-floating topology were presented in [27].

2.3 High-gain boost-derived floating-output interleaved converters

The topology discussed in this paper is comprised of two basic boost modules connected in parallel at the input [29, 34, 35]; the non-floating-output version (Module 1, Fig. 1*a*) and the floating-output version (Module 2, Fig. 1*b*) resulting in a floating-output double-boost converter as shown in Fig. 4.

The interleaving concept is guaranteed by the parallel connection of the two modules at the input and the phase-shifted control signals between the two switches (S_1 and

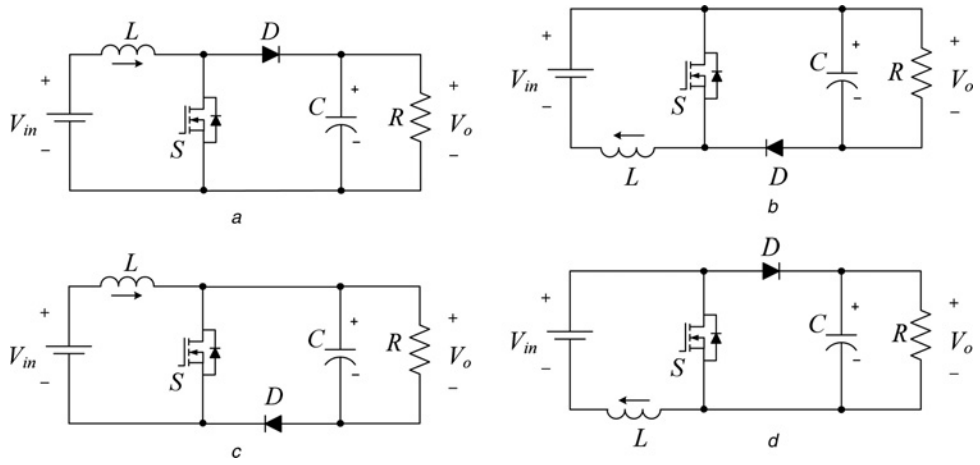

Figure 1 *Boost converter topologies*

a Non-floating boost
b Floating boost and inductor placed on the negative rail
c Floating boost converter topology with the inductor placed on the positive rail
d Floating boost converter topology with the inductor placed on the negative rail and the diode repositioned

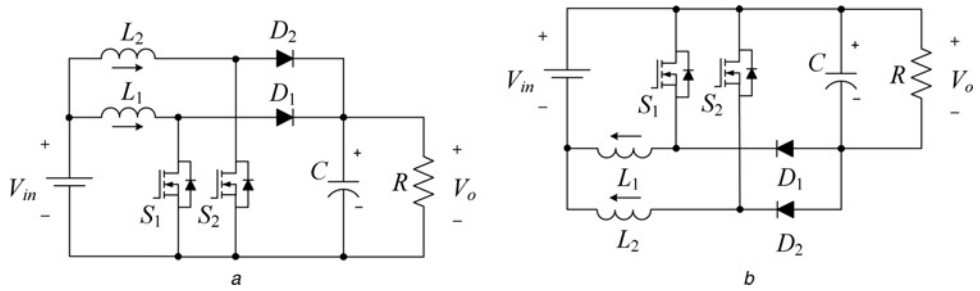

Figure 2 *Paralleling of two basic boost building blocks*

a Non-floating-output type (also known as parallel interleaved boost); resulting topology of the non-floating-output type
b Floating-output type; resulting topology of the floating-output type

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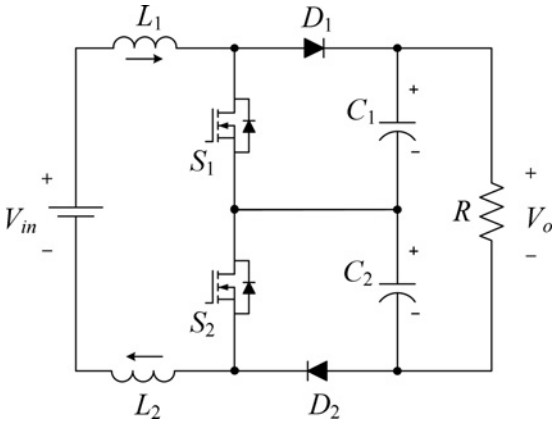

Figure 3 *Series–series connection of the two basic boost building blocks resulting in a floating topology (also known as three-level boost converter)*

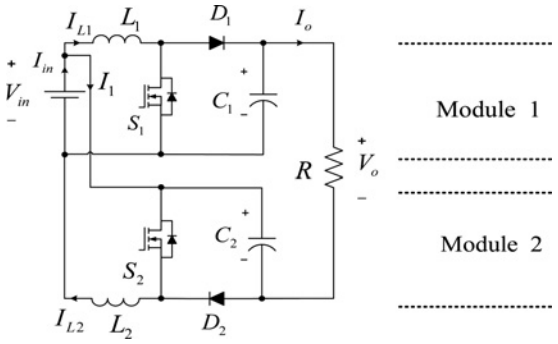

Figure 4 *Floating-output double-boost converter*

S_2). High gain is obtained by the series connection of the two modules at the output with the input source at all times. The series connection at the output results in reduced overall output voltage ripple.

3 High-gain floating double-boost converter

The high-gain transformer-less floating-output double-boost converter topology is shown in Fig. 4. In this section, a description of the various modes of operation of the converter is provided.

Although the operation of the converter is intended for a high voltage gain ratio ($D > 0.5$), the analysis of the converter presented here also considers the operation of the converter when ($D < 0.5$). For the analysis, the power losses are neglected. Since both converters are boost type, it is assumed that the output voltage across each capacitor C_1 and C_2 is higher than the input voltage source voltage V_{in}. It is also assumed that the converter operates in the continuous conduction mode (CCM). The load current is assumed to be ripple free. Both converters have identical duty cycles

$$\text{Duty Cycle 1} = \text{Duty Cycle 2} = D \tag{1}$$

Based on the assumption that both converters have the same duty cycle, it is deduced that the output voltages of each converter are also of the same average value

$$V_{C1} = V_{C2} \tag{2}$$

The key converter operating waveforms are plotted for both the cases when $D < 0.5$ and $D > 0.5$ in Figs. 5*a* and *b*, respectively. The equivalent circuits for the converter modes are presented in Fig. 6.

3.1 Operation for D < 0.5 (Fig. 5a)

The switch S_1 turns on at zero and the switch S_2 turns on at $T_s/2$.

3.1.1 $0 \le t \le t_1$ (S_1 on and S_2 off), Mode I (Fig. 6a): The switch S_1 is on, the switch S_2 is off and the diode D_1 is reversed biased. The inductor L_1 is being charged through the input voltage source voltage V_{in} and the current through the inductor L_1 increases. The current through the inductor L_2 decreases and the voltage across the inductor L_2 is $(-V_{C2} + V_{in})$ as the diode D_2 closes the circuit by becoming forward biased. The load current I_o flows through the capacitor C_1 which is being discharged, and the input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{in}$.

3.1.2 $t_1 \le t \le t_2$ (S_1 off and S_2 off), Mode IV (Fig. 6d): During this mode of operation, both switches S_1 and S_2 are off. The current through the inductors L_1 and L_2 decreases. The voltage across the inductor L_1 is $(-V_{C1} + V_{in})$. The voltage across the inductor L_2 is $(-V_{C2} + V_{in})$. Both the output capacitors are charged and their voltage increases. The input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{in}$.

3.1.3 $t_2 \le t \le t_3$ (S_1 off and S_2 on), Mode III (Fig. 6c): The switch S_1 is off and the switch S_2 is on. The diode D_2 becomes reversed biased. The current through the inductor L_1 keeps decreasing and that through the inductor L_2 starts increasing. The voltage across the inductor L_2 is $+V_{in}$. The voltage across the inductor L_1 is $(-V_{C1} + V_{in})$. The input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{in}$.

3.1.4 $t_3 \le t \le T_s$ (S_1 off and S_2 off), Mode IV (Fig. 6d): Both the switches S_1 and S_2 are off once again and the converter is again in Mode IV as described above. The voltage across the inductor L_1 is $(-V_{C1} + V_{in})$. The voltage across the inductor L_2 is $(-V_{C2} + V_{in})$. Both the output capacitors are charged and their voltage increases.

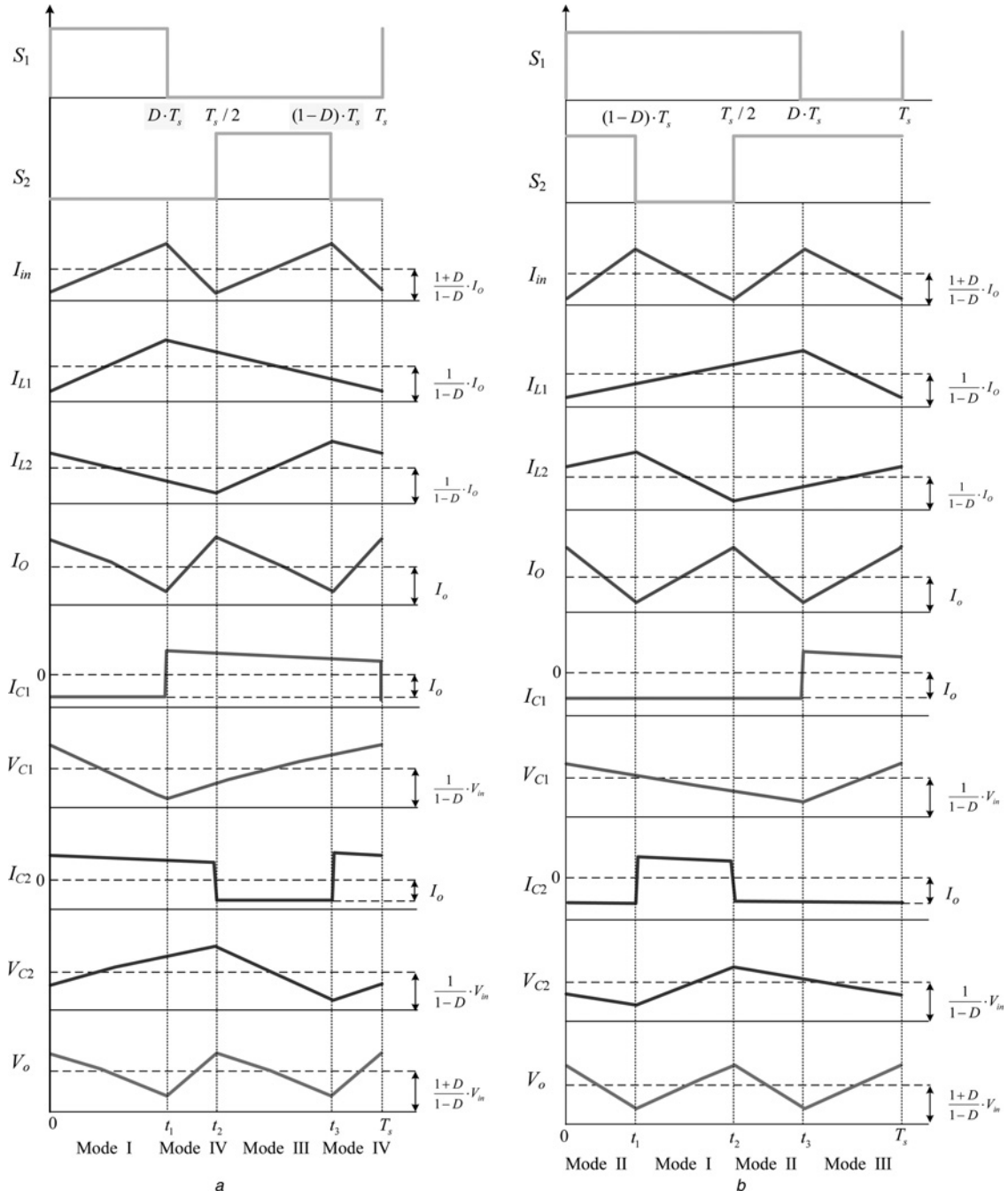

Figure 5 *Key waveforms of the proposed high-gain boost converter*

a $D < 0.5$
b $D > 0.5$

The input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{\text{in}}$.

3.2 Operation for $D > 0.5$ (Fig. 5b)

The switch S_1 turns on at zero and the switch S_2 turns on at $T_s/2$.

3.2.1 $0 \leq t \leq t_1$ (S_1 on and S_2 on), Mode II (Fig. 6b): Both the switches S_1 and S_2 are on. The current through both the inductors L_1 and L_2 increases. The voltage across both the inductors is the input voltage source voltage V_{in}. The input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{\text{in}}$.

3.2.2 $t_1 \leq t \leq t_2$ (S_1 on and S_2 off), Mode I (Fig. 6a): The switch S_1 is on but the switch S_2 is off. Therefore the current through the inductor L_1 increases whereas that through the inductor L_2 decreases. The voltage across the inductor L_1 is V_{in}. The voltage across the inductor L_2 is $(-V_{C2} + V_{\text{in}})$. The input voltage source is in

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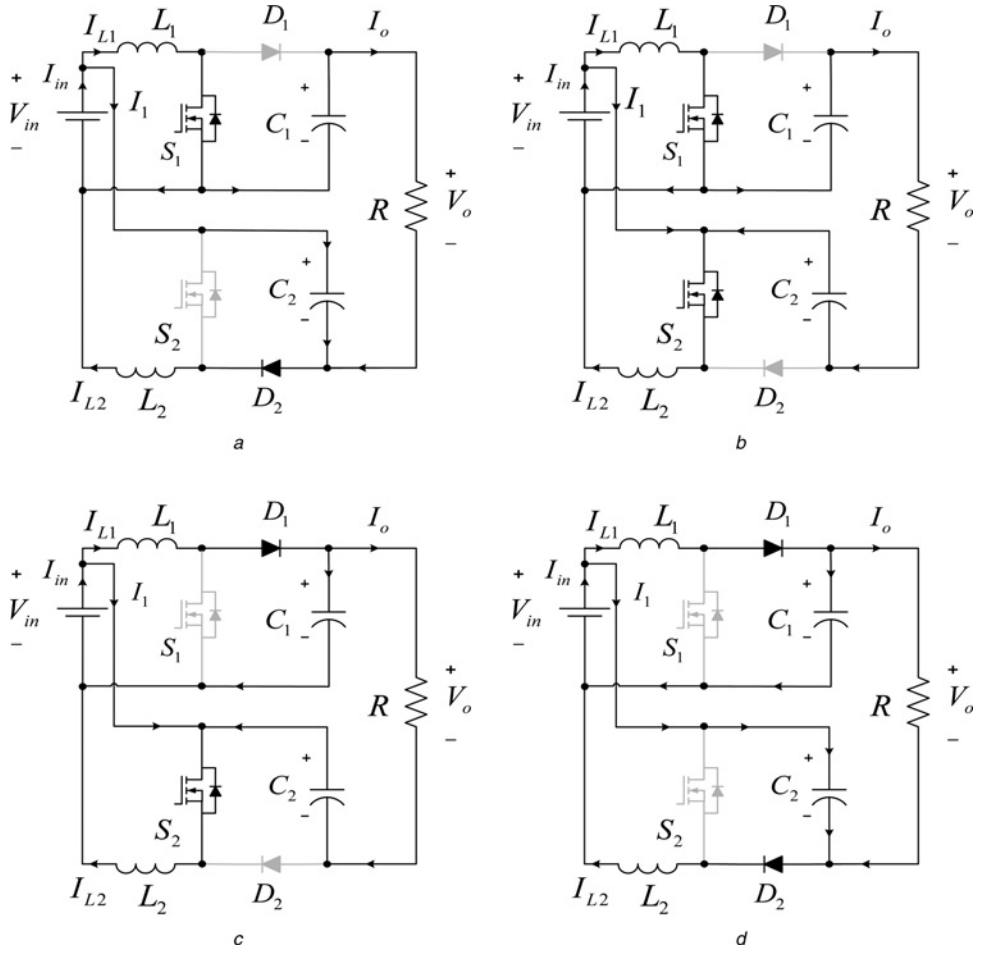

Figure 6 *Operation modes of the proposed converter*

a Mode I
b Mode II
c Mode III
d Mode IV

series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{\text{in}}$.

3.2.3 $t_2 \leq t \leq t_3$ (S_1 on and S_2 on), Mode II (Fig. 6b): Both the switches S_1 and S_2 are on. The current through both the inductors L_1 and L_2 increases and the converter operates in Mode II. The voltage across both the inductors is the input voltage source voltage V_{in}. The input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{\text{in}}$.

3.2.4 $t_3 \leq t \leq T_s$ (S_1 off and S_2 on), Mode III (Fig. 6c): The switch S_1 is off and the switch S_2 is on. The current through both the inductors L_1 and L_2 increases, decreases and increases, respectively. The input voltage source is in series with both the output capacitors and the load voltage is $V_{C1} + V_{C2} - V_{\text{in}}$.

3.3 Converter analysis

Each module operates in the CCM and it is a separate boost converter. Therefore the voltages across the output capacitors C_1 and C_2 can be expressed as

$$V_{C1} = V_{C2} = \frac{1}{1-D} V_{\text{in}} \tag{3}$$

As explained through the description of the various modes of operation, the two output capacitors are always in series with the input voltage source and therefore the output voltage can also be expressed as

$$V_{\text{o}} = V_{C1} + V_{C2} - V_{\text{in}} \tag{4}$$

Therefore the voltage rating of the main switch and diode is determined directly by the input voltage and maximum duty cycle and is much smaller than the output voltage. This allows selection of devices with lower voltage rating, resulting in reduced conduction and switching losses. From (3) and (4), the voltage gain of the proposed converter can be obtained by

$$\frac{V_{\text{o}}}{V_{\text{in}}} = \frac{1+D}{1-D} \tag{5}$$

It should be noted that the voltage gain of the proposed converter is increased compared to that of the basic boost converter. The voltage gain of 4 can be achieved with the duty cycle of $D = 0.6$, which leads to reduced voltage rating and peak current rating of the main switch and diode, resulting in further reduced conduction and switching losses. Applying Kirchhoff's current law on the input side and referring to Fig. 4, we have

$$I_{L2} = I_o + I_1 \tag{6}$$

$$I_{in} = I_{L1} + I_1 \tag{7}$$

The input current can be obtained by

$$I_{in} = I_{L1} + I_{L2} - I_o \tag{8}$$

Fig. 5 shows key waveforms of the proposed converter in the case of CCM for both $D < 0.5$ and $D > 0.5$. Depending upon the duty cycle the converter has three among four operating modes, as shown in Fig. 6, within each operating cycle. In case of $D > 0.5$ there exists an overlap mode at which both main switches are turned on at the same time. The operations of Modes I–III occur (Figs. 5*b* and 6). In case of $D < 0.5$ there exists a dead time between the mode at which both main switches are turned off at the same time. The operations of Modes I, III and IV occur (Figs. 5*a* and 6).

4 Converter design

In this section, the main components of the converter are selected based on analytical expressions derived from the operation of the converter.

4.1 Inductor design

In case of $D < 0.5$ (Fig. 5*b*) inductor currents and input current at $t = T_s/2$ can be obtained by, respectively

$$i_{L1}\left(\frac{T_s}{2}\right) = \frac{1}{1-D} I_o + \frac{\Delta i_L}{2} - \frac{\Delta i_L}{1-D}(0.5 - D) \tag{9}$$

$$i_{L2}\left(\frac{T_s}{2}\right) = \frac{1}{1-D} I_o - \frac{\Delta i_L}{2} \tag{10}$$

$$i_{in}\left(\frac{T_s}{2}\right) = \frac{1+D}{1-D} I_o - \frac{\Delta i_{in}}{2} \tag{11}$$

Using (8)–(11) the input current ripple can be expressed as

$$\Delta i_{in} = 2\frac{\Delta i_L}{1-D}(0.5 - D) \tag{12}$$

The inductor current ripple can be expressed as

$$\Delta i_L = \frac{(V_C - V_{in})(1-D)}{L} T_s \tag{13}$$

From (12) and (13) the inductance can be obtained by

$$L = \frac{2(0.5 - D)(V_C - V_{in})}{\Delta i_{in} f_s} \tag{14}$$

In a similar way, the inductance in case of $D > 0.5$ can be obtained by

$$L = \frac{2V_{in}(D - 0.5)}{\Delta i_{in} f_s} \tag{15}$$

Finally, the larger value of the two calculated from (14) and (15) is chosen.

4.2 Capacitor design

In case of $D > 0.5$ (Fig. 5*b*) capacitor voltages and output voltage at $t = D\,T_s$ can be obtained by, respectively

$$v_{C1}(D\,T_s) = \frac{1}{1-D} V_{in} - \frac{\Delta v_C}{2} \tag{16}$$

$$v_{C2}(D\,T_s) = \frac{1}{1-D} V_o + \frac{\Delta v_C}{2} - \frac{\Delta v_C (D - 0.5)}{D} \tag{17}$$

$$v_o(D\,T_s) = \frac{1+D}{1-D} V_{in} - \frac{\Delta v_o}{2} \tag{18}$$

Using (4) and (16)–(18) the output voltage ripple can be

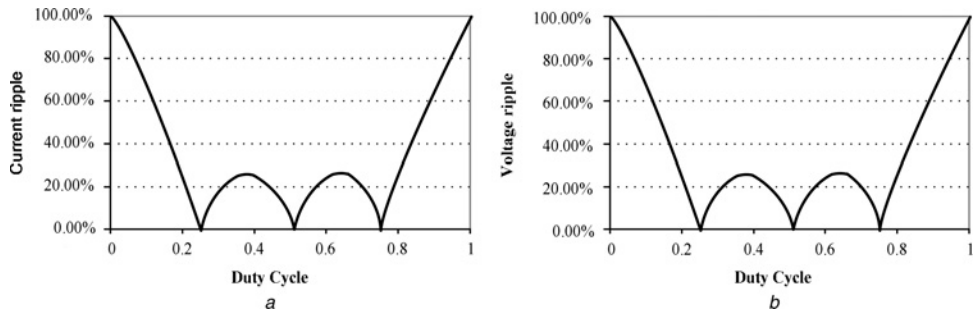

Figure 7

a Input current ripple against duty cycle as a percentage of the ripple through one inductance of the converter
b Output voltage ripple against duty cycle as a percentage of the ripple across one output capacitance of the converter

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Table 1 Comparison of component ratings of the proposed converter and two conventional converters

		Single boost converter ($D = 0.825$)	Two interleaved boost converter ($D = 0.825$)	Proposed converter ($D = 0.7$)
switch	V_{pk}	200 V	200 V	119 V
	I_{rms}	26 A	13 A	14 A
	switch utilisation factor $\left(\frac{V_o \times I_o}{n \times V_{pk} \times I_{pk}}\right)$	0.17	0.32	0.48
diode	V_{pk}	200 V	200 V	119 V
	I_{avr}	5 A	2.5 A	5 A
	diode utilisation factor $\left(\frac{V_o \times I_o}{n \times V_{pk} \times I_{pk}}\right)$	0.17	0.32	0.48
inductor	L	562 μH	450 μH × 2	300 μH × 2
	I_{rms}	28.6 A	14.3 A	16.7 A
	total energy volume (LI^2)	0.46	0.18	0.16
capacitor	C	35 μF	15 μF	17 μF × 2
	V_{avr}	200 V	200 V	117 V
	total energy volume (CV^2)	1.4	0.6	0.46

expressed as

$$\Delta v_o = 2\frac{\Delta v_C}{D}(D - 0.5) \tag{19}$$

The output voltage ripple can be expressed as

$$\Delta v_C = \frac{I_o D}{f_S C} \tag{20}$$

From (19) and (20), the capacitance can be obtained by

$$C = \frac{2I_o(D - 0.5)}{\Delta v_o f_S} \tag{21}$$

In a similar way, the capacitance in case of $D < 0.5$ can be obtained by

$$C = \frac{2I_o D(0.5 - D)}{\Delta v_o f_S} \tag{22}$$

Finally, the larger value of the two calculated from (21) and (22) is chosen.

4.3 Input current and output voltage ripple

There exist some interesting operating points corresponding to the duty cycles D of 0.25, 0.5 and 0.75 [23]. At these operating points the input current ripple of the converter is theoretically non-existent as shown in Fig. 7*a* while high voltage gain is achieved. It should be noted that the same cancellation occurs for the output voltage ripple at these exact points as shown in Fig. 7*b*, where the voltage ripple across a single capacitor is plotted as a percentage of the ripple.

4.4 Design example and comparison

In order to demonstrate the advantages of the proposed converter, a comparison for the component ratings of three

Table 2 Converter component specifications

inductance (L_1, L_2)	300 μH
capacitance (C_1, C_2)	100 μF
switch – MOSFET	FDH44N50
diode	RHRG5060

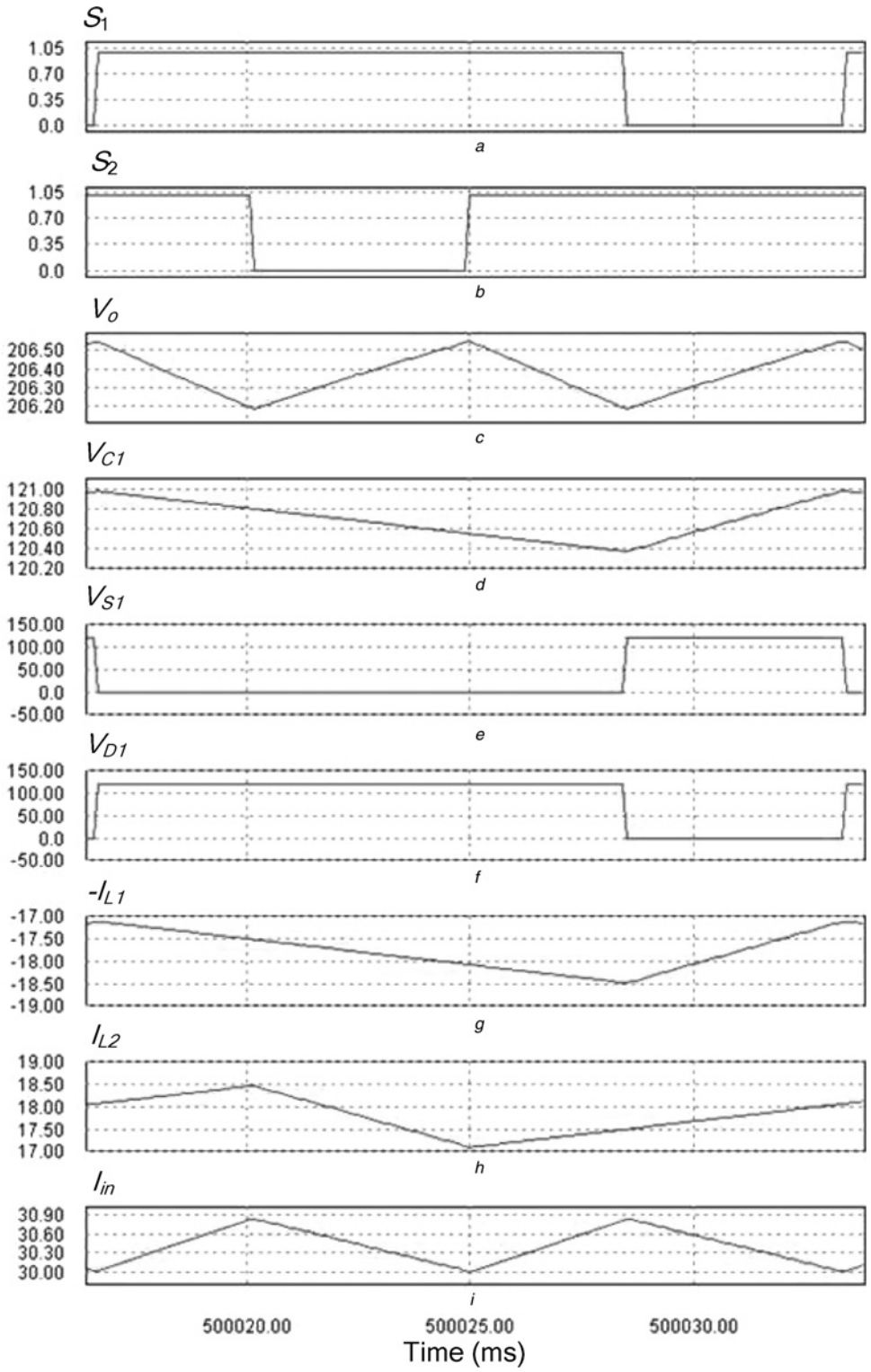

Figure 8 *Simulation results*

a and *b* Gate signals for the switches S_1 and S_2, respectively
c Output voltage
d Capacitor C_1 voltage
e Voltage across the switch S_1
f Voltage across the diode D_1
g Inductor current I_{L1}
h Inductor current I_{L2}
i Input current

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converter topologies is provided in this section. The three converters considered for comparison purposes are as follows:

1. The conventional single boost converter (Fig. 1*a*)

2. The conventional two interleaved boost converter connected in parallel (Fig. 2*a*)

3. The proposed converter (Fig. 4)

The comparison is performed for the following specifications and is summarised in Table 1:

$P_o = 1$ kW, $V_{in} = 35$ V, $V_o = 200$ V, $\Delta I_{in} = 3\%$, $\Delta V_o = 1\%$, $f_s = 60$ kHz

From the information presented in Table 1, the following observations can be made:

- The switch and diode voltage ratings of the proposed converter are 60% of those of the conventional converters. Therefore lower on-drop devices can be chosen for the proposed converter, leading to reduced conduction losses.

- The switch and diode utilisation factors are 2.8 times and 1.5 times higher than those of the single boost converter and the two interleaved boost converter, respectively. Therefore the cost of the switching devices of the proposed converter is the lowest.

- Since the input currents are divided, the total inductor energy volumes of the proposed converter and the two

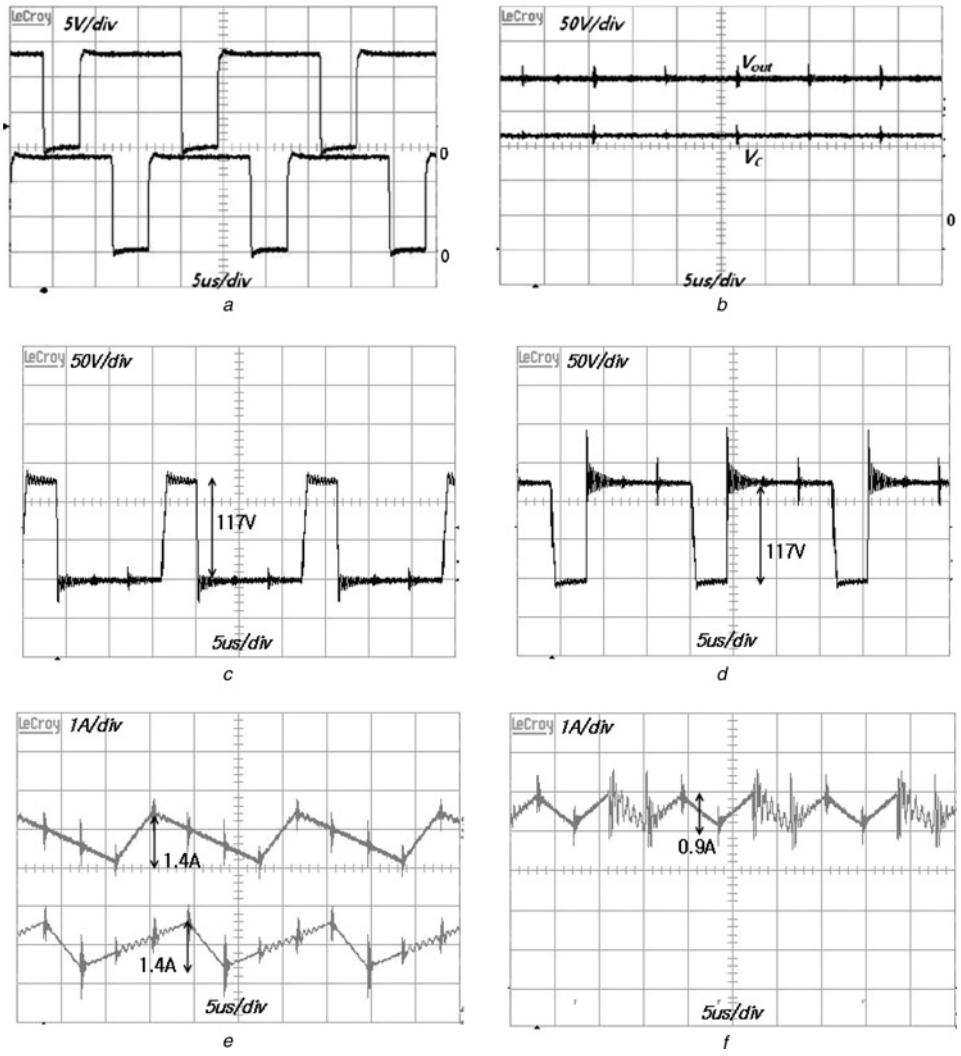

Figure 9 *Experimental waveforms*

a Gate signals for main switches
b Output voltage and capacitor voltage (50 V/div)
c Switch voltage (50 V/div)
d Diode voltage (50 V/div)
e Inductor currents $-I_{L1}$ (top waveform) and I_{L2} (bottom waveform) (1 A/div)
f Input current (1 A/div)

interleaved converter are less than half of that of the single boost converter even though they require two inductors.

- The capacitor voltage rating of the proposed converter is 60% of those of the conventional converters. Even though the proposed converter requires two capacitors, the total energy volume of the capacitor is only 33 and 76% of the single boost converter and the two interleaved boost converter, respectively.

Therefore the volume and cost of the proposed converter will be reduced compared to the single boost converter even though it requires twice as many components. Moreover, when compared to the conventional two interleaved boost converter, the proposed converter shows higher switch and diode utilisation factors and lower energy volume of the passive components since it requires smaller duty cycle for the same design specification.

5 Simulated and experimental results

A laboratory prototype has been built and tested to confirm the theoretical analysis and design of the proposed converter.

$$P_o = 1\ \text{kW} \quad V_{in} = 35\ \text{V} \quad V_o = 200\ \text{V}$$

$$\Delta I_{in} = 3\% \quad \Delta V_o = 1\% \quad f_s = 60\ \text{kHz}$$

The duty cycle is calculated to be 0.71. The key operating waveforms of the converter with the specifications provided above (Table 2) generated through computer simulation are presented in Fig. 8. PSIM software has been used to generate the waveforms and the presented results [36].

Experimental waveforms taken from the laboratory prototype with the above specifications (Table 2) are presented in Fig. 9. Specifically, Fig. 9*a* shows gating signals for main switches S_1 and S_2. Fig. 9*b* shows the output voltage and capacitor voltage V_{C1}. It is noted that the capacitor voltage is only 117 V which is slightly larger than half the output voltage. Figs. 9*c* and *d* show the voltages across the main switch and the diode, respectively. They are the same as the capacitor voltage which is much smaller than the output voltage.

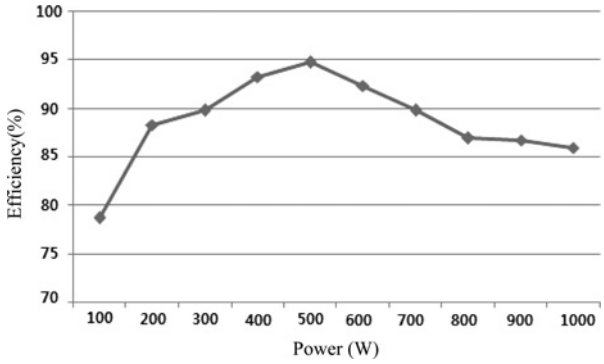

Figure 10 *Measured efficiency of the proposed converter*

The interleaving effect of the proposed converter is shown in Figs. 9*e* and *f*. The peak-to-peak ripples of the inductor current and input current are shown to be 1.4 and 0.9 A, respectively, which are in close agreement with theoretical values obtained by (13) and (12), respectively, and the simulated results are presented in Figs. 8*g*, *h* and *k*.

The measured overall efficiency of the proposed converter is shown in Fig. 10. The maximum overall efficiency of 95% was measured at 500 W load.

6 Conclusion

A generalised approach to deriving new floating-output boost converters using the basic non-floating boost and versions of the floating boost has been presented in this paper. The analysis and design of the basic high-gain floating-output transformer-less boost converter are also provided. It is shown that by paralleling at the input a non-floating and a floating boost converter topology, an interleaved input and higher output voltage with reduced voltage ripple can be derived which also offers modularity. Other combinations can also be explored and derived but they need to follow some rules. Experimental results taken from a 1 kW laboratory prototype operating at 60 kHz have been presented to confirm the principles of operation of the converter and the respective design guidelines, which are also provided in the paper.

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