Multiphase DC–DC Converters Using a Boost-Half-Bridge Cell for High-Voltage and High-Power Applications

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***Abstract*—In this paper, multiphase dc–dc converters are proposed for high-voltage and high-power applications. A generalized converter is configured such that the boost-half-bridge (BHB) cells and voltage doublers are connected in parallel or in series to increase the output voltage and/or the output power. In addition to reduced device voltage and current ratings by the connection, the proposed converter has the following features: high-step-up voltage gain with significantly reduced transformer turn ratio, low-input current ripple due to interleaving effect, zero-voltage switching turn-ON of switches and zero-current switching turn-OFF of diodes, no additional clamping and start-up circuits required, high-component availability and easy thermal distribution due to the use of multiple small components, and flexibility in device selection resulting in optimized design. A design guideline of determining the optimum circuit configuration for given output voltage and power level is presented. Experimental results are also provided to validate the proposed concept.**

***Index Terms*—Active clamping, boost-half-bridge (BHB), high step-up, multiphase, soft-switched.**

I. Introduction

THE ISOLATED step-up dc–dc converter has been increasingly needed in high-power applications, such as fuel-cell systems, photovoltaic systems, hybrid electric vehicles, and uninterruptible power system (UPS), where high-step-up ratio and the use of high-frequency transformers for galvanic isolation and safety purpose are required. The multiphase dc–dc converter could be a choice of topology for high-power applications. Generally, the multiphase dc–dc converter has several advantages over the conventional dc–dc converter based on full-bridge, half-bridge, and push–pull topologies, reduction of MOSFET conduction losses, easy device selection due to reduced current rating, reduction of the input and output filters' volume due to increased effective-switching frequency by a factor of phase number, and reduction in transformer size due to better transformer utilization. Several isolated three-phase dc–dc converters have been proposed for high-power applications [1]–[10]. They can be classified into voltage-fed [1]–[5] and current-fed [6]–[10] types. The first three-phase dc–dc converter that has been introduced by Ziogas in [1] does not provide soft commutation, which limits the switching frequency and the power density. The asymmetrical pulsewidth modulation (PWM) has been proposed to provide zero-voltage switching (ZVS) commutation, which utilizes transformer leakage inductances and MOSFET output capacitors [2]. The hybridge rectifier has been employed to reduce the diode conduction losses in the low-voltage and high-current applications [3]. An active-clamping technique not only suppresses the surge voltage, but helps to reduce the circulating current and compensate the duty cycle loss [4]. At the expense of increased number of switches, the V6 converter [5] becomes beneficial in higher power application. The current-fed converter, compared to its voltage-fed counterpart, exhibits lower transformer turns ratio, smaller input current ripple, and lower diode voltage rating.

The three-phase current-fed dc–dc converter proposed so far can be classified by primary-side configuration into three basic topologies: push–pull [6], [7], full-bridge [8], and half-bridge [9], [10]. Among them, the current-fed push–pull converter [6] has the simplest structure and the least number of components, but suffers from dissipative losses associated with hard switching of main switches and voltage spikes caused by leakage inductance of the high-frequency transformer. An active-clamped current-fed push–pull converter [7] achieves ZVS operation and lossless clamping as well as enlarges the operating duty cycle to whole range at the expense of increased components and complexity. A full-bridge-based current-fed converter with active clamp [8] also achieve ZVS of main switches, but the single-active clamp branch suffers from high-current rating and high-switching frequency, which is three times the switching frequency of the main switch. The passive [9] and active [10] clamping versions of the L-type half-bridge-based current-fed converter were proposed with similar advantages and disadvantages discussed in the aforementioned schemes.

In the meanwhile, the boost-half-bridge (BHB) converter has been presented [11]–[15]. It demonstrates the following features: small input filter due to continuous input current, low electromagnetic interference (EMI) due to ZVS turn ON of all power switches, wide-input voltage range application due to wide-duty cycle range. The BHB converter with a voltage-doubler rectifier at the secondary has further advantages, which are no dc magnetizing current of the transformer, reduced voltage surge associated with diode reverse recovery, and no circulating current due to absence of output filter inductor [13].

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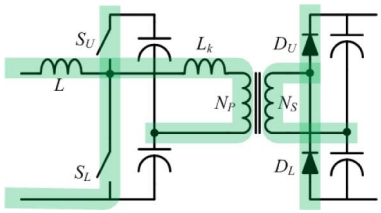

Fig. 1. BHB cell as a building block for the proposed multiphase converter.

In this paper, multiphase dc–dc converters using a BHB converter as a basic building block are proposed for high-voltage and high-power applications. A generalized multiphase dc–dc converter is configured in such a way that the BHB cell and the voltage-doubler rectifier are connected in series, in parallel, or by combination of them at the primary and secondary, respectively, to increase the output voltage and/or the output power. Therefore, the device current rating of the proposed multiphase converter is reduced by increasing the number of parallel connection, and the device voltage rating is reduced by increasing the number of series connection. In summary, in addition to the advantages of the conventional multiphase converter, which include reduced current rating and reduced volume of input and output filters resulting from the interleaved switching, the proposed multiphase converter has the following features.

1) Significantly reduced turn ratio of the transformer and voltage rating of the diodes and capacitors, and therefore, especially suitable to high-step-up applications.
2) Natural ZVS turn-ON of main switches using energy stored in transformer leakage inductor, and zero-current switching (ZCS) turn-OFF of rectifier diodes, which results in greatly reduced voltage surge associated with the diode reverse recovery.
3) No additional clamping and start-up circuits required due to the proposed interleaved asymmetrical PWM switching.
4) High-component availability, easy thermal distribution, and low profile due to the use of multiple small components instead of single-large component.
5) Flexibility in device selection by proper choice of topology resulting in optimized design under harsh design specification.

The interleaving effect of the multiphase configuration is examined. How to determine the optimum circuit configuration for given output voltage and power level is also presented.

II. Proposed Multiphase DC–DC Converter

A. Generalized Multiphase DC–DC Converter

Fig. 1 shows the BHB cell that is used as a building block of the proposed multiphase converter. Fig. 2 shows the generalized circuit of the proposed multiphase dc–dc converter for high-voltage and high-power applications.

The generalized converter has "*N*" groups of converters, where each group of switch legs is connected in parallel at the low-voltage high-current side, while each group of voltage doublers is connected in series at the high-voltage low-current side, i.e., "*N*" is the number of voltage doublers connected in series to build the output voltage. Each of *N* groups also has "*P*" parallel connected legs, where "*P*" is the number of switch or diode legs connected in parallel to increase the output power.

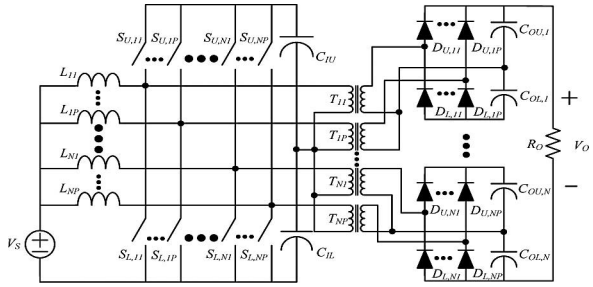

Fig. 2. Proposed multiphase dc–dc converter (*N* is the number of series-connected voltage doublers, and *P* is the number of diode legs connected to the same output capacitors).

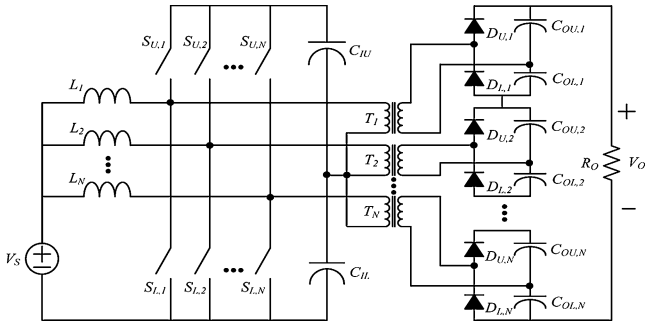

Fig. 3. Example circuit configuration of the proposed multiphase converter, which illustrates how to increase the output voltage ($P = 1$).

For example, the "*N*th" group having "*P*" parallel-connected legs includes input inductors L_{N1} to L_{NP}, upper switches $S_{U,N1}$ to $S_{U,NP}$ (lower switches $S_{L,N1}$ to $S_{L,NP}$), transformers T_{N1} to T_{NP}, and upper diodes $D_{U,N1}$ to $D_{U,NP}$ (lower diodes $D_{L,N1}$ to $D_{L,NP}$), which are connected to the same output capacitors $C_{\mathrm{OU},N}$ ($C_{\mathrm{OL},N}$).

In summary, "*N*" could be increased to get higher output voltage, and "*P*" could be increased to get higher output power. Fig. 3 shows an example circuit configuration when *P* is equal to 1, which illustrates how to increase output voltage by increasing "*N*." Fig. 4 shows an example circuit configuration when *N* is equal to 1, which illustrates how to increase power level by increasing "*P*." In both cases, the interleaving technique can be applied to reduce the size of input filter inductors, and input and output capacitors. Therefore, "*N*" and "*P*" could properly be chosen according to given output voltage and power level. This could give flexibility in device selection resulting in optimized design even under harsh design specifications.

B. Operating Principles

The key waveforms of the generalized multiphase dc–dc converter are shown in Fig. 5. The interleaved asymmetrical PWM switching is applied to the multiphase converter, i.e., *D* and $1 - D$ are the duty cycles of lower and upper switches of a leg, respectively, and each leg is interleaved with a phase difference of $2\pi/(N{\cdot}P)$. The average value of the inductor current can be

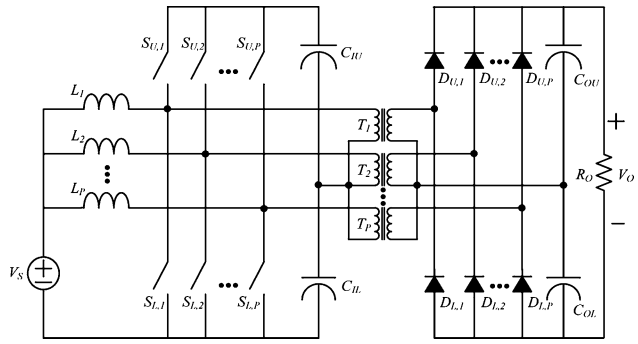

Fig. 4. Example circuit configuration of the proposed multiphase converter, which illustrates how to increase the output power ($N = 1$).

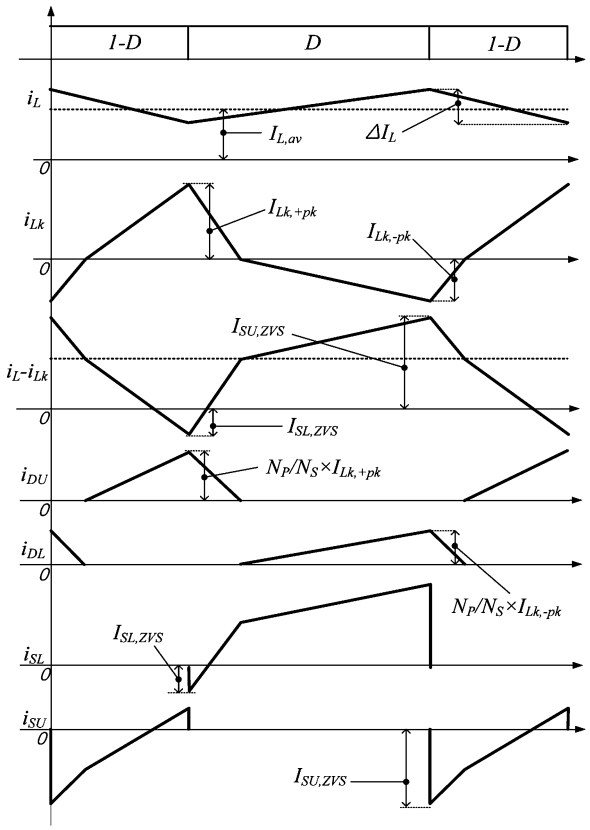

Fig. 5. Key waveforms of the generalized multiphase dc–dc converter.

obtained by

$$I_{L,\mathrm{av}} = \frac{V_O^2}{V_S R_O}\frac{1}{NP}. \tag{1}$$

This value decreases as $N{\cdot}P$ increases. The magnitude of the inductor current ripple is obtained by

$$\Delta I_L = \frac{V_S}{L f_S} D. \tag{2}$$

The positive-peak value of the primary winding current can be obtained by

$$I_{L_k,+\mathrm{pk}} = \frac{2V_O}{(1-D)R_O}\frac{N_S}{N_P}\frac{1}{P} + \frac{D^2 V_S}{\left(D^2+(1-D)^2\right) L_k f_s}. \tag{3}$$

It decreases as P increases and does not depend on N. The negative-peak value of the primary winding current can be obtained by

$$I_{L_k,-\mathrm{pk}} = \frac{2V_O}{DR_O}\frac{N_S}{N_P}\frac{1}{P} + \frac{(1-D)DV_S}{\left(D^2+(1-D)^2\right) L_k f_s}. \tag{4}$$

It decreases as P increases and does not depend on N.

C. ZVS Characteristics of Main Switch

The ZVS current of main switches is related with the difference of the inductor current and the primary winding current $i_L - i_{L_k}$, as shown in Fig. 5. The negative peak of $i_L - i_{L_k}$ is $I_{S_L,\mathrm{ZVS}}$, which is ZVS current for lower switches when the upper switch is turned off and can be expressed as follows:

$$\begin{aligned} I_{S_L,\mathrm{ZVS}} &= |I_{L_k,+\mathrm{pk}}| - \left(I_{L,\mathrm{av}} - \frac{1}{2}\Delta I_L\right) \\ &= \frac{V_O}{(1-D)R_O}\frac{N_S}{N_P}\frac{2}{P} + \frac{D^2 V_S}{(D^2+(1-D)^2)L_k f_s} \\ &\quad - \frac{V_O^2}{V_S R_O}\frac{1}{NP} + \frac{DV_S}{2Lf_s}. \end{aligned} \tag{5}$$

The positive peak of $i_L - i_{L_k}$ is $I_{S_U,\mathrm{ZVS}}$, which is ZVS current for upper switches when the lower switch is turned off and can be expressed as follows:

$$\begin{aligned} I_{S_L,\mathrm{ZVS}} &= |I_{L_k,-\mathrm{pk}}| - \left(I_{L,\mathrm{av}} + \frac{1}{2}\Delta I_L\right) \\ &= \frac{V_O}{DR_O}\frac{N_S}{N_P}\frac{2}{P} + \frac{(1-D)DV_S}{(D^2+(1-D)^2)L_k f_s} \\ &\quad + \frac{V_O}{V_S R_O}\frac{1}{NP} + \frac{1}{2}\frac{V_S}{Lf_s}D. \end{aligned} \tag{6}$$

To ensure the ZVS turn ON of upper switch S_U, the following condition should be satisfied:

$$\frac{1}{2}L_k I_{S_U,\mathrm{ZVS}}^2 > \frac{1}{2}C_{\mathrm{os,tot}}\left(\frac{V_S}{1-D}\right)^2. \tag{7}$$

In fact, the condition of (7) can easily be satisfied, and ZVS of upper switch S_U can be achieved over the whole load range. To ensure the ZVS turn ON of lower switch S_L, the following condition should be satisfied:

$$\frac{1}{2}L_k I_{S_L,\mathrm{ZVS}}^2 > \frac{1}{2}C_{\mathrm{os,tot}}\left(\frac{V_S}{1-D}\right)^2. \tag{8}$$

Equation (8) may not be satisfied under the conditions of small transformer leakage inductance, large input filter inductance, and/or heavy load [refer to (5)]. Increasing transformer leakage inductance to enlarge the ZVS region makes the duty cycle loss large, resulting in increased turn ratio. Instead, in order to enlarge the ZVS region, the input inductance can be decreased so that $I_{S_L,\mathrm{ZVS}}$ can be increased. However, decreasing the input filter inductance increases the current rating of the power devices, and therefore, the input filter inductance should be properly chosen considering a tradeoff between the ZVS region and the device current ratings.

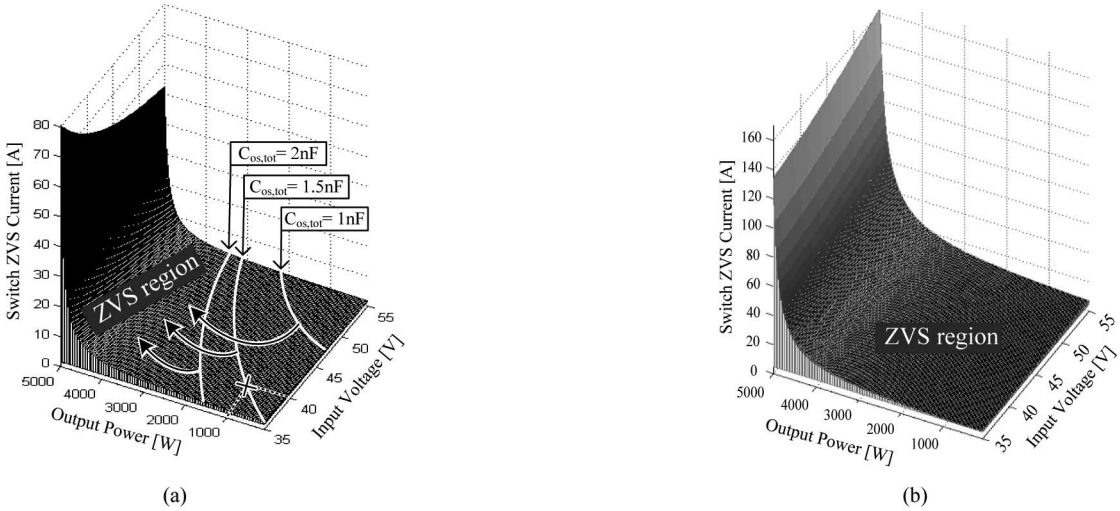

Fig. 6. ZVS currents and ZVS ranges of lower and upper switches as the function of the input voltage and output power when $N = 3$ and $P = 1$. (a) Lower switch. (b) Upper switch ($V_S = 35$–55 V, $V_O = 400$ V, $P_O = 100$ W–5 kW, $N_S/N_P = 2$, and $L_k = 4\ \mu$H).

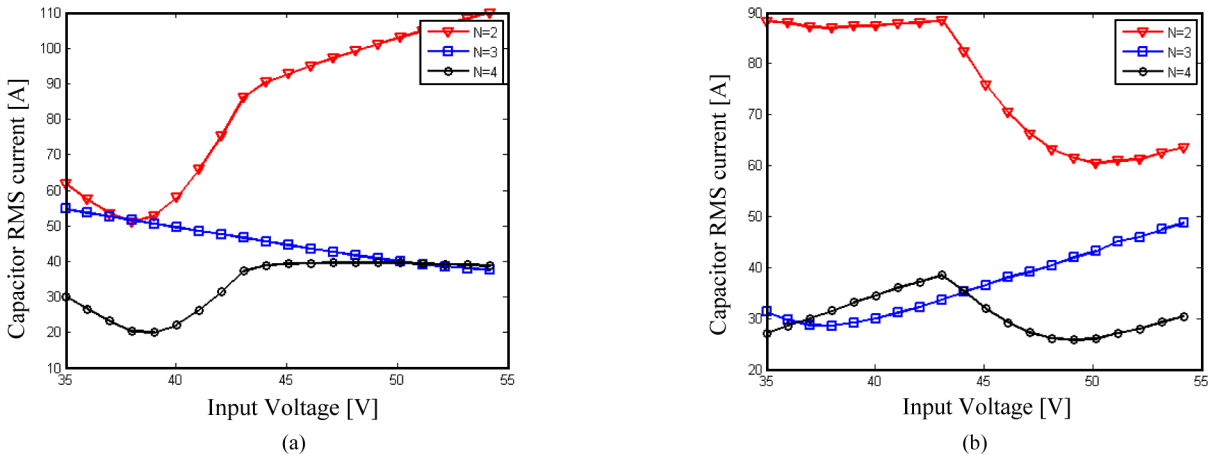

Fig. 7. RMS current of input capacitor as a function of input voltage and N when $P = 1$. (a) $C_{\rm IL}$. (b) $C_{\rm IU}$ ($V_S = 35$–55 V, $V_O = 400$ V, $P_O = 100$ W–5 kW, and $L_k = 4\ \mu$H).

Using (5)–(8), the ZVS currents and ZVS ranges of lower and upper switches as the function of input voltage and output power are plotted, respectively, as shown in Fig. 6. As shown in Fig. 6(a), the ZVS current of the lower switch tends to increase as the output power increases and decrease as the input voltage increases. This means that the ZVS turn-ON of the lower switch can be more easily achieved under the condition of higher output power and lower input voltage. It is noted that the ZVS range of the lower switch becomes broader for smaller total output capacitance $C_{\rm os,tot} = C_{{\rm oss},S_L} + C_{{\rm oss},S_U}$ of MOSFETs. For example, if MOSFETs with total output capacitance $C_{os,{\rm tot}}$ of 1.5 nF are selected in this example, the ZVS turn-ON of the lower switch can be achieved with output power, which is greater than 1000 W at input voltage of 40 V[see Fig. 6(a)].

The ZVS current of the upper switch tends to increase as the output power and input voltage increase. It should be noted from Fig. 6(b) that the ZVS turn-ON of the upper switch can be achieved in the overall input voltage and output power ranges.

D. Interleaving Effect

Each leg of the multiphase converter is switched with a phase difference of $2\pi/(N{\cdot}P)$. The ripple frequency of the input and input capacitor currents becomes $N{\cdot}P$ times the switching frequency of the main switch. The rms current of the input and input capacitor also decrease as N and P increases.

The ripple frequency of the output capacitor current becomes P times the switching frequency of the main switch. The rms current of the output capacitor decreases as P increases. Due to the interleaved operation, the weight and volume of input capacitors, output capacitor, and input inductors are significantly reduced.

The interleaving effect on the input inductor and output capacitor of the proposed converter is obvious and has been mentioned in many literatures [12]–[14]. The interleaving effect on the input capacitors $C_{\rm IU}$ and $C_{\rm IL}$ differs from that of the input inductor and output capacitor. The capacitor rms currents are calculated and plotted in Fig. 7 as a function of input voltage and N. It tends to decrease as N increases in general. The

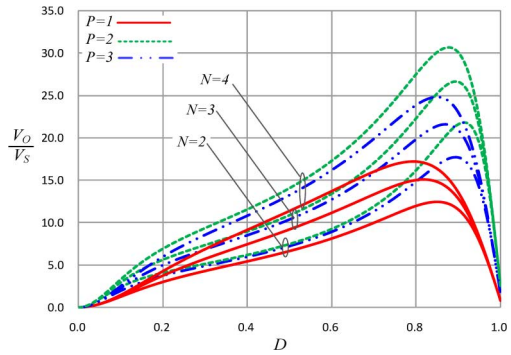

Fig. 8. Voltage conversion ratio as a function of duty ratio D with different N and P ($V_S = 35$ V, $V_O = 400$ V, $L_k = 4\ \mu$H, $f_S = 50$ kHz, $N_S/N_P = 2$, and $P_O = 5$ kW).

capacitor current as a function of P is not shown in this paper and it also tends to decrease as P increases.

E. Voltage Conversion Ratio

The ideal voltage conversion ratio of the proposed converter can be obtained by

$$\frac{V_O}{V_S} = \frac{N}{1-D}\frac{N_S}{N_P}. \tag{9}$$

Basically, as N increases the voltage conversion ratio linearly increases. Considering the effect of voltage drop across the leakage inductance of the transformer, the actual voltage conversion ratio can be obtained by (10), as shown at the bottom of the page.

In Fig. 8, the actual voltage conversion ratio is plotted as a function of duty ratio D with different N and P. It can be seen that as P increases the voltage conversion ratio also slightly increases (theoretically, it converges to the ideal voltage conversion ratio as P increases to infinity), since the effect of the voltage drop across the leakage inductance on the voltage conversion ratio becomes smaller.

In general, the duty cycles of the conventional voltage-fed and current-fed converters based on push–pull, half-bridge, or full-bridge topologies are restricted to smaller than 0.5 or larger than 0.5, respectively. However, the duty cycle of the proposed converter based on the BHB cell ranges from 0 to 1, resulting in no use of an additional clamping circuit as well as improved dynamic characteristics. It should be noted that no additional start-up circuits is also required for the proposed converter, since there is no restriction on the duty cycle.

It should also be noted that the rectifier diodes of the proposed converter are turned off with ZCS, as shown in Figs. 5 and 10, surge voltage associated with the diode reverse recovery is trivial, and therefore, the snubber circuit does not necessitate.

TABLE I
TRANSFORMER TURN RATIO AND VOLTAGE RATING OF THE SWITCH AND DIODE ($V_S = 35$–55 V, $V_O = 400$ V, AND $P_O = 5$ KW)

N	*Range of* N_S/N_P	N_S/N_P	*Range of* D	*Switch* V_{PK}	*Diode* V_{PK}
1	3.0 ~7.0	5	0.32~0.72	125	400
2	1.6~3.5	4	0.41~0.68	107.7	200
3	1.1~2.3	2	0.38~0.61	89	133
4	0.8~1.8	1.5	0.35~0.57	81.3	100

III. DESIGN EXAMPLE

In this section, a design example of the proposed converter is presented, considering the following specifications:

- $P_O = 5$ kW, $V_O = 400$ V, V_S : 35–55 V,
- $L_k = 4\ \mu$H, $f_S = 50$ kHz, $\Delta I_s = 5\%$, $\Delta V_O = 3\%$.

The usable range of the transformer turn ratio can be calculated, using (9), as follows:

$$\frac{V_O}{V_{S,\min}}\frac{1-D_{\max}}{N} < \frac{N_S}{N_P} < \frac{V_O}{V_{S,\max}}\frac{1-D_{\min}}{N}. \tag{11}$$

The duty cycle of each switch of the proposed converter, theoretically, ranges from 0 to 1 due to the switching method based on asymmetrical PWM. However, the operating duty cycle should be limited, say $0.3 < D < 0.7$, since too small or large duty cycles cause large peak current rating of the components. Table I lists the usable range of the transformer turn ratio for several cases of N for a specified duty cycle range of $0.3 < D < 0.7$.

A proper transformer turn ratio is chosen within the usable range, considering the actual duty cycle range, which also affects the voltage and current rating of the switch and diode. It should be noted that the peak voltage rating of the main switch is calculated to be $V_{S,\min}/(1-D_{\max})$, where $D_{\max}$ depends on the output voltage, N, and P, as shown in (10).

In this example, N is chosen to be 3 so that the switch voltage rating is 89 V, and therefore, the MOSFETs with lower $R_{\mathrm{ds(ON)}}$ can be chosen for the proposed converter, resulting in reduced conduction losses. The peak diode voltage rating is 133 V, a third of output voltage, due to the series connection of the three voltage doublers. A Schottky diode of voltage rating of 170 V with lower reverse recovery loss and forward voltage drop can be used, and the losses associated with rectifier diodes can be significantly reduced. With $N = 3$ and several cases of P, the current rating of the main switch and rectifier diode can also be calculated using the current waveform in Fig. 5.

Table II lists the current rating of the switch and diode for several cases of P when $N = 3$. In this example, P is chosen to be 1, and the MOSFET IXFH120N15 (150 V, 120 A) and the Schottky diode STPS30170C (170V, 30A) are selected, which

$$\frac{V_O}{V_S} = \frac{D^2(1-D)}{((((2D-1)^2+1)L_k f_s N_S)/N_P R_O)\,(1/P) + ((D^2(1-D)^2 N_P)/N_S)(1/N)}. \tag{10}$$

TABLE II
CURRENT RATING OF THE SWITCH AND DIODE WITH $N = 3$ (V_S = 35–55 V, V_O = 400 V, AND P_O = 5 KW)

P	*Lower Switch* $I_{SL,rms}$	*Upper Switch* $I_{SU,rms}$	*Upper Diode* $I_{DU,av}$ ($I_{DU,PK}$)	*Lower Diode* $I_{DL,av}$ ($I_{DL,PK}$)
1	67.8	29.7	14.0(58)	14.0(58)
2	33	14	7.0(29)	7.0(29)
3	16.5	7	4.7(19.3)	4.7(19.3)
4	8.2	3	3.5(14.5)	3.5(14.5)

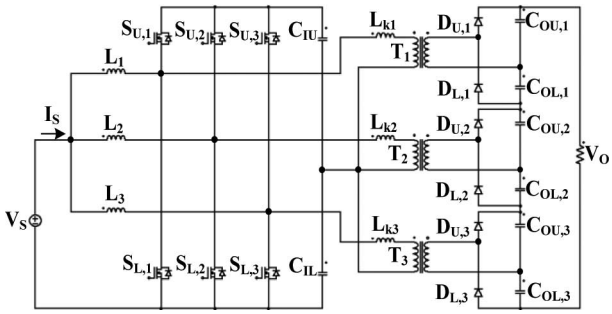

Fig. 9. Circuit diagram of the proposed converter with $N = 3$ and $P = 1$.

satisfy both voltage ratings in Table I and current ratings in Table II.

The circuit diagram of the proposed multiphase converter with $N = 3$ and $P = 1$ is shown in Fig. 9. The proposed converter with $N = 3$ and $P = 1$ consists of three filter inductors, six MOSFET switches, two input capacitors at the low-voltage side and three series-connected voltage-doubler rectifiers at the high-voltage side. Three high-frequency transformers are employed for step-up and isolation. Three voltage-doubler rectifiers are connected in series at the output so that the diode voltage rating becomes one-third of the output voltage. The proposed converter also employs six output capacitors, but total energy volume of the capacitors are smaller, since the capacitor peak voltage is much smaller.

Since the ideal voltage conversion ratio of the proposed converter is three times that of the conventional BHB converter, the required turn ratio has greatly reduced $N_P{:}N_S$ = 1:2 in this example, which reduces the number of turns of the transformer winding, leading to reduced copper loss and leakage inductance of the transformer. The ratings of the passive components, such as the input inductor, the input capacitor, and the output capacitor according to the design specification are calculated and listed in Table III.

Fig. 10 shows key waveforms of the proposed converter with N = 3 and P = 1. The three switch legs are interleaved with 120° phase shift, and the upper and lower switches of each leg are operated with asymmetrical complementary switching to regulate the output voltage. The converter has six operating modes within each operating one-third cycle.

Fig. 11 shows the equivalent circuits of the six operating modes. At the beginning of Mode 3, the output capacitor of upper switch $S_{U,1}$ is discharged by $I_{S_U,\mathrm{ZVS}}$, summation of the

TABLE III
RATINGS OF PASSIVE COMPONENTS WITH $N = 3$, $P = 1$ (V_S = 35–55 V, V_O = 400 V, P_O = 5 KW, ΔI_s = 5%, AND ΔV_O = 3%)

	Design item	*Value*
Input filter inductor L_1, L_2, L_3	Inductance	12uH
	I_{rms}(I_{pk})	48.45A(64.65A)
Input capacitor C_{IU}, C_{IL}	Capacitance	20uF
	I_{rms}(I_{pk})	56.19A (122.69A)
Output capacitor C_{OU}, C_{OL}	Capacitance	6.8uF
	I_{rms} (I_{pk})	17.7A(39.1A)

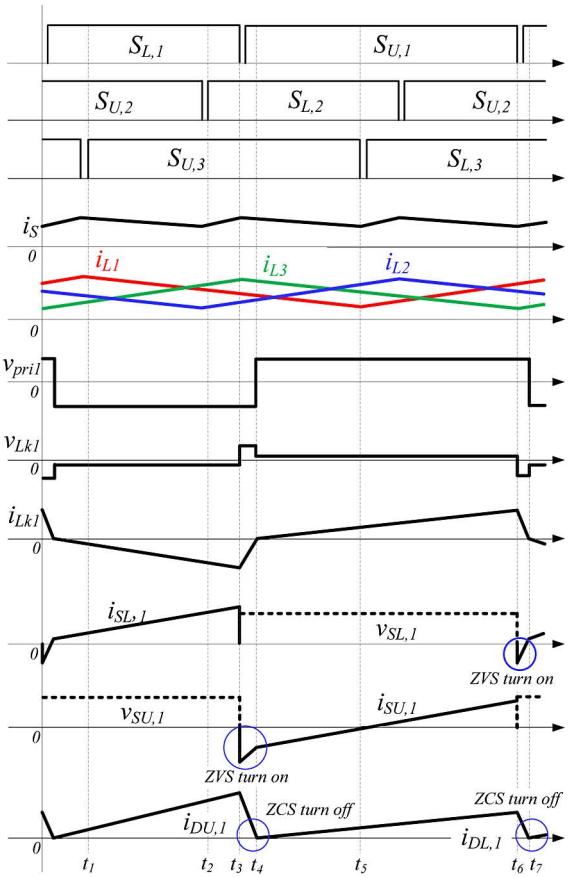

Fig. 10. Key waveforms of the proposed converter with $N = 3$ and $P = 1$.

input filter inductor current and the primary winding current at t_3, which is determined by (7). At the beginning of Mode 6, the output capacitor of lower switch $S_{L,1}$ is discharged by $I_{S_L,\mathrm{ZVS}}$, difference between the primary winding current and the input filter inductor current at t_6, which is determined by (8). The ZVS currents and ZVS ranges of lower and upper switches as the function of the input voltage and output power for this case of $N = 3$ and $P = 1$ is shown in Fig. 6.

IV. EXPERIMENTAL RESULT

A 5-kW laboratory prototype of the proposed converter with $N = 3$ and $P = 1$ (see Fig. 9) has been built to demonstrate the operating principles.

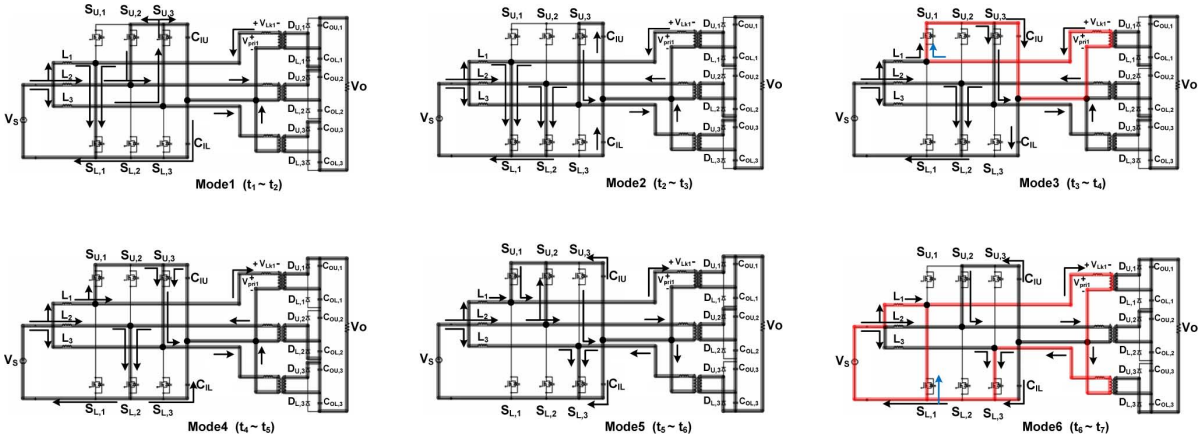

Fig. 11. Operation modes of the proposed converter with $N = 3$ and $P = 1$.

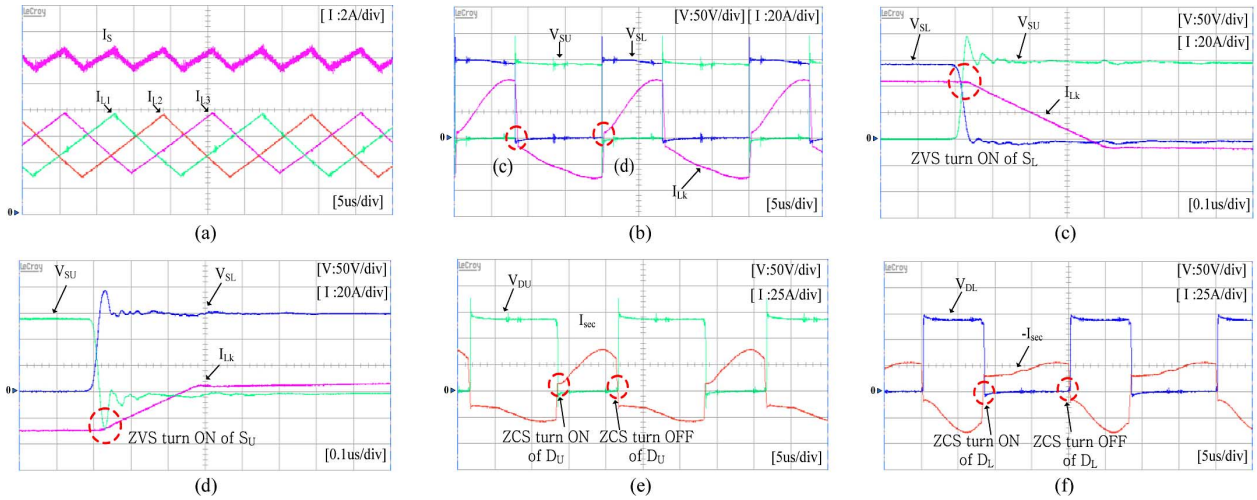

Fig. 12. Experimental waveforms. (a) Input and inductor currents showing interleaving effect. (b) Drain–source voltages of S_L and S_U and primary transformer current I_{L_k}. (c) Extended waveform of (b) showing ZVS turn ON of switch S_L. (d) Extended waveform of (b) showing ZVS turn ON of switch S_U. (e) Diode voltage of D_U and secondary transformer current $I_{\rm sec}$. (f) Diode voltage of D_L and secondary transformer current $I_{\rm sec}$.

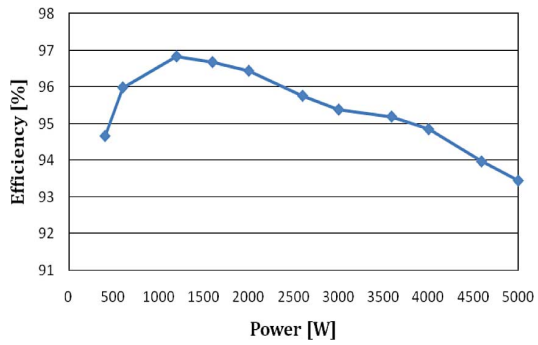

Fig. 13. Measured efficiency ($P_o = 5$ kW, $V_{\rm in} = 60$ V, and $V_{\rm out} = 400$ V).

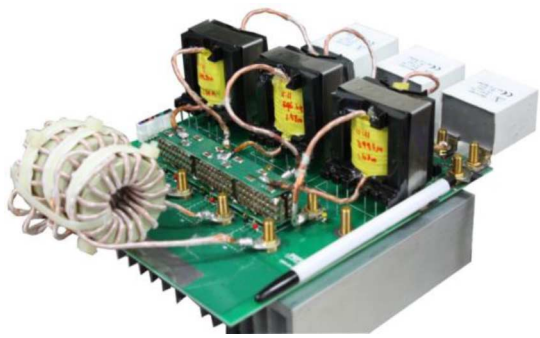

Fig. 14. Photograph of the proposed converter.

The proposed converter is experimented under the following system parameters:

- $P_O = 5$ kW, • $V_O = 400$ V, • $V_S = 60$ V, • $f_S = 50$ kHz
- $L_1 = L_2 = L_3 = 50\ \mu$H, • $C_{\rm IU} = C_{\rm IL} = 45\ \mu$F,
- $C_{\rm OU} = C_{\rm OL} = 30\ \mu$F.

Each transformer is built using PQ50/50 core with the number of turns of *Np*:*Ns* = 11:11. The transformer leakage inductance referred to the primary side is 1 μH. Each switch is implemented with International Rectifier IRFB4668PbF (200 V, 130 A, and 8 mΩ) MOSFET. Schottky diodes of ON Semiconductor MBR40250 (250 V and 40 A) are used for secondary rectifier. The prototype has been implemented with open-loop test to verify the proposed topology. Fig. 12 shows experimental waveforms obtained at 5 kW load. As we can see from Fig. 12(a),

there is no distinguishable disequilibrium among the interleaved inductor currents. Actually, the input capacitors were separated for each phase and this helps to alleviate the unbalance caused by difference in circuit parameters or mismatch in duty cycle [20]. Fig. 12(b) shows the drain-source voltages of switches S_L and S_U, and primary transformer current I_{L_k}. The extended waveforms of Fig. 12(b) are shown in Fig. 12(c) and (d). It can be seen from Fig. 12(c) and (d) that both lower switch S_L and upper switch S_U are being turned on with ZVS, respectively. Fig. 12(e) and (f) show ZCS turn ON and OFF of upper diode D_U and lower diode D_L, respectively. The measured efficiency of the proposed converter is shown in Fig. 13.

The maximum efficiency of 96.8% was measured at 1200 W load. The full-load efficiency was 93.4%. The photograph of the proposed converter is shown in Fig. 14.

V. Conclusion

This paper proposes a generalized multiphase dc–dc converter using the BHB cell and voltage doubler for parallel and/or series connection to increase the output voltage and/or the output power. The proposed converter has the following features: significantly reduced transformer turn ratio, ZVS turn-ON of switches and ZCS turn-OFF of diodes, no additional clamping and start-up circuits required, high-component availability and easy thermal distribution, and flexibility in device selection resulting in optimized design. Therefore, the proposed multiphase converter is suitable for high-voltage and high-power applications.

A way of determining the optimum circuit configuration for given output voltage and power level has been presented. Experimental results have also been provided to validate the proposed concept.

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