Control Scheme for Autonomous and Smooth Mode Switching of Bidirectional DC–DC Converters in a DC Microgrid

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***Abstract*—In dc microgrid (MG) systems, energy storage systems (ESSs) capable of short- or long-term energy buffering are indispensable for energy management and providing high-quality electric energy. The MG should be able to operate in both islanded and grid-connected modes. A sudden failure of ac utility grids can lead to an inoperable condition of the MG or a large transient phenomenon accompanied by oscillation and overshoot during the mode transition. This paper proposes a control scheme of the bidirectional dc–dc converter for the ESS to resolve the issue associated with mode switching. The proposed control scheme provides autonomous and smooth mode switching, thereby reducing the reliance on the communication with the central controller, and enhancing the reliability of the system. To validate the proposed concept, simulation results and experimental results are provided.**

***Index Terms*—Autonomous, bidirectional dc–dc converter (BDC), dc microgrid (MG), distributed control, energy storage system (ESS).**

I. Introduction

A SMALL-SCALE grid system based on the concept of smart grids was proposed [1], [2] for small islands, mountains, industrial parks, and remote areas. Such a small-scale grid is called a microgrid (MG). MGs are classified based on the grid type into ac grid, dc grid, and hybrid grid. In recent years, interest in the dc MG system has gradually increased with the growth in the dc coupled subsystems such as photovoltaics, batteries, and LEDs. Noticeable benefits of the dc grid system are that there are no reactive powers, harmonics, and synchronization issues [3], [4]. A typical dc MG system consists of renewable energy sources (RESs), local loads, an energy storage system (ESS), and a voltage source inverter (VSI) as shown in Fig. 1. The RESs are expected to steadily operate at the maximum power point (MPP) regardless of the ac utility grid condition. To balance the power difference between the RESs and local loads, the VSI in connection with the utility grid regulates the dc-bus voltage. The ESS is used to prevent power fluctuations caused by the stochastic characteristics of the RESs that may lead to the instability of the utility grid. Moreover, the ESS is indispensable for energy management tasks such as peak-cut, load shifting, and load leveling. Besides, the ESS should be able to act as a backup power source during a failure of the utility grid when islanded operation is required. During mode switching between the grid-connected mode and the islanded mode, a large transient phenomenon accompanied by oscillation and overshoot may appear because of a sudden failure of the utility grid. The mode switching should be one of the important considerations in the control strategies of the MG [5]–[8]. Several control strategies dealing with mode switching have been presented in [8]–[15]. A possible approach proposed in [11] is that the ESS takes charge of the dc-bus voltage regulation instead of the VSI in both modes, thereby avoiding the issue associated with mode switching. However, in this approach, frequent charging/discharging cycles caused by unpredictable power fluctuations from the RESs and local loads can lead to a reduced battery lifetime [12]. Practically, most of the studies have proposed individual control loops for each mode [8], [12]–[14] although there exists an issue on mode switching.

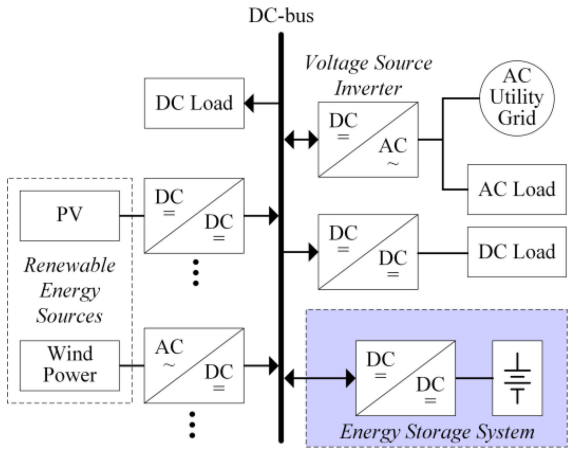

Fig. 1. Typical dc microgrid system.

Coordinated control schemes presented in [14] and [15] are realized in a central controller. In this control scheme, all power conversion units in the MG are controlled by real-time commands from the central controller with a high bandwidth communication link. However, the large distances among the power

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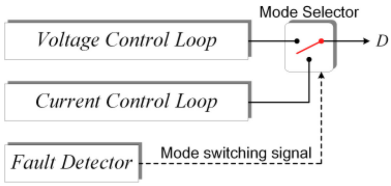


Fig. 2. Concept of the conventional mode switching scheme [12]–[14].

conversion units are an obstacle to the establishment of the high bandwidth communication link. In addition, a communication failure can cause an inoperable condition of the MG. In [9] and [12], distributed control systems operating autonomously with a low bandwidth communication have been proposed to reduce the reliance on the communication with the central controller. This is commonly accepted as an efficient management method in MGs [17], [18].

A mode switching strategy of the bidirectional dc–dc converter (BDC) for ESS is critically important to maintain a stable dc-bus voltage and a steady MPP tracking of RESs even under a failure of the utility grid. In [12]–[14], control schemes of the BDC have been realized with individual control loops which are generally implemented as proportional-integral (PI) compensators according to the control objective such as a dc-bus voltage, battery current, or battery voltage regulation. Fig. 2 shows concept of the conventional mode switching scheme where these two control loops can be interactively interchanged through the mode selector by a fault detector or a command from the central controller. This interchanging can lead to instability due to the transient response inherent in the control loop. Smooth transition between the control loops in Fig. 2 can be achieved by forcing the initial conditions of the inactive PI compensator to the output value of the active PI compensator. However, this approach may suffer from the chattering phenomenon in judging the operating mode. To increase the reliability, it is necessary to have a strategy that can achieve autonomous mode switching without depending on an external signal from the fault detector or the central controller. In [9] and [19], the charging and discharging control loops are combined for autonomous mode switching. However, these methods do not deal with mode switching under the discharging condition.

This paper proposes a control scheme of the BDC for the ESS to resolve the issue associated with the mode switching. In the proposed control scheme, control loops for dc-bus voltage, battery current, and battery voltage are combined by variable limiters, and switching of the control objective of the proposed control scheme is not only autonomous but also smooth, thereby reducing the reliance on the communication and enhancing the reliability of the system. Furthermore, an autonomous and smooth mode switching can be achieved under both charging and discharging conditions, which can contribute to efficient energy management in the grid-connected mode.

II. Proposed Control Scheme

The focus of this paper is to propose a control scheme for BDCs, so a synchronous buck converter is used in this study to implement the proposed control scheme. The block diagram

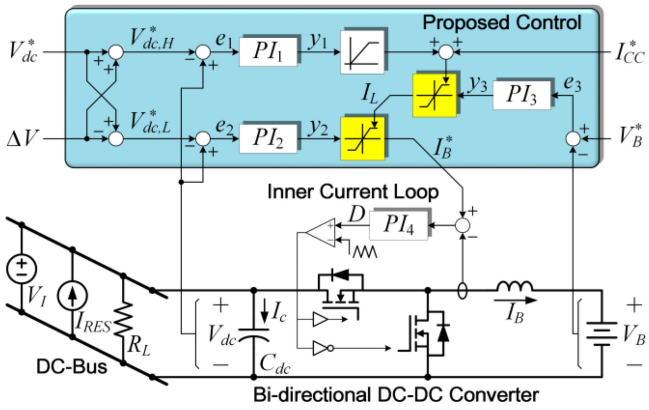


Fig. 3. Control block diagram of the proposed autonomous and smooth control scheme.

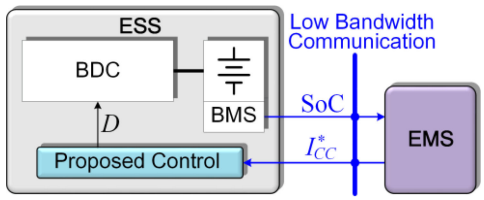


Fig. 4. Interface between the proposed control and the EMS.

of the proposed autonomous and smooth control scheme is shown in Fig. 3. The VSI works as a sole voltage source of the dc-bus, and RESs work at MPP. Therefore, the VSI and RESs can be represented as a voltage source (V_I) and a current source (I_{RES}), respectively. In addition, local loads in the dc MG are represented as a resistor (R_L).

The proposed control scheme consists of four PI compensators and three limiters. The inner closed loop for the battery current control is implemented by a PI compensator (PI_4) using an average current-mode control. The other three outer closed loops for voltage regulation are also implemented by PI compensators (PI_1, PI_2, and PI_3), and their outputs are combined using three limiters. The three PI compensators for the outer loops alternate between saturation and activation according to the dc-bus voltage level, and one of their outputs becomes the battery current reference I_B^*, which is to regulate the dc-bus voltage or the battery voltage. Two of the three limiters are variable limiters of which the upper limit level can be varied.

The battery voltage reference V_B^* is set as the full-charge voltage of the battery. I_{CC}^* is a desired current reference of the battery in the grid-connected mode. To perform the energy management of the MG and the battery management, I_{CC}^* is handled by a central controller such as an energy management system (EMS) as shown in Fig. 4. The references for the dc-bus voltage regulation are set as follows:

$$V_{\mathrm{dc}}^{H^*} = V_{\mathrm{dc}}^* + \Delta V \tag{1}$$

$$V_{\mathrm{dc}}^{L^*} = V_{\mathrm{dc}}^* - \Delta V \tag{2}$$

where V_{dc}^* is a nominal voltage of the dc-bus and is the same with the dc-bus voltage reference of the VSI. Thus, V_{dc}^* equals

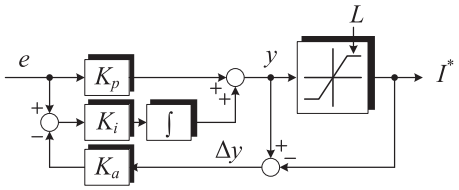


Fig. 5. Block diagram of a PI compensator with a limiter and an antiwindup mechanism for the outer loops.

to V_I in the grid-connected mode. In addition, ΔV is a voltage band for the dc-bus voltage regulation. It must be set within an allowable range of the dc-bus voltage.

The PI compensators for the outer closed loops alternate between saturation and activation according to the operating modes. Therefore, an antiwindup mechanism [20] is indispensable to each PI compensator as shown in Fig. 5.

For saturation of the PI compensator, the output of PI term $y(t)$ can be expressed as follows:

$$y(t) = K_p e(t) + K_i \int e(t) - K_a \left(y(t) - L\right) dt \tag{3}$$

where L is the upper limit level of the limiter and is equal to I^*. The final value of $y(t)$ caused by a constant value of $e(t)$ can be obtained as follows:

$$\lim_{t\to\infty} y(t) = \frac{E}{K_a} + L \tag{4}$$

where E is a constant error. If $e(t)$ is a linear equation with a slope of A, a first-order differential equation can be derived from (3) as follows:

$$\frac{dy(t)}{dt} + K_i K_a y(t) = A\left(K_p + K_i t\right) + K_i E + K_i K_a L. \tag{5}$$

The general solution of (5) can be obtained by

$$y(t) = \frac{A}{K_a K_i}\left(K_p - \frac{1}{K_a} + K_i t\right) + k e^{-K_i K_a t} + y(0) \tag{6}$$

where k is an arbitrary constant. This equation will be used to obtain the mode switching time in Section II-B.

A. Operating Modes

The operating modes of the proposed control scheme can be divided into four categories—constant current (CC) mode, constant voltage (CV) mode, low dc-bus voltage regulation (LDVR) mode, and high dc-bus voltage regulation (HDVR) mode as shown in Figs. 6–9. The equivalent control loops of each mode are based on a general current mode control, called average current mode control, and the inner loop is the same for each mode. It is assumed that the inner closed loop of the proposed controller is well designed to regulate the battery current I_B, and its dynamic bandwidth is sufficiently larger than that of the outer closed loops for voltage regulation.

When the MG is connected to the utility grid, the VSI acts as the sole voltage source V_I for the dc-bus, and therefore, the BDC operates in either the CC mode or the CV mode. When the VSI is incapable of regulating $V_{\rm dc}$ because of the failure of the utility grid, the BDC operates in either the LDVR mode

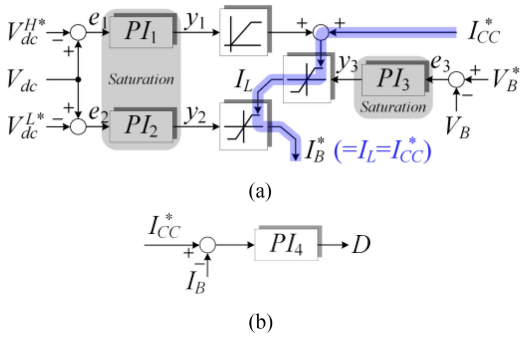


Fig. 6. CC mode of the proposed control scheme (a) showing the activated loop and (b) equivalent control loop.

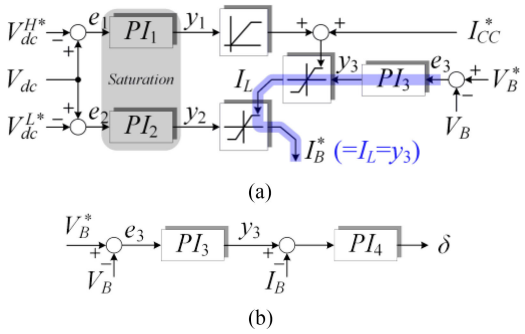


Fig. 7. CV mode of the proposed control scheme (a) showing the activated loop and (b) equivalent control loop.

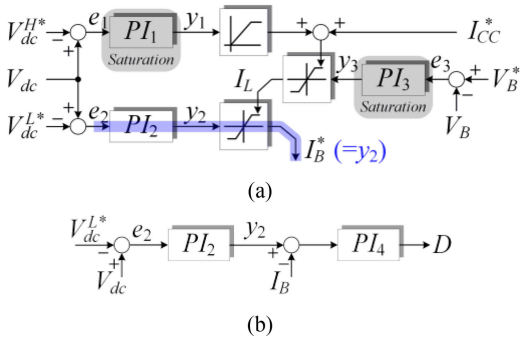


Fig. 8. LDVR mode of the proposed control scheme (a) showing the activated loop and (b) equivalent control loop.

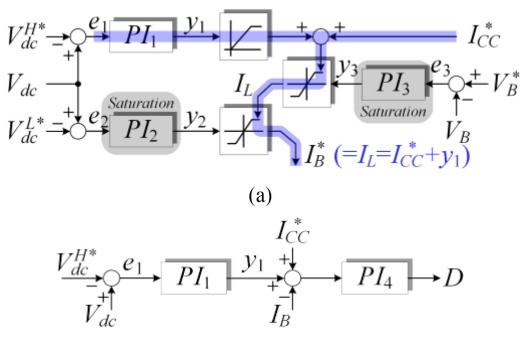


Fig. 9. HDVR mode of the proposed control scheme (a) showing the activated loop and (b) equivalent control loop.

or the HDVR mode in order to regulate the dc-bus voltage. The desired battery current for the dc-bus voltage regulation in the islanded mode can be expressed as follows:

$$I_{\mathrm{dc}}^{*} = \left(I_{\mathrm{RES}} - \frac{V_{\mathrm{dc}}}{R_L}\right)\frac{V_{\mathrm{dc}}}{V_B}. \tag{7}$$

It can be considered as a load condition for the BDC. If I_{CC}^{*} is greater than I_{dc}^{*} when the islanding occurs, the BDC will operate in the LDVR mode; otherwise, the BDC will operate in the HDVR mode. Each mode of the proposed control is described as follows.

1) CC Mode: In this mode, the battery is not fully charged ($V_B < V_B^{*}$), and the dc-bus voltage V_{dc} is determined by V_I and positioned at the middle of $V_{\mathrm{dc}}^{H^{*}}$ and $V_{\mathrm{dc}}^{L^{*}}$. Accordingly, PI_1, PI_2, and PI_3 are all in saturation because of the accumulated voltage errors. From (4), the steady-state outputs of PI_1, PI_2, and PI_3 can be, respectively, obtained as follows:

$$y_1 = \frac{-\Delta V}{K_a}, \tag{8}$$

$$y_2 = \frac{\Delta V}{K_a} + I_{\mathrm{CC}}^{*}, \tag{9}$$

$$y_3 = \frac{V_B^{*} - V_B}{K_a} + I_{\mathrm{CC}}^{*}. \tag{10}$$

As a result, all the outputs of the outer loops have no effect on the current reference I_B^{*} owing to the limiters as shown in Fig. 6(a). Therefore, in this mode, I_B^{*} is equal to I_{CC}^{*}. Consequently, as shown in Fig. 6(b), the battery current is regulated at I_{CC}^{*} which is handled by a central controller. This makes it possible to perform the energy management task from the central controller such as EMS.

2) CV Mode: In this mode, V_B is equal to V_B^{*}, which means that state of charge of the battery is high enough. Thus, the battery voltage error e_3 converges to zero, activating PI_3 to regulate the battery voltage as shown in Fig. 7(b). PI_1 and PI_2 are still in saturation as in the CC mode. In this mode, I_B^{*} is equal to y_3, which becomes the current reference for CV charging as shown in Fig. 7(b).

3) LDVR Mode: This mode occurs when the VSI is disabled under the following condition:

$$I_{\mathrm{CC}}^{*} > I_{\mathrm{dc}}^{*}. \tag{11}$$

This condition denotes that the battery power command by I_{CC}^{*} is greater than the power difference between RESs and local loads, which leads to a decreasing V_{dc} and causes PI_2 to be in activation as shown in Fig. 8(a). Thus, V_{dc} is regulated to be $V_{\mathrm{dc}}^{L^{*}}$. In this mode, I_B^{*} is equal to y_2, which becomes the current reference for regulating V_{dc}. In the meantime, the steady-state output of PI_1 is determined as follows:

$$y_1 = \frac{-2\Delta V}{K_a}. \tag{12}$$

Thus, PI_1 is kept in saturation, and the equivalent control loop can be expressed as shown in Fig. 8(b).

4) HDVR Mode: This mode occurs when the VSI is disabled under the counter-condition of (11). In this mode, V_{dc} increases, thereby causing PI_1 to be in activation as shown in Fig. 7(a). Thus, V_{dc} is regulated to be $V_{\mathrm{dc}}^{H^{*}}$, and therefore, in this mode, I_B^{*} is determined as follows:

$$I_B^{*} = I_L = I_{\mathrm{CC}}^{*} + y_1. \tag{13}$$

In the meantime, the steady-state output of y_2 is determined as follows:

$$y_2 = \frac{2\Delta V}{K_a} + I_{\mathrm{CC}}^{*}. \tag{14}$$

Thus, PI_2 is kept in saturation, and the equivalent control loop can be expressed as shown in Fig. 9(b).

B. Mode Transition

For the sake of simplicity, it can be assumed that I_{CC}^{*}, I_{RES}, I_R, and V_I are constant values during a short period of transition, and the high-frequency switching ripples are neglected.

1) Operating Principle: The four representative cases shown in Fig. 10 are described as follows.

Fig. 10(a) shows the mode transition from the CC mode to the LDVR mode. During the CC mode (before t_1), the dc-bus voltage V_{dc} is being regulated to be V_I by the VSI, and the BDC is charging the battery with a positive value of I_{CC}^{*}, and therefore, the battery voltage V_B is being increased. In the meantime, I_{dc}^{*} is a negative value, which means that the power supplied by RESs is smaller than the power demanded by local loads. At t_1, the VSI regulating V_{dc} is disabled because of the failure of the utility grid, and therefore, V_{dc} goes into a floating (unregulated) state and is determined by

$$V_{\mathrm{dc}}(t) = \frac{I_C}{C_{\mathrm{dc}}}t + V_I \tag{15}$$

where I_C is the instantaneous average current flowing C_{dc} in the floating state of V_{dc} and is determined by the difference between the load condition in the dc-bus and the current reference of the battery as follows:

$$I_C = \left(I_{\mathrm{dc}}^{*} - I_{\mathrm{CC}}^{*}\right)\frac{V_B}{V_{\mathrm{dc}}}. \tag{16}$$

Thus, in this case, V_{dc} decreases, which leads to reducing e_2 and y_2. At t_2, the decreasing y_2 reaches I_{CC}^{*}, which leads to the activation of PI_2, and therefore, V_{dc} starts to be regulated to be $V_{\mathrm{dc}}^{L^{*}}$. After t_2, I_B^{*} starts to decrease from I_{CC}^{*} to I_{dc}^{*}.

The time interval between t_1 and t_2 is defined as mode switching time T_m. The output of PI_2 during T_m can be obtained from (6) and (9) as follows:

$$y_2(t) = \frac{I_C}{C_{\mathrm{dc}}K_aK_i}\left(K_p - \frac{1}{K_a} + K_i(t - t_1)\right) + ke^{-K_iK_a(t-t_1)} + \frac{\Delta V}{K_a} + I_{\mathrm{CC}}^{*} \tag{17}$$

where k can be obtained from the initial value (9) as follows:

$$k = \frac{I_C}{C_{\mathrm{dc}}K_aK_i}\left(\frac{1}{K_a} - K_p\right). \tag{18}$$

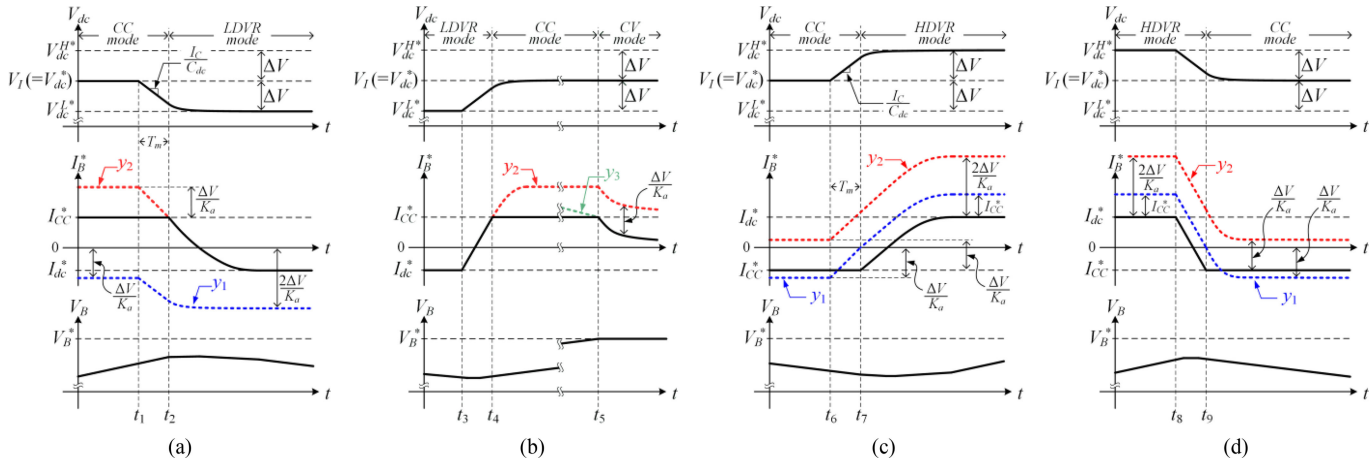


Fig. 10. Key waveforms showing the mode transition (a) from CC mode to LDVR mode, (b) from LDVR mode to CC mode and from CC mode to CV mode, (c) from CC mode to HDVR mode, and (d) from HDVR mode to CC mode.

In this case, PI_1 and PI_3 have no effect on this transition because they are still in saturation.

Fig. 10(b) shows the mode transitions from the LDVR mode to the CC mode and then from the CC mode to the CV mode. When the utility grid is restored to the normal condition, the VSI can restart to regulate $V_{\rm dc}$. At t_3, $V_{\rm dc}$ and I_B^* start increasing with the restarting of the VSI. Their increasing slopes are determined by the dynamic performance of the VSI. At t_4, I_B^* reaches $I_{\rm CC}^*$, which leads to the saturation of PI_2, and therefore, the BDC goes into the CC mode. At t_5, y_3 meets $I_{\rm CC}^*$ because the increasing V_B reaches V_B^*, thereby activating PI_3, and therefore, the BDC goes into the CV mode.

Fig. 10(c) shows the mode transition from the CC mode to the HDVR mode. Before t_6, the BDC operates in the CC mode with a negative value of $I_{\rm CC}^*$, and $I_{\rm dc}^*$ is a positive value. From (19) and (20), $V_{\rm dc}$ starts to increase after the VSI is disabled at t_6. At t_7, y_1 reaches zero, which leads to the activation of PI_1, and therefore, $V_{\rm dc}$ starts to be regulated to be $V_{\rm dc}^{H^*}$. The output of PI_1 during T_m can be obtained from (6) and (8) as follows:

$$y_1(t) = \frac{I_C}{C_{\rm dc}K_aK_i}\left(K_p - \frac{1}{K_a} + K_i(t-t_6)\right) + ke^{-K_iK_a(t-t_6)} - \frac{\Delta V}{K_a} \tag{19}$$

where k is the same as in (22).

Fig. 10(d) shows the mode transition from the HDVR mode to the CC mode. At t_8, $V_{\rm dc}$ and I_B^* start decreasing with the restarting of the VSI. At t_9, y_1 reaches zero, which leads to the saturation of PI_1, and therefore, the BDC goes into the CC mode.

2) Mode Switching Time: From (17) to (19), the mode switching time T_m in Fig. 10 can be derived and expressed using the Lambert-W function [21] as follows:

$$T_m = \frac{1}{K_iK_a}\left(1 + W\left[\left(K_pK_a - 1\right)e^{K_iK_aC_{\rm dc}\Delta V/I_C + K_pK_a - 1}\right]\right) - \frac{C_{\rm dc}\Delta V}{I_C} - \frac{K_p}{K_i}. \tag{20}$$

TABLE I
PI GAINS OF THE OUTER LOOPS

	PI_1	PI_2	PI_3
K_p	1.4	1.4	0.7
K_i	200	200	20

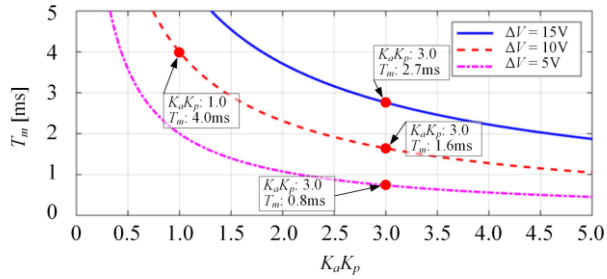


Fig. 11. Mode switching time as a function of K_a for different ΔV.

Here, T_m is mainly dependent on the antiwindup gain K_a, the voltage band ΔV, and I_C. The others are preferentially determined by the dynamic performances, stability, or hardware specifications of the BDC. The control parameters of the PI compensators are listed in Table I. Their design procedure for the proposed control is not different with that for the conventional BDC because the control loop of each mode is based on a general current mode control. Using (20), T_m has been plotted as a function of K_a for different ΔV in Fig. 11 under the condition listed in Table II. A small T_m means a reduced transient state right after the mode switching. In order to reduce T_m, K_a should be increased. However, increasing the value of K_a too much will lead to interference among the three outer loops resulting from the sampling inaccuracies and small perturbations. The interference may also occur if the value of ΔV used is too small. On the contrary, if ΔV is too large, the BDC operates with a low voltage and a high current, leading to low efficiency and overcurrent faults [9]. Hence, K_a and ΔV should be carefully chosen. In addition, the different levels of the dc-bus voltage

TABLE II
PARAMETERS USED IN SIMULATION AND EXPERIMENTAL

Parameter	Symbol	Value	Unit
Nominal dc-bus voltage ($= V^*_{\rm dc}$)	V_I	200	V
CV reference	V^*_B	80	V
CC reference	$I^*_{\rm CC}$	5	A
Battery voltage	V_B	70	V
Generated current from RES	$I_{\rm RES}$	1.25	A
Local load resistance	R_L	80	Ω
Filter inductance	L_f	360	μH
DC-bus capacitance	$C_{\rm dc}$	1.2	mF
Switching frequency	f_s	50	kHz

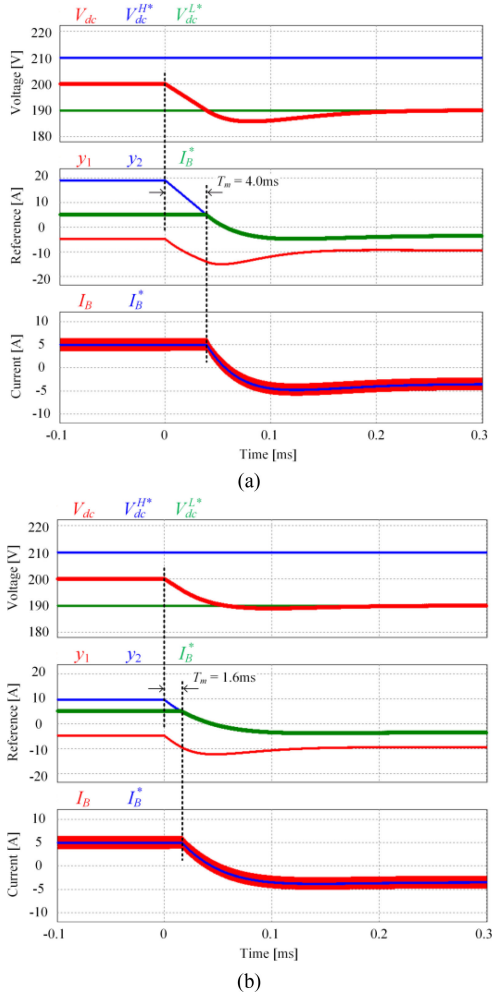


Fig. 12. Simulation waveforms in different K_a. (a) $K_aK_p = 1$. (b) $K_aK_p = 3$.

according to ΔV can be utilized as a signal indicating the status of the MG, which is called the dc-bus voltage signaling [22].

Fig. 12 depicts the simulation waveforms showing T_m in different K_a under the conditions listed in Tables I and II. Note that the different values of T_m measured from the simulations correspond to the theoretically obtained values of T_m shown in Fig. 11.

In addition, the magnitude of I_C, which means the load condition for the BDC to be changed when the mode is switched, affects T_m because it depends on the slope of the voltage error during T_m. Fig. 13 shows a trend of T_m as a function of K_a

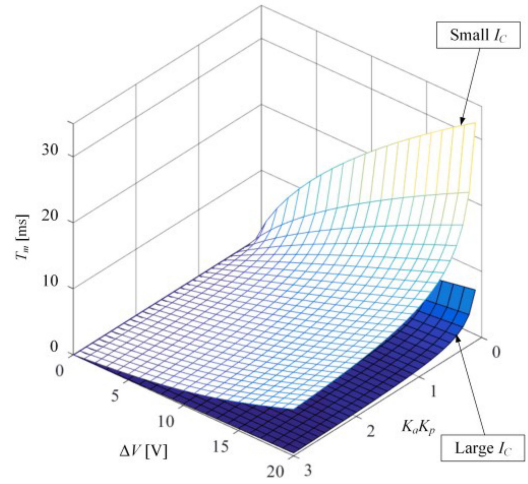


Fig. 13. Mode switching time according to K_a and ΔV for different magnitudes of I_C.

and ΔV in different I_C. In case of a small magnitude of I_C, T_m can be dramatically increased, especially, when using a small K_a and a large ΔV. However, this case means a little change of I^*_B during the mode transition; therefore, the transient on $V_{\rm dc}$ will be trivial even if T_m is large. Fig. 14 shows the simulation waveform to compare the transient state for different values of I_C. In case of a greater R_L, the transient state on $V_{\rm dc}$ is better in spite of the longer T_m.

III. CONTROL SCHEME FOR MULTIPLE ESS

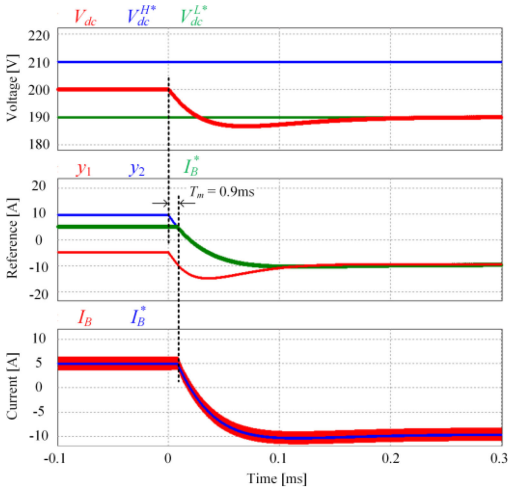
In an MG system consisting of multiple ESS, there is no issue for power-sharing between ESSs in the case of the grid-connected mode because all ESSs perform their own power control according to supervision of a central controller. However, in the case of the islanded mode, the ESSs should regulate the dc-bus voltage, and therefore a power-sharing strategy is required to prevent circulating power and functional disorder. To cope with this problem, dc droop control has been proposed [17], [23]. The droop control allows not only power-sharing but voltage regulation. Fig. 15 shows the proposed control scheme for multiple ESS in the dc MG. In primary control, the dc-bus voltage reference for the proposed control ($V^*_{\rm dc}$) is adjusted by the output of the dc droop control and is determined by the dc-bus side current of the BDC ($I_{\rm dc}$) and the virtual output impedance (R_d). The droop control has an inherent load-dependent voltage deviation of which the maximum value can be expressed as follows:

$$\varepsilon_v = 2R_d I_{\rm dc,max}. \tag{21}$$

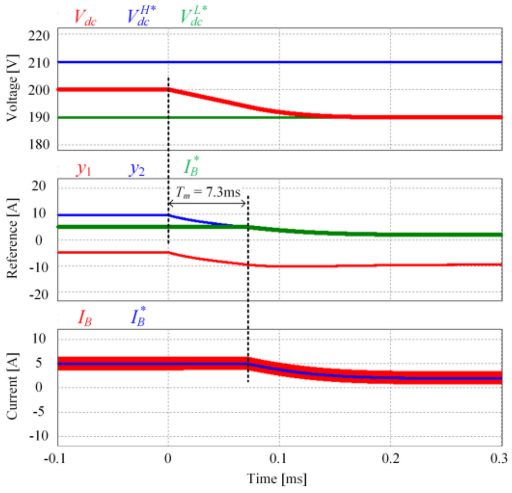
Unfortunately, in the islanded mode, the proposed control also has an inherent dc-bus voltage deviation which is $\pm\Delta V$. Droop curve showing the voltage deviation is illustrated in Fig. 16. Thus, total voltage deviation caused by the droop and proposed control is as follows:

$$\Delta V_{\rm tot} = \varepsilon_v + 2\Delta V. \tag{22}$$

The voltage deviation could be considerable, especially in a high power system. To overcome this problem, an external



(a)



(b)

Fig. 14. Simulation waveforms in different R_L with $K_a K_p = 3$. (a) $R_L = 40\ \Omega$. (b) $R_L = 400\ \Omega$.

secondary control is employed, which performs compensation for the voltage deviation by feedback of the dc-bus voltage [17]. The compensated value δV is transferred to all ESSs by the low bandwidth communication. Thus, the reference of the dc-bus voltage for the proposed control is determined as follows:

$$V_{\rm dc}^* = V_{\rm dc0}^* - R_d I_{\rm dc} + \delta V \tag{23}$$

where $V_{\rm dc0}^*$ is the reference of the dc-bus voltage at no load and is set as the nominal value of the dc-bus voltage.

Fig. 17 shows the simulation results of the mode switching followed by droop control of two ESSs connected in common dc-bus to show the feasibility of power-sharing of multiple ESS in the dc MG. The simulation condition is listed in Table III. For the sake of simplicity, RESs in the dc MG are omitted. Before 0.2 s, both converters are being operated in the CC mode with the same current reference. After the VSI regulating, $V_{\rm dc}$ is turned OFF at 0.2 s, the operating mode of both converters is autonomously switched to the LDVR mode, and then the local load in the dc MG is increased at 0.4 s. In the islanded mode, the battery currents are regulated at different values for the power-sharing because the battery voltages are different from each other. It is seen that the dc-bus side current ($I_{\rm dc}$) sharing is well achieved although the line impedance and battery conditions are different from each other. Fig. 17(a) shows the simulation result with the primary control only. It shows that the voltage deviation is increased proportionally to the load in the islanded mode. Fig. 17(b) shows that the voltage deviation is compensated by employing the secondary control.

The secondary control compensates the voltage deviation caused by not only the droop control but also the proposed control. Hence, it can also be utilized for the single ESS equipped application in order to compensate the voltage deviation inherent in the proposed control.

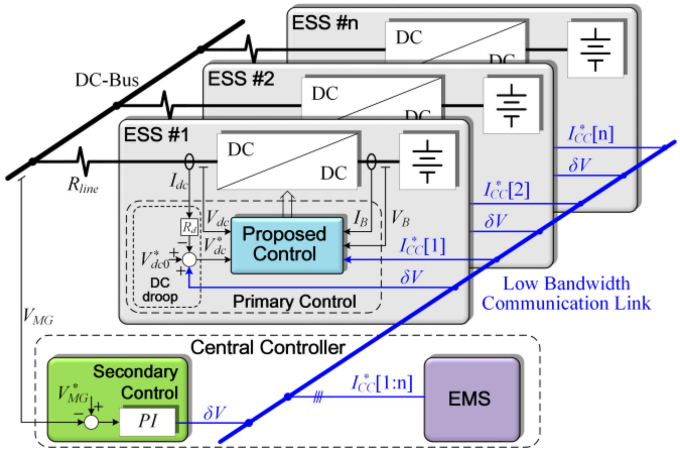


Fig. 15. Proposed control scheme for multiple ESS.

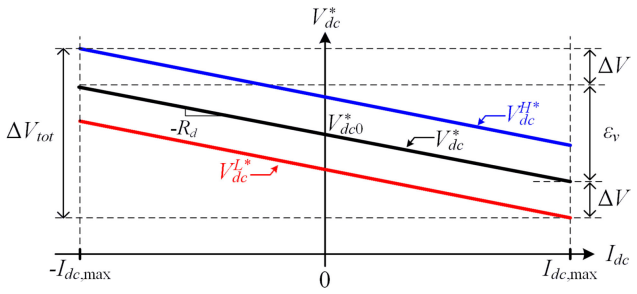


Fig. 16. Droop curve of the proposed control scheme.

TABLE III
PARAMETERS USED IN DROOP SIMULATION

Parameter	Symbol	ESS #1	ESS #2
Battery voltage	V_B	80 V	120 V
Line impedence	$R_{\rm line}$	0.1 Ω	0.2 Ω
DC-bus voltage reference	$V_{\rm dc0}^*$, $V_{\rm MG}^*$	200 V	
CC reference	$I_{\rm CC}^*$	5 A	
Virtual impedence	R_d	1.7 Ω	
Voltage deviation of the proposed control	ΔV	10 V	

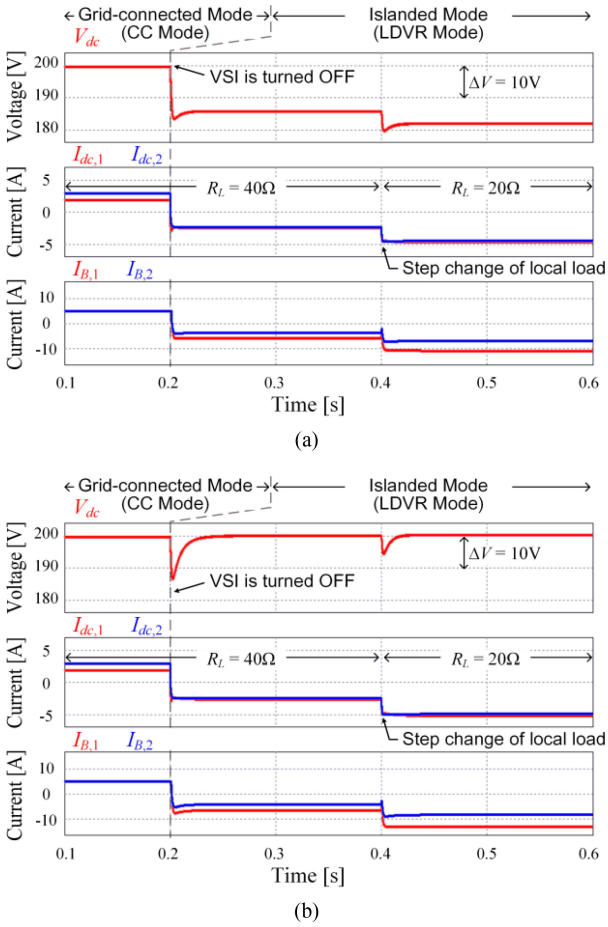


Fig. 17. Simulation waveforms of the mode switching followed by droop control (a) without secondary control and (b) with secondary control.

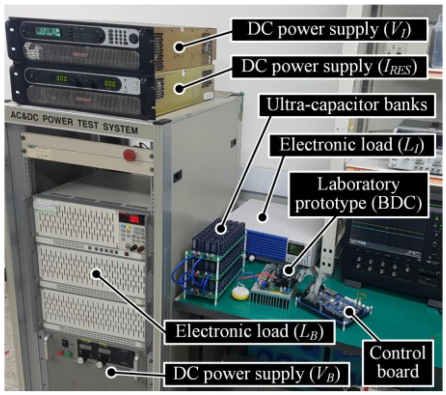


Fig. 18. Experimental setup.

IV. Experimental Results

To demonstrate the theoretical analysis of the proposed control scheme, a laboratory prototype using the synchronous buck has been built. The specifications and PI gains of the prototype are the same as those in the simulation listed in Tables I and II. Three programmable dc power supplies (V_I, V_B, and I_{RES}), two electronic loads (L_I and L_B), and a resistor (R_L) are used for the experimental setup as shown in Fig. 18. In addition, three parallel ultracapacitor (UC) banks are used in the experiment for the CV mode. Each of the UC banks consists of 50 UC connected in series. Each UC is implemented by LSUC002R80100FEA (100 F/2.8 V) from LS. A controller for realizing the proposed control scheme is implemented by a 32-bit digital signal processor (TMS320F28335 from TI).

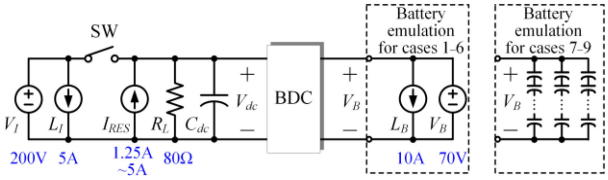


Fig. 19. Schematic diagram for experiment.

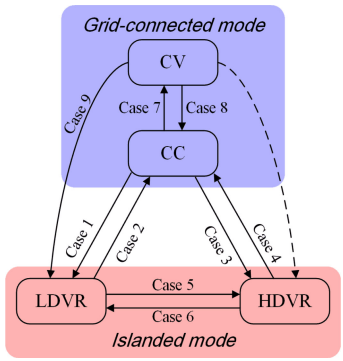
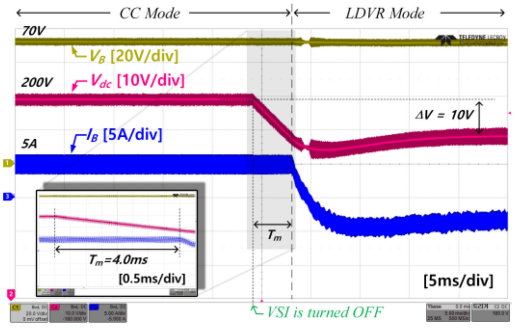


Fig. 20. All possible mode switching cases.

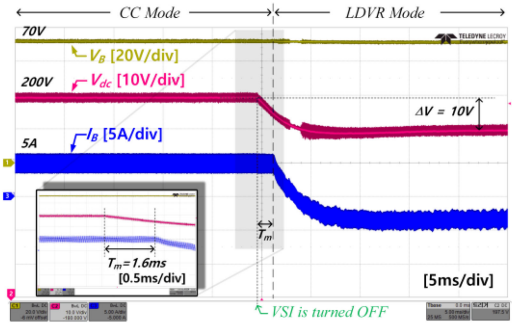
Fig. 19 shows the schematic diagram for experiment. The VSI is emulated by V_I in parallel with L_I. I_{RES} and R_L are implemented to emulate RESs and local loads, respectively. The battery is emulated by either V_B in parallel with L_B or the UC banks. The circuit breaker (SW) is implemented to simulate a failure of the utility grid.

All the possible cases of mode switching in the dc MG system are indicated in Fig. 20. Fig. 21 shows the experimental result for case 1 using different values of K_a under the same value of ΔV. V_{dc} starts to decrease when the SW is turned OFF, but the battery current I_{B} is kept at 5 A for a short time, which can be regarded as the mode switching time T_m. In case of the larger K_a, T_m is shorter, and V_{dc} has a smaller undershoot. The mode transition using different values of ΔV is shown in Fig. 22. Note that the different values of T_m shown in Figs. 21 and 22 also correspond to the theoretically obtained values of T_m shown in Fig. 11.

Case 2 occurs when the SW is closed while BDC operates in the LDVR mode. With turning ON the SW, V_{dc} starts increasing in order to be restored to the nominal dc-bus voltage, and the operating mode of the BDC is autonomously switched to the CC mode as shown in Fig. 23. In this transition, the slopes of V_{dc} and I_B are determined by the dynamic performance of the VSI. Fig. 24 shows the experimental result for cases 3 and 4 under the following conditions: $I_{\mathrm{RES}} = 4\,\mathrm{A}$; $I^*_{\mathrm{CC}} = -5\,\mathrm{A}$. While the battery is discharged in the CC mode, the SW is turned OFF, and then V_{dc} starts to increase because the power injected into the dc-bus from the RES and battery is greater than the power

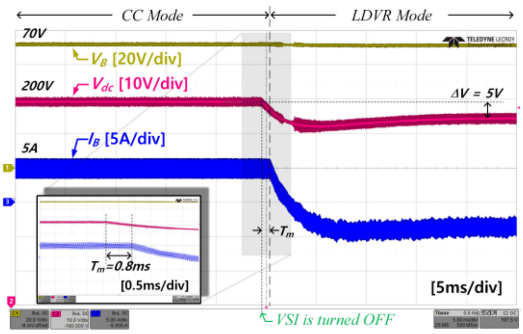


(a)

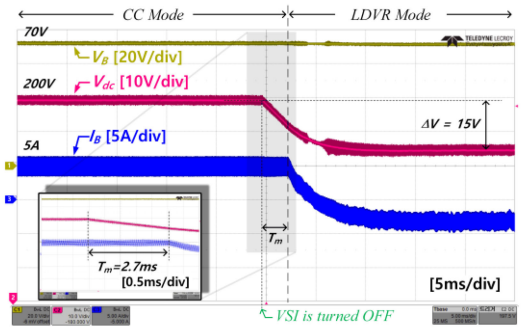


(b)

Fig. 21. Experimental waveforms showing case 1 in different K_a ($\Delta V = 10$ V). (a) $K_a K_p = 1$. (b) $K_a K_p = 3$.



(a)



(b)

Fig. 22. Experimental waveforms showing case 1 in different ΔV ($K_a K_p = 3$). (a) $\Delta V = 5$ V. (b) $\Delta V = 15$ V.

consumption of R_L, leading to the switching to the HDVR mode as shown in Fig. 24(a). And then after the SW is turned ON, $V_{\rm dc}$ goes back to the nominal dc-bus voltage as shown in Fig. 24(b).

Cases 5 and 6 can occur with a sudden change of the amount of power generated by RESs under the islanded mode. Figs. 25 and 26 show the experimental waveforms in the islanded mode under step increase and decrease in $I_{\rm RES}$. As shown in Fig. 25, $I_{\rm RES}$ is increased from 1.25 to 2.5 A but the BDC is still in the LDVR mode because the changed $I_{\rm RES}$ is not greater than I_R. Fig. 26 shows the step increase of $I_{\rm RES}$ from 1.25 to 5 A under $I^*_{\rm CC} = 1$ A. The increased $I_{\rm RES}$, which is greater than I_R, leads to an increase in $V_{\rm dc}$, and therefore, the operating mode is switched from the LDVR mode via the CC mode to the HDVR mode. In the islanded mode, power fluctuations from the RESs and local loads can cause frequent switching of the operating mode, which leads to undesirable voltage fluctuation of the dc-bus. To cope with this problem, $I^*_{\rm CC}$ is set to its maximum value after the islanding. Thereby, the operating mode will be kept in the LDVR mode as long as the battery is neither fully charged nor fully discharged.

The UC banks are used in the experiment for cases 7–9. Fig. 27(a) shows the experimental waveforms for case 7 under $I^*_{\rm CC} = 5$ A. The experiment for case 8 is simulated varying $I^*_{\rm CC}$ (from 5 to –5 A) in the CV mode as shown in Fig. 27(b). Fig. 27(c) shows the experimental waveforms for case 9. Note that all the experimental results demonstrate autonomous and smooth mode transition.

The dashed line in Fig. 20 corresponds to an operation that could lead to an unmanageable excess of energy. In this case, the dc-bus voltage is better to be regulated by a converter for

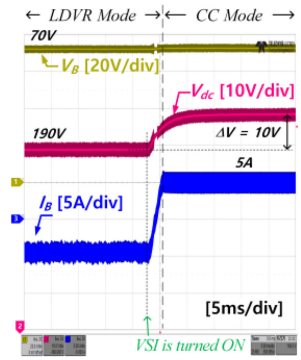
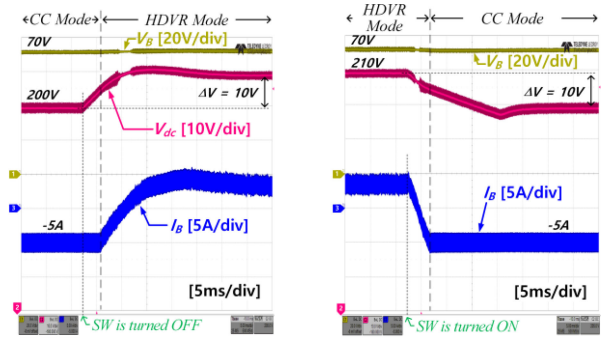


Fig. 23. Experimental waveforms showing case 2.



(a) (b)

Fig. 24. Experimental waveforms ($I_{\rm RES} = 4$ A, $I^*_{\rm CC} = -5$ A, $K_a K_p = 3$, $\Delta V = 10$ V). (a) Case 3. (b) Case 4.

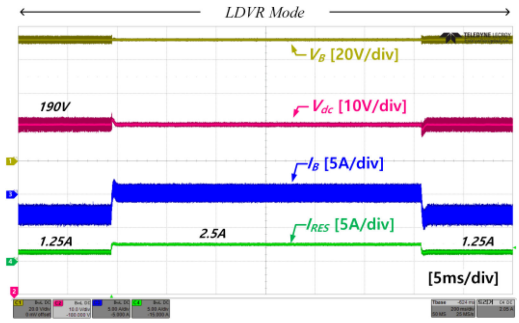


Fig. 25. Experimental waveforms in an islanded mode under step changes in I_{RES}.

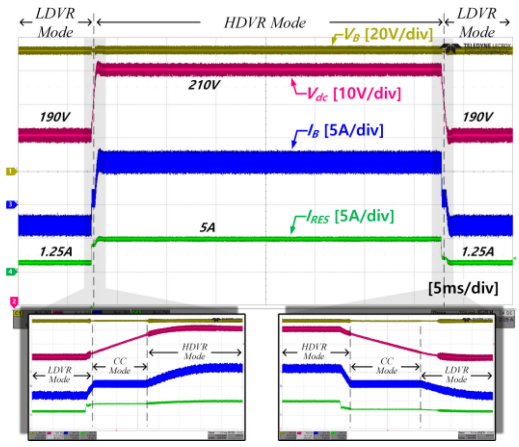


Fig. 26. Experimental waveforms in an islanded mode under step changes in I_{RES} (showing cases 5 and 6).

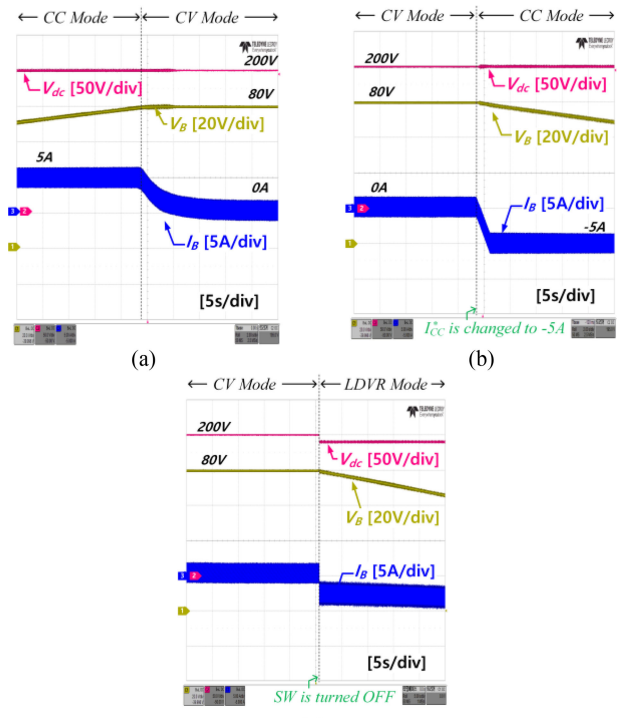


Fig. 27. Experimental waveforms using the ultracapacitor bank. (a) Case 7. (b) Case 8. (c) Case 9.

an RES even though MPP tracking cannot be achieved [9]. This case is not considered in this paper.

V. Conclusion

In this paper, a control scheme of the BDC for ESS has been proposed to resolve the issue associated with mode switching. The proposed control scheme is capable of autonomously altering the control objective even without the supervision of the central controller. Furthermore, a smooth switching between the three outer loops is obtained using variable limiters.

By analysis of the transition between the activation and saturation of PI compensators, the mode switching time has been derived. In addition, the dominant factors improving the transient performance during the mode transition have been analyzed. The experimental results corresponding to the theoretical analysis demonstrate the validity of the proposed control scheme.

References

[1] R. H. Lasseter and P. Paigi, "Microgrid: A conceptual solution," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2004, pp. 4285–4290.
[2] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, "Microgrids," *IEEE Power Energy Mag.*, vol. 5, no. 4, pp. 78–94, Jul./Aug. 2007.
[3] J. Lee *et al.*, "DC micro-grid operational analysis with a detailed simulation model for distributed generation," *J. Power Electron.*, vol. 11, no. 3, pp. 350–359, May 2011.
[4] D. E. Olivares *et al.*, "Trends in microgrid control," *IEEE Trans. Smart Grid*, vol. 5, no. 4, pp. 1905–1919, Jul. 2014.
[5] F. Katiraei, M. R. Iravani, and P. W. Lehn, "Micro-grid autonomous operation during and subsequent to islanding process," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 248–257, Jan. 2005.
[6] N. Eghtedarpour and E. Farjah, "Control strategy for distributed integration of photovoltaic and energy storage systems in dc micro-grids," *J. Renewable Energy*, vol. 45. pp. 96–110, Sep. 2012.
[7] S. Lu, L. Wang, T. Lo, and A. V. Prokhorov, "Integration of wind power and wave power generation systems using a dc microgrid," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 2753–2761, Jul./Aug. 2015.
[8] L. Xu and D. Chen, "Control and operation of a dc microgrid with variable generation and energy storage," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2513–257, Oct. 2011.
[9] K. Sun, L. Zhang, Y. Xing, and J. M. Guerrero, "A distributed control strategy based on dc bus signaling for modular photovoltaic generation systems with battery energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 3032–3045, Oct. 2011.
[10] H. Kakigano, Y. Miura, T. Ise, and R. Uchida, "DC micro-grid for super high quality distribution – System configuration and control of distributed generations and energy storage devices –," in *Proc. 37th Annu. IEEE Power Electron. Spec. Conf.*, 2006, pp. 3148–3154.
[11] P. Arboleya *et al.*, "Efficient energy management in smart micro-grids: Zero grid impact buildings," *IEEE Trans. Smart Grid*, vol. 6, no. 2, pp. 1055–1063, Mar. 2015.
[12] T. Dragicevic, J. M. Guerrero, J. C. Vasquez, and D. Skrlec, "Supervisory control of an adaptive-droop regulated dc microgrid with battery management capability," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 695–706, Feb. 2014.
[13] Y. Zhang and Y. W. Li, "Energy management strategy for supercapacitor in droop-controlled dc microgrid using virtual impedance," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2704–706, Apr. 2017.
[14] X. Liu, P. Wang, and P. C. Loh, "A hybrid ac/dc microgrid and its coordination control," *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 278–257, Jun. 2011.
[15] P. Sanjeev, N. P. Padhy, and P. Agarwal, "Peak energy management using renewable integrated dc microgrid," *IEEE Trans. Smart Grid*, 2017, to be published.
[16] A. G. Tsikalakis and N. D. Hatziargyriou, "Centralized control for optimizing microgrids operation," *IEEE Trans. Energy Convers.*, vol. 23, no. 1, pp. 241–248, Mar. 2008.

[17] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. De Vicuña, and M. Castilla, "Hierarchical control of droop-controlled ac and dc microgrids–A general approach toward standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, Jan. 2011.
[18] S. Moayedi and A. Davoudi, "Distributed tertiary control of dc microgrid clusters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1717–1733, Feb. 2016.
[19] J. Park and S. Choi, "Design and control of a bidirectional resonant dc–dc converter for automotive engine/battery hybrid power generators," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3748–3757, Jul. 2014.
[20] S. Sul, "Design of regulators for electric machines and power converters," in *Control of Electric Machine Drive System*, Piscataway, NJ, USA: Wiley, 2011, pp. 170–173.
[21] S. Yi, P. W. Nelson, and A. G. Ulsoy, *Time-Delay Systems: Analysis and Control Using the Lambert W Function*, Singapore: World Scientific, 2010.
[22] J. Schönberger, R. Duke, and S. D. Round, "DC-bus signaling: A distributed control strategy for a hybrid renewable nanogrid," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1453–1460, Oct. 2006.
[23] X. Lu *et al.*, "An improved droop control method for dc microgrids based on low bandwidth communication with dc bus voltage restoration and enhanced current sharing accuracy," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1800–1812, Apr. 2014.

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