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A Compact 17.6 kW Single-/22 kW Three-Phase Compatible EV Charger: Analysis of Active Power Decoupling, Wide Voltage Range Operation

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Abstract-In this article, a single- and three-phase compatible battery charger with active power decoupling (APD) is proposed. The two-stage system consists of CLLC resonant converter for dc-dc converter and integration of two-level inverter (three-phase) and three-phase interleaved totem-pole inverter (single-phase) for ac-dc converter. Through the simple relay operation, the ac-dc converter switches the operations according to the grid phase. By applying the active power decoupling technique to reduce the used capacitance and substitute to film capacitor, it solves the problems of lifespan and stability caused by using electrolytic capacitors. The ac-dc converter variably control the dc link voltage to maximize the battery voltage range of the DCX region with good efficiency characteristics for the dc-dc converter. In addition, the CLLC resonant converter performs the seamless control combining with frequency control and phase-shift control by using only one PI controller. A 17.6/22 kW(1Ø/3Ø), 2.18 kW/L prototype is implemented to validate the proposed concept and demonstrated 95.77% and 94.98% peak efficiency for three- and singlephase, respectively.

Index Terms—Active power decoupling (APD), bidirectional battery charger, CLLC resonant converter, single- and three-phase compatible system, wide battery voltage range.

I. INTRODUCTION

S INCE the beginning of the 21st century, electric vehicles (EVs) have emerged as a viable alternative to internal combustion engine vehicles to reduce greenhouse gas emissions. Despite being eco-friendly and sustainable use, there are many

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obstacles to EV development as limited mileage and long charging time for battery. Therefore, a high-capacity battery is essential to increase the vehicle mileage. In addition, it is necessary to increase the power level of the on-board charger (OBC) to shorten the charging time. As shown in Fig. 1, a 3.3/6.6 kW/L battery charger trends become 11/22 kW/L which means the reformation in the usable voltage range of the lithium-ion battery (400 V \rightarrow 800 V) [1]. The power density of OBC is a very important factor because the interior space of the vehicle is limited regardless of the increase in OBC power level [2], [3]. Therefore, the main way to increase power density is to use wide band-gap (WBG) devices to achieve low power dissipation and high switching frequency operation, thereby reducing the design value and volume of passive components [4], [5].

Single-phase OBCs are commonly used worldwide due to the availability of single-phase grid input [2], [6]. Single-phase grid input can be used in certain areas (i.e., the US and Japan), where there are facilities that only provide single-phase. However, the three-phase grid provides higher charging power to the vehicle, which shortens the charging time of the battery. Thus, automakers are offering EV owners another option, a three-phase grid, to

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Fig. 2. Single- and three-phase grid voltage range according to a wide battery voltage range during battery charging/discharging operation.

charge their vehicles wherever adequate ac power is available. In particular, EVs equipped with three-phase OBC are increasing in the European market because charging infrastructure by three-phase grid is dominant [7], [8], [9]. Therefore, as shown in Fig. 2, it is commercially valuable to design a universal OBC compatible with the single- and three-phase grid input that is easily used in public places and homes around the world [10].

A commercial two-stage OBC is consist of a power factor correction (PFC) stage and an isolated dc-dc stage with a dc link electrolytic capacitor [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. The modular-type of the two-stage structure [11], [12], [13], [14], [15], [16], [17], [18], [19], [20] performs the three-phase operation with the three-phase input, and the parallel-operation with single-phase input. A nonmodular type that is compatible with single- and three-phase input by turning ON and OFF the relays at the grid terminal [21], [22], [23]. Due to the development of WBG devices (low $R_{ds.on}$, fast rising time t_r and falling time t_f , there is no need to parallelize the switches. Thus, the universal grid input operation is possible only by changing the relay structure and topology operation according to the grid input conditions. Furthermore, it has significant advantages in terms of price competitiveness and power density since the number of components is quite low.

However, single-phase battery chargers have their own power ripple component that fluctuates with twice the grid frequency in both situations mentioned above, resulting in dc link voltage ripple. Typically, a bulky dc link capacitor is used to absorb the second low-frequency components, which is an important barrier to achieving the high power density of OBC. To deal with the high voltage rating of 800 V at the three-phase grid input, it is implemented in series and parallel connection to satisfy the same capacitance compared to the 400 V electrolytic capacitor structure, resulting in four times the capacitor volume [17]. Also, electrolytic capacitor of the dc link has a short lifespan, which reduces the reliability of OBC. Furthermore, the overall two-stage structure released on the EV charger market have a power density of less than 1.7 kW/L. Even if the volume of several passive components is reduced by increasing the switching frequency with the WBG devices, the portion of the dc link electrolytic capacitor related to the second low-frequency component of grid frequency becomes larger in the total hardware volume [17]. Therefore, there is a need for a new technology that has cost and volume advantages while replacing electrolytic capacitors to improve power density.

Moreover, the other challenge of OBC is a bidirectional operation for grid supports with wide voltage range operating capability. BRUSA Elektronik AG develops the OBC product [24] that reports the 22 kW three-phase operation with variable dc link control for wide voltage operation. However, the battery voltage range is limited to the range of 310–430 V due to the full DCX operation of the dc–dc converter. In single-phase operation, the power is limited to 7.4 kW. Li et al. [17] reports the design of a 6.6 kW prototype with variable dc link control of the PFC stage and near DCX control of the dc–dc stage. The output battery voltage is limited in the range of 250–450 V. Further discussion on wide voltage operation is not provided.

This article proposes a nonmodular two-stage battery charger that is compatible with single- and three-phase grid input, where each operation is easily switched by a relay structure. For the single- and three-phase grid, the operations are two-level inverter and three-phase interleaving totem-pole inverter, respectively, and the rated power is 22 kW and 17.6 kW under battery charging mode. The proposed two-stage system suggests a solution by applying an active power decoupling circuit to cope with the volume and stability problems of the existing OBC due to the use of electrolytic capacitors (four times increase for an 800 V battery system). The CLLC resonant converter achieves seamless control combining the frequency control and phase-shift control using only one PI controller. Furthermore, the dc-dc converter obtains DCX operation over a wide battery voltage range since the ac-dc converter variably controls the dc link voltage. The operation and control strategy and experimental results of the proposed two-stage system are described in detail. Contributions of this article are summarized as follows:

- This article presents a trending design of a high power 22 kW (3Ø)/17.6 kW (1Ø) OBC that is compatible with universal single- and three-phase grid input.
- 2) Proposed an active power decoupling circuit to eliminate the electrolytic capacitors for increasing the lifespan of the converter.
- 3) OBC can operate under wide voltage by the proposed modulation method that utilizes the both frequency and phase shift of the CLLC converter, and the variable dc link control of the PFC converter (the output battery voltage range is from 360 V to 845 V).
- Seamless mode change (Phase-shift ↔ Frequency) and start-up sequence to prevent transient-state cause damage to major components.
- Bidirectional EV charger capable of V2G (11 kW) and G2V (22 kW/17.6 kW) with 2.18 kW/L high-power density.

II. DERIVATION OF THE ONBOARD BATTERY CHARGER TOPOLOGIES

Fig. 3(a) shows the circuit diagram of the proposed on-board battery charger; it consists of single- and three-phase ac-dc converter, active power decoupling circuit and CLLC resonant converter. For single- or three-phase grid input, the PFC operations are switched by the input relay structure. In single-phase operation, a decoupling circuit is applied for replacing the use of electrolytic capacitors. The CLLC resonant converter performs optimal operation over a wide battery voltage range at full load condition.

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Fig. 3. Overall configuration of the ac–dc converter. (a) Comprehensive circuit diagram. (b) Three-phase operation. (c) Single-phase operation.



Fig. 4. Comparison of capacitance. (a) Conventional design for twostage. (b) Design for active power decoupling (APD).

A. Concept of Topologies Deriving From APD and OBC

Fig. 3(a) shows the conceptual structure of the proposed single- and three-phase compatible EV charger for the dc charging, and it is differently expressed into Fig. 3(b) and 3(c) according to the grid input. The proposed charger is a two-stage circuit consisting of ac-dc converter + CLLC resonant converter, and the electrolytic capacitor is replaced by a film capacitor by using an active decoupling circuit.

For three-phase charging, as shown in Fig. 3(b), all input relays are turned off and switches S_{7-10} for low-frequency switching are disabled. In addition, the decoupling circuit is disable, so that single module with a two-stage structure is able to transfer the dc output. A three-phase single module can handle up to 22 kW of power rating under battery charging mode. Conversely, it can discharge up to 11 kW of power rating. As shown in Fig. 3(c), the mode change three-phase operation to the single-phase operation by connecting the grid line-to-line relays and neutral line relay.

Unlike the three-phase operation, the PFC circuit configuration of single-phase operates as a three-phase interleaved totem-pole that consist of high frequency switches S_{1-6} and low-frequency switches S_{7-10} . In addition, as shown in Fig. 4, the electrolytic capacitors is able to be replaced with film capacitors by using a buck-type decoupling circuit to cancel the even harmonic ripples in the system. A single-phase single module can handle up to 17.6 kW (220 V × 80 A) of power rating under battery charging mode. Conversely, it can discharge up to 11 kW of power rating.

B. Operation Principle of Proposed OBC

A representative operation waveform of the proposed twostage system is shown in Fig. 5. The sequence for each mode is described as follows.



Fig. 5. Representative operation sequence.

Mode 1 ($t_0 \sim t_1$): DC link precharging mode. Charge the dc link voltage to the peak value of the grid line-to-line voltage (3Ø) and the peak value of the grid phase voltage (1Ø).

Mode 2 ($t_1 \sim t_2$): DC link voltage control. To prevent excessive current injection into the dc link capacitor, the link voltage is controlled with a constant slope operation rather than a step operation.

Mode 3 ($t_2 \sim t_3$): Decoupling capacitor average voltage control. Only valid in grid single-phase system. The decoupling capacitor voltage is controlled from 0 to (0.707 × v_{dc}) with a constant slope.

Mode 4 ($t_3 \sim t_4$): Decoupling capacitor average voltage control + PR control of even harmonic components. Only valid in grid single-phase system. A PR controller of single-phase system for even harmonic components are included in addition to the decoupling average voltage controller. Until the time t_4 , the reference value of power tracking is still zero.

Mode 5 ($t_4 \sim t_5$): Power control of CLLC resonant converter. The PFC-stage maintains the operation of *Mode 4*, and the CLLC converter of dc–dc stage performs power control with a constant slope. At light load, CLLC resonant converter control the system power by controlling the phase-shift angle of primary side switch legs. When the system power reaches 50% or more of the rated power, the synchronous rectifier switches of the secondary side are performed.

Mode 6 ($t_5 \sim t_6$): Power control of CLLC resonant converter. The PFC-stage maintains the operation of *Mode 5*, and the CLLC converter performs power control with a constant slope by controlling the phase-shift angle and switching frequency of primary side switch legs. The SR switches also have the same switching frequency.

Mode 7 ($t_6 \sim t_7$): The reverse operation of (*Mode 5* to *Mode 6*) is performed.

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TABLE I
COMPARISON OF OPTIMAL SELECTION OF DECOUPLING CAPACITANCE \mathcal{C}_{S}

Case 1	Case 2	Proposed [28]
v _{Cs} waveform:	v _{Cs} waveform:	v _{Cs} waveform:
Convertional design – No consider the step-up ratio μ_{\pm} (see)	Maximum step-up ratio : 4 times F/a 569V 165 165 165 165 165 165 165 165	Proposed design - Minimum capacitance of <i>Cs</i>
$C_s = 220 \ \mu F$	$C_s = 448 \ \mu \mathrm{F}$	$C_s = 320 \ \mu F$
Current: 44.0 A _{rms}	Current: 39.5 A _{rms}	Current: 28.7 A _{rms}

III. ACTIVE POWER DECOUPLING DESIGN CONSIDERATION

In this section, a design guideline of the proposed single- and three-phase compatible ac-dc converter is presented. The following converter specifications are considered in the design: battery voltage $V_{\text{bat}} = 360-845$ V, dc link voltage $V_{\text{dc}} = 650-850$ V, grid input voltage $V_g = 360-440(3\emptyset)/70-285(1\emptyset)$ Vac, output power $P_o = 22(3\emptyset)/17.6(1\emptyset)$ kW, and switching frequency $f_{s,\text{pfc}}$ and $f_{s,\text{apd}} = 60$ kHz.

A. Active Power Decoupling Capacitor Design

First of all, it is assumed that the power contribution of the inductor in the buck-type active power decoupling circuit is neglected for the sake of the design. The C_s is designed at minimum $V_{dc} = 650$ V, and the P_o is at maximum of 22 kW. Equation (1) shows the relationship between capacitance, power P_o , coupling capacitor voltage V_{Cs} , voltage swing ΔV_{Cs} . We need to select the value of C_s and the control target V_{Cs} to ensure that the converter has sufficient gain to charge and discharge the capacitors. A smaller capacitance C_s results in a higher ΔV_{Cs} , where the minimum of V_{Cs} can reach 0, causing the converter to be unable to operate, as shown in case 1 in Table I. A higher capacitance for C_s will increase the size of the converter. Therefore, there is a tradeoff between available boost gain and capacitor size. On the other hand, the average voltage of C_s is controlled so that the current rating of C_s is smallest. As shown in Table I and [28], it is compared that the current rating and decoupling capacitance according to the average voltage of the decoupling capacitor and the step-up ratio at the minimum dc link voltage (650 V).

Finally, C_s is selected at 320 µF, and the target V_{Cs} is controlled at 650/1.41 V to reduce the current rating of the capacitance

$$C_s = \frac{V_{\rm dc} \cdot I_{\rm dc} \cdot P_o}{\omega \cdot V_{Cs} \cdot \Delta V_{Cs}}.$$
(1)

This allows the use of film capacitors because of the large voltage amplitude of the decoupling capacitor and the much smaller capacitance compared to traditional passive capacitive dc link buffering.



Fig. 6. Strategy for a wide battery voltage range. (a) Battery charging mode. (b) Battery discharging mode.

B. Active Power Decoupling Inductor Design

As shown in Table I, if the proposed method is applied, the current rating flowing through the decoupling circuit is 28.7 $A_{\rm rms}$. The approximate peak value of the rated current is 28.7 × sqrt(2) = 40.6 $A_{\rm pk}$. Therefore, the decoupling inductor value is designed by selecting 40% of the ripple at the peak current (at $D_{\rm apd} = 0.707$). The value of inductor L_s is calculated to be 140 μ H referring to (2)

$$L_s = \frac{V_{Cs} \cdot (1 - D_{apd})}{f_{s,pfc} \cdot \Delta I_{Cs}}.$$
 (2)

Using the designed inductor L_s , the decoupling circuit maintains the CCM operation, which can reduce the conduction loss and turnoff loss of the active switches compared to the DCM operation.

IV. CLLC DESIGN FOR WIDE VOLTAGE RANGE OPERATION

In this section, a design guideline of the proposed single- and three-phase compatible ac-dc converter is presented. The following converter specifications are considered in the design: battery voltage $V_{\text{bat}} = 360-845$ V, dc link voltage $V_{\text{dc}} = 650-850$ V, grid input voltage $V_g = 360-440(3\emptyset)/70-285(1\emptyset)$ Vac, output power $P_o = 22(3\emptyset)/17.6(1\emptyset)$ kW, and switching frequency $f_s = 150-250$ kHz.

A. Turn Ratio and Switching Frequency Range Design

1) Determine Turn Ratio n: To avoid any setbacks in the design, the below and above area of the CLLC resonant converter's gain curve should be properly distributed to facilitate subsequent design under both charging and discharging mode. Therefore, as shown in Fig. 6, the turn ratio n of the transformer with the narrowest voltage gain range is selected as n = 1.1. This allows a small volume of the magnetic material to be designed using a relatively high designed minimum switching frequency.

2) Determine Switching Frequency Range f_s : The specifications shown in Table II indicate the cross-section area of the customized core and the required B_{max} for designing the transformer. Also, the maximum input voltage (v_{dc}) is applied to the primary side of the transformer at the minimum switching

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TABLE II				
FACTOR OF DETERMINATION FOR MINIMUM SWITCHING FREQUENCY				

Item	Values
Turn ratio (<i>n</i> :1)	1.1:1
Cross section area (A_c)	800 mm ²
Maximum flux density (B_{max})	150 mT
The number of primary side turns (N_p)	12
Magnetizing inductor (L_m)	80.6 µH
Ratio of magnetizing inductor L_m to resonant inductor L_r (L_n)	4-8
Resonant frequency (f_r)	200 kHz



Fig. 7. Equivalent circuit of CLLC resonant converter. (a) Overall circuit of CLLC. (b) Battery charging mode. (c) Battery discharging mode.

frequency, so the switching frequency is selected using the (3)

$$f_{s,\min} \ge \frac{V_{\text{pri}} \cdot D}{2 \cdot B_{\max} \cdot A_c \cdot N_p} = 148 \text{ kHz.}$$
(3)

The maximum switching frequency is designed using the loss value of the gate driver external resistor, and the loss formula is as follows:

$$P_{R,\text{loss}} = (V_{CC} - V_{EE}) \cdot Q_g \cdot f_{s,\text{max}} < 1 \text{ Watt}$$
(4)

where $V_{CC} - V_{EE} = 18$ V, $Q_g = 220$ nC, On/Off resistor size and Watt: R3225, 0.5 W. Therefore, the switching frequency range of the CLLC resonant converter is selected from 150 kHz to 250 kHz using the above (3), (4) and referring the [29].

B. CLLC Voltage Gain Curves Design for Wide Voltage Range

The proposed resonant converter is composed of a circuit as shown in Fig. 7(a). To easy to derive the resonant tank design, both battery charging mode and discharging mode must be analyzed with first harmonic analysis (FHA) using first harmonic approximation and Appendix. Each mode can be expressed equivalently as in Fig. 7(b) and 7(c). Formulating the impedance of the equivalent circuit to obtain the voltage gain of the charging mode and the discharging mode, it can be expressed as



Fig. 8. Countermeasure for insufficient voltage gain. (a) Battery charging/discharging profiles. (b) Voltage gain curves with power derating.



Fig. 9. Comparison of voltage gain curves using Matlab and Psim. (a) w/o power derating. (b) with power derating.

follows, respectively

$$\frac{R'_{\text{vec}}}{n \cdot (Z'_s + R'_L) \cdot ((Z'_s + R'_L) / / Z_{Lm})} = \frac{R'_L \cdot ((Z'_s + R'_L) / / Z_{Lm})}{n \cdot (Z'_s + R'_L) \cdot (((Z'_s + R'_L) / / Z_{Lm}) + Z_p)}$$
(5)

$$\frac{\nu_{\rm pri}}{\nu_{\rm sec}} = \frac{n \cdot R_L \cdot ((Z_p + R_L) / / Z_{Lm})}{(Z_p + R_L) \cdot (((Z_p + R_L) / / Z_{Lm}) + Z'_s)}.$$
 (6)

Fig. 8(a) shows the charging mode profile (in discharging mode, it is a fixed power of 11 kW over the entire voltage range of the battery voltage). Based on the battery voltage of 540 V, the constant current operation (41 A) is performed below the corresponding voltage, and constant power operation (22 kW) is maintained at 540 V or higher. At battery voltages above 770 V (below region of CLLC gain curve), the converter's step-up ratio may not be sufficient. However, considering the lifespan of the lithium-ion battery and the safety of the system, a solution that derate the power as the battery voltage approaches the full charge voltage range is derived through discussion with the customer. Therefore, it is possible to obtain sufficient voltage gain in the below region of the converter by using the voltage transfer ratio (5) and (6) as shown in Fig. 9(b). Fig. 9(a) shows the gain curves of the situation without power derating (CP operation) using two simulation tools (Psim, Matlab). As the load increases, the FHA (in Matlab) provides inaccurate data on the gain curve. Rather, it appears similar to the gain that can be obtained in an actual experiment since the gain curve using Psim is based on the square wave operation. Fig. 9(b) also shows the gain curves of the situation with power derating using two simulation tools. The gain curves of the two simulation tools overlap equally under low load condition.

C. CLLC Operation Strategy and SR Mode

The proposed converter satisfies both the voltage gains for step-up and step-down using the 150–250 kHz switching frequency variable range and phase-shift angle between the

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Fig. 10. Control strategy of CLLC resonant converter. (a) Voltage gain curves according to load conditions. (b) Frequency and phase-shift controls compatible method.



Fig. 11. Typical resonance waveforms and required duty of synchronous rectification. (a) Below region. (b) DCX region. (c) Above region.

primary side switch legs. Referring to Fig. 10(a), the graphs of voltage gain curve for each load are shown. The below region of the converter is able to satisfy the step-up ratio through the power derating, but the above region must operate at a fairly high switching frequency to achieve a step-down ratio. However, in the proposed paper, the maximum frequency is selected as 250 kHz in order to increase the degree of freedom for the converter's operation. It also responds to low battery voltage using by the phase difference of the primary side switch legs. The control strategy will be described in more detail in Section V, but the output variable of the PI controller called varA is commonly used for both frequency control and phase-shift control. In other words, one variable (varA) can be flexibly used for both controllers without using each output variable for each controller, so that a seamless operation can be implemented. Therefore, as shown in Fig. 10(b), when varA is less than 180, the power control of the converter is implemented through phaseshift control. Conversely, if the corresponding variable is 180 or higher, power is controlled through frequency control.

For 22 kW rated operation and switch thermal management, there is a limit to operation only by using the switch parasitic diode. Therefore, it is necessary to reduce the heat of the switch through the synchronous rectification mode under more that 50% of full load. The rectification circuit of the resonance current is often additionally used for the synchronous rectification method. But in the proposed paper, the synchronous rectification is applied using a lookup table for each area (below, DCX and above). The conceptual diagram of the gate signal is shown in Fig. 11. In the below/DCX region of the converter, there is no significant change in the phase of the secondary-side resonant current. Therefore, the PWM carrier is synchronized based on the primary gate signal and the duty is applied to about D = 0.3. On the other hand, the secondary side duty is applied in consideration of the appropriate phase difference because there is a phase shift of the secondary side resonance current in the above

TABLE III CLLC TRANSFORMER'S CONNECTION AND BALANCING ISSUE



region. In the discharge mode, only the switch position is changed and applied in the same way as above.

D. Transformer Wiring Diagram and Unbalanced Issue

The high frequency transformer wiring structure of the dc-dc converter can be divided into two cases as shown in Table III. The most common method is Case A, which is a series connection for both the primary and secondary connections. In this method, a volt-sec difference across the transformer is generated by the impedance difference between L_{m1} and L_{m2} , resulting in an unbalance of magnetic flux density. It is difficult to manage the thermal imbalance of the transformer core and the stack-safety since the impedance of each manufactured core is significantly different during long-term operation of the system. In Case B, the secondary side of the transformer is connected in parallel. In this method, even if the magnetizing inductance of each core is different, the same volt-sec is applied to both ends of the secondary side of the transformer to form the identical magnetic flux density. Therefore, the connection method of Case B is selected in consideration of the current unbalance and the aspect of core volt-sec.

V. CONTROL AND SEQUENCE STRATEGY

A. Control Strategy of PFC+CLLC

1) Three-Phase System (3Ø): Fig. 12 shows the control strategy for the grid three- and single-phase systems. In a three-phase system, the voltage and current of each grid phase are sensed and converted from *abc* to *dq* transformation. The phase angle of grid θ_g is derived as the grid voltage *dq* value v_{dq} is passed through the phase-locked loop (PLL). The grid current *dq* value *i_{dq}* is used for the current controller. The dual-loop controller is applied in the PFC controller, and the outer/inner-loop controllers are composed of the dc link voltage/grid current controllers, respectively. Therefore, the dc link voltage is variably controlled to 600–850 V using the outer-loop voltage controller. The output value of the outer-loop controller is a reference value of the current controller, which is required for grid current control in the inner-loop current controller. The gate signal of the PFC switch legs is generated by comparing the current controller output value with the PWM carrier



Fig. 12. Control scheme of the proposed two-stage system.

through dq to *abc* conversion. At this time, the important point is to deactivate the low-frequency switches S_{7-10} and active power decoupling switches S_{11-12} .

The CLLC resonant converter strategy is shown in the grey box in Fig. 12, and the method is equally applied to the grid three- and single-phase system. In battery charging mode, the primary side switches S_{13-16} of the converter are used for control, and the secondary side switches S_{17-20} set the switching frequency to be the same as the primary side. The primary side switches use a 0.5 fixed duty and performs frequency control or phase-shift control according to the output value *varA* of the current controller. The current controller reference value i_{bat}^* is provided by the sequence strategy shown in Fig. 13. Figure shows the algorithm scheme of



Fig. 13. Sequence strategy of the proposed two-stage on-board charger.

the CLLC converter responsible for power control in the OBC system. The processes of summation/averaging battery voltage and current are occurred at the beginning of the flow chart. The control variable *varA* is the output value of the CLLC PI controller (refer to Fig. 12), and is ultimately converted into a frequency or phase-shift value. Using a lookup table, *deltaI* is adjusted to power variation tolerance of the system during P_{bat} becomes equal to P_{ref} .

2) Single-Phase System (1Ø): In a single-phase system, grid voltage and current are sensed and converted to $\alpha\beta$ to dq. The phase angle of grid is derived as the grid voltage dq value v_{dq} is passed through the PLL. The dual-loop controller is applied in the interleaved totem-pole PFC controller, and the outer/innerloop controllers are composed of the dc link voltage/grid current controllers, respectively. Therefore, the dc link voltage is variably controlled to 600-850 V using the outer-loop voltage controller. The output value of outer-loop controller divided by 3 is used as the current reference for each current PI regulator to control each high frequency leg. An important point is that the PWM carrier for each leg has a phase difference of 120 degrees due to the characteristics of the three-phase interleaved totempole circuit. The low-frequency switches S_{7-10} perform lowfrequency switching according to the grid positive and negative voltage. The decoupling controller extracts the 2nd (120 Hz), 4th (240 Hz), and 6th (360 Hz) components of the dc link voltage and uses it as the input variable of PR controller. The output value of the corresponding controller is injected into the output value of decoupling average controller. The CLLC explanation is omitted since it is the same as the three-phase system.

B. Sequence Strategy

The sequence strategy required for system power control is shown in Fig. 13. For the safety of the vehicle internal system,

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Fig. 14. Proposed two-stage system prototype. (a) Top view of prototype. (b) Side view of 3-D outline.

the on-board charger pursues relatively slow operation rather than fast response speed during battery charging or discharging. Therefore, the average value of the sensed current and voltage is used for control rather than instantaneous control. Comparing the power reference $P_{\rm ref}$ and $P_{\rm bat}$ multiplied by the battery average voltage and current determines the direction of the Fig. 13 flowchart. The battery current reference $I_{\rm ref}$ increases or decreases with each flow chart direction. To prevent the output power of the system from exceeding the power reference significantly, the output value *varA* of the CLLC current controller [refer to Fig. 10(b)] fluctuates through the increase or decrease of $I_{\rm ref}$. In addition, the frequency control and phase-shift control are seamlessly controlled using the *varA*.

VI. EXPERIMENTAL RESULTS

To validate the performance of the proposed single- and three-phase grid input compatible battery charging system, a 22 kW prototype with hardware packaging [with 3-D outline in Fig. 14(b)] is built as shown in Fig. 14. The system specification used in the experiment is presented in Table IV. Component ratings and selected devices of the proposed two-stage system are listed in Table V. The control algorithm is implemented in a floating-point DSP platform TMS320F28384S. And the digital power meter YOKOGAWA WT3000 is used to measure the efficiency. The proposed converter is tested to verify the operating principle and control scheme, and the several representative experimental waveforms are provided.

TABLE IV
PROTOTYPE SPECIFICATIONS OF THE PROPOSED TWO-STAGE OBC

Item	Values	
Rated power (P_o)	G2V: 3ph- 22 kW/1ph- 17.6 kW V2G: 3ph- 11 kW/1ph- 11 kW	
Grid voltage (V_g)	3ph: 360–440 V, 1ph: 70–285 V	
Battery voltage (V_B)	G2V: 360–845 V V2G: 500–845 V	
Maximum grid current	3ph- 32 A/1ph- 80 A	
Maximum battery current	41 A	
Switching frequency (f_s)	PFC: 60 kHz, CLLC: 150-250 kHz	
Power density	2.18 kW/L (313 \times 304 \times 106 mm)	

TABLE V PARAMETER'S RATING AND COMPONENTS

Parameters	Rating		Components	
Input filter inductor L_g	Inductance V_{peak} I_{rms}	280 μH 840 V 33 A	H225138A, 2stack (DONGBU CORE)	
Switch S_{1-20}	$V_{ m peak} \ I_{ m rms}$	845 V 30.2 A	NVH4L020N120SC1 (ONSEMI)	
DC-link capacitor C_{dc}	Capacitance V^{peak} I_{rms}	72 μF 840 V 32 A	C4AQNBU4400M18J 3EA, (KEMET) C4AQNBW5150M3HJ 4EA, (KEMET)	
APD capacitor C_s	Capacitance V_{peak} I_{rms}	320 μF 715 V 32 A	C4AQNBW5400M3NJ 8EA, (KEMET)	
APD inductor L_s	Inductance V_{peak} I_{rms}	134 μH 715 V 31 A	H225138A, 2stack (DONGBU CORE)	
Transformer T_r	L ^m inductance Turn ratio	77.3 μH 12:11	Customized core PL-17YH (SAMWHA)	
Resonant inductor L_{r1} and L_{r2}	L_{r1} inductance L_{r2} inductance $I_{rms,Lr1}$ $I_{rms,Lr2}$	12.35 μF 10.2 μF 43 A 45 A	Customized core PL-17YH (SAMWHA)	
Resonant capacitor C_{r1} and C_{r2}	C_{r1} capacitance C_{r2} capacitance $I_{rms,Cr1}$	56.6 nF 68.8 nF 43 A 45 A	GCM32E5C2J333J 8S14P, (Murata) GCM32E5C2J333J	
Output capacitor C_o	Capacitance V _{peak} I _{rms}	30 μF 845 V 22 A	C4AQNBW5150M3HJ 2EA, (KEMET)	

A. Operation Sequence

The experimental waveforms for the initial operation at the single-phase grid input are shown in Fig. 15. The dc link capacitor becomes the initial charge with applying the single-phase grid voltage. The dc link voltage is variably controlled with a slope. After several seconds, the average voltage + PR control is implemented for charging and discharging the active decoupling capacitor. All of the above-mentioned sequences are no-load conditions, and then the power control is performed by monitoring the battery current at the output stage of the CLLC resonant converter.



Fig. 15. Initial sequence operation waveforms of ac-dc converter at single-phase grid input.



Fig. 16. Experimental waveforms showing power factor correction and ZVS turn on of switches under full-load condition at three- and single-phase grid input, respectively: (a.1) PFC of a-phase, (b.1), (c.1) primary side and secondary side of CLLC converter at three-phase grid input, respectively. (a.2) PFC of single-phase, (b.2), (c.2) primary side and secondary side of CLLC converter at single-phase grid input, respectively.

B. Experimental Results

Fig. 16 shows the experimental waveforms under full load conditions according to single- and three-phase grid input. In addition, the operation waveforms of the CLLC resonant converter are representative waveforms of the DCX region among several regions (below, DCX, above). Fig. 16(a.1) shows the grid a-phase voltage and current waveforms at three-phase grid input. The power factor is over 0.99 and the maximum current of each phase is $32 A_{\rm rms}$ under the 22 kW full-load condition. As described above, Fig. 16(b.1) shows the gate-source voltage and drain-source voltage of switch S_{13} and resonant inductor L_{r1} current under battery charging mode. At this time, the switch S_{13} achieves ZVS turn-on and hard-switched turn-off with the magnetizing inductor L_m current. Fig. 16(c.1) shows the gate-source voltage and drain-source voltage of switch S_{17} and resonant inductor L_{r2} current. The synchronous rectification (SR) is inevitably applied due to the junction temperature of secondary side



Fig. 17. Experimental waveforms of active power decoupling (APD) at full-load conditions. (a) Battery charging mode. (b) Battery discharging mode.

switches. Therefore, a value of SR duty is about 0.33 in this experiment. The resonant inductor L_{r2} current is determined by the summation of the primary-side resonant current and the magnetizing inductor current.

Fig. 16(a.2) shows the grid single-phase voltage and current waveforms. The power factor is over 0.98 and the maximum grid current is $80 A_{\rm rms}$ under the 17.6 kW (220 V and 80 A) full-load condition. The CLLC converter waveforms are same as in Fig. 16(b.1) and 16(c.1) at single-phase grid input situation.

As shown in Fig. 17, it is the waveforms in the cases of battery charging (17.6 kW) and discharging (11 kW) at a singlephase grid input. The decoupling capacitor C_s voltage has a large ripple width since it extracts the low-frequency components of the dc link voltage. In addition, the battery charging mode is selected as the worst case for passive device design. Therefore, the maximum voltage of the decoupling capacitor is close to the dc link voltage at the full-load condition. Fig. 17(b) shows the waveforms of the battery discharging mode at 11 kW, and the difference between the maximum value of decoupling capacitor voltage and the dc link voltage is relatively large compared to Fig. 17(a).

Fig. 18 shows temperature data of single-phase operation according to battery voltage fluctuation (540 V \rightarrow 360 V) in charging mode under full-load condition. The proposed system reduces the output power as constant current mode (40 A) while battery voltage is lower than 540 V, which is the CLLC above region. Temperature data represents the following components: PFC high-side switches (201–203), PFC inductor (204), Trans core (205), PFC low-side switch (206), CLLC 2nd side switch (207), CLLC 1st side switch (208), Trans coil (209), and Case (210).

Fig. 19 shows the efficiency curves of the proposed two-stage system under three- and single-phase grid input. The measured peak efficiencies of the proposed two-stage system with active power decoupling according to three- and single-phase grid input are 95.77% and 94.98%, respectively. It should be noted





Fig. 18. Measured temperature data of single-phase operation in charging mode under full-load condition.



Fig. 19. Measured efficiency graphs of the proposed single- and threephase compatible two-stage system.

that the overall efficiencies are greater than 95% at DCX region of CLLC resonant converter.

VII. CONCLUSION

In this article, a single- and three-phase compatible battery charger with active power decoupling (APD) is proposed for reducing the hardware footprint area and extending the long-life time of passive components. The proposed two-stage system has compact structure due to absence of electrolytic capacitors. Furthermore, it is easy to change the mode operation by handling the relay structure at grid input terminal. The ac-dc converter variably controls the dc link voltage to widen the proportion of the DCX region (good efficiency performance) in a wide battery voltage range. In addition, a seamless single PI controller for CLLC resonant converter is presented to cover a wide battery voltage range and overall load conditions by combining the frequency control and phase-shift control. The power density of prototype for the single-phase 17.6 kW and threephase 22 kW is 2.18 kW/L and volume length is $313 \times 304 \times$ 106 mm (xyz). Experimental results from a 22 kW prototype are provided to validate the proposed system concept. The twostage prototype achieved peak efficiencies of 95.77% and 94.98% under full-load condition at three- and single-phase grid input, respectively.

APPENDIX

where
$$R'_L = n^2 \cdot R_L = n^2 \cdot \left(\frac{8}{\pi^2}\right) \cdot R_o$$
, $v'_{sec} = n \cdot v_{sec}$
 $Z_p = Z_{Lr1} + Z_{Cr1}$, $Z'_s = n^2 \cdot (Z_{Lr2} + Z_{Cr2})$.

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