A GaN-Based Improved Zeta Converter With Integrated Planar Transformer for 800-V Electric Vehicles

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***Abstract*—This article proposes a high-step-down dc-dc converter for electric vehicles with an 800 V battery system. The proposed converter significantly reduces the current rating requirement for the dc blocking capacitor on the secondary side by reconstructing the secondary side circuit. The maximum duty cycle of the proposed converter is larger than the phase-shift full-bridge converter, which allows the use of larger leakage inductance. This turns out to be a crucial advantage to achieve the wide range zero voltage switching (ZVS) in high switching frequencies over 500 kHz. In addition, with a three-level structure, the voltage rating of the primary side switch is determined as half the input voltage and the energy to achieve ZVS turn-on is reduced, so it is suitable for high-frequency operation using a gallium nitride (GaN) device. The two transformers are integrated with partial flux cancelation, resulting in 10.3% of power loss and 27.7% of footprint reduction. Finally, a 700 kHz GaN-based 1.2 kW prototype achieved a power density of 10.2 kW/L and a peak efficiency of 93.4%.**

***Index Terms*—800-V battery, electric vehicles (EVs), GaN, high power density, low voltage dc-dc converter, planar magnetics.**

I. Introduction

ELECTRIC vehicles (EVs) are attracting strong attention as a viable solution to reduce greenhouse gas emissions. In EV applications, the driving range and charging time are major obstacles to the wide deployment of EVs. The energy density of Li-ion battery cell has almost tripled since 2010, thus the driving range of EVs has been increasing. EVs, which were released in 2021, were expected to have driving ranges from 400 to 1000 km [1], [2]. The increased EV battery capacity needs longer charging times with the conventional 400 V EV fast charger system. A sufficient charge of 5% to 80% battery SOC for roughly 400 km is desirable within the usual break time of 15–20 min [3]. Even with a 200 kW fast charger, the charging time for the 400 V EVs cannot be done within 20 min because the charging current is limited to 500 A [4]. Consequently, the 800 V EV battery system was introduced to shorten the charging time because it allows twice the charging power with the same charging current. IONIQ 5 launched in 2021 adopted an 800 V battery system with a 72.6 kWh Li-ion battery and is charged within 18 min using a 350 kW fast charger [5]. Also, the 800 V system has the advantages, among others, of reduction in wiring size and I^2R loss and improved performance of the propulsion motor [6], [7].

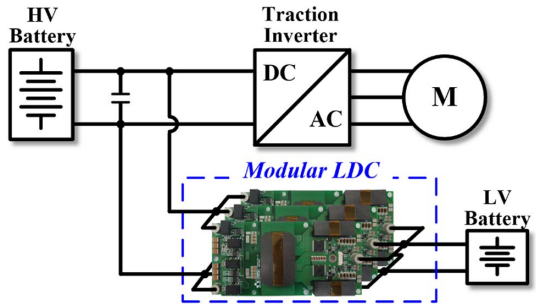

Fig. 1. Configuration of multimodule LDC for 800 V EV power train.

In EV application, the low voltage dc-dc converter (LDC) is one of the key components that charge 12 V battery from high voltage battery. The 12 V auxiliary loads are headlamps, wiper blade motors, audio systems, interior lights, etc. Currently, LDCs with power levels of around 2 kW are dominant in EVs on the road [8], [9]. However, recent developments demand power levels of around 3 kW due to increased electrical accessories such as electric panels and navigation systems [4]. Further, as the number of auxiliary loads tend to increase due to the improvement of ADAS technology such as LIDAR, RADAR, cameras, and ultrasonic sensors, the required power level for the LDC is expected to further increase to 5 kW. This increase requires LDC to have a higher power density to fit into a limited vehicle space [10], [11].

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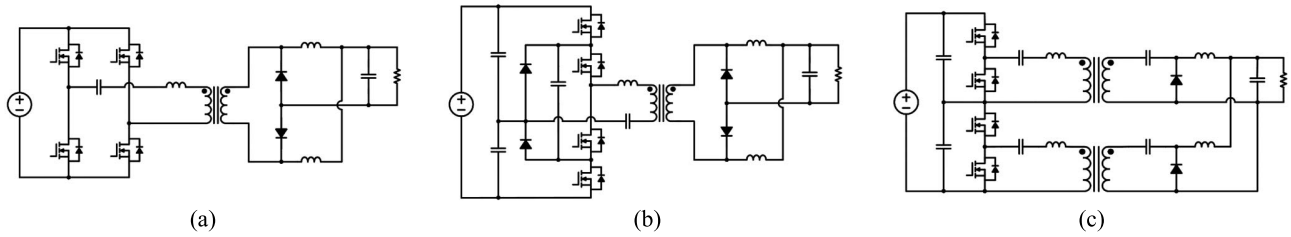


Fig. 2. Candidate topologies for 800 V LDC. (a) PSFB converter. (b) HBTL converter [26]. (c) ISHB zeta converter [27].

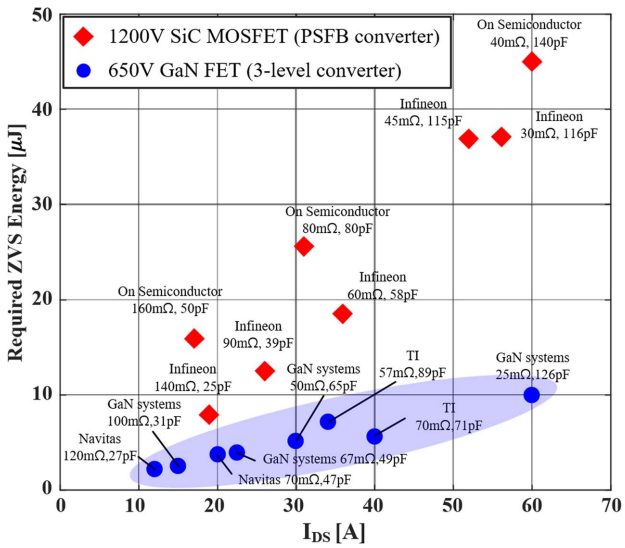


Fig. 3. Required ZVS energy of 1200 V SiC MOSFET and 650 V GaN FET for 800 V systems.

In response to this concern, the U.S. Department of Energy (DoE) sets a challenging power density target for LDC to achieve 4.5 kW/L in 2025 [12]. Achieving such challenging power density needs the use of high-frequency operated wide band gap (WBG) devices that have superior characteristics such as low loss, high speed, high-temperature operating capabilities, high power density, and easy cooling techniques. High-frequency gallium nitride (GaN)-based LDCs that achieved high power density have been introduced in [13], [14], [15], [16], and [17].

Meanwhile, due to lower operating costs, EVs are suitable for mobility-as-a-service (MaaS) applications such as connected taxi and car share that have high operating time of 50 000 to 80 000 miles a year, thereby requiring high durability and life expectancy. In this regard, the reliability target for 2025 was increased from 150 000 to 300 000 miles for these vehicles [12]. Fig. 1 shows the structure of the multimodule LDC for EV power train. A modular approach was introduced in [18] for improving the reliability and power density of LDC. The modular method allows the use of higher switching frequency, which leads to not only high-power density but also improved regulating capability due to reduced passive components value [19].

II. Issues on LDC for 800 V Battery System

Figure 2 shows candidate topologies for 800 V LDC. The phase-shift full-bridge (PSFB) converter has been widely used as a basic topology for 400 V LDC due to its zero voltage switching (ZVS) characteristic and simple structure [15], [16], [17]. However, for 800 V systems, the PSFB converter should adopt 1200 V SiC metal oxide semiconductor field effect transistors (MOSFETs) while the three-level type converter can adopt 650 V GaN devices [20]. Fig. 3 represents the required ZVS energies of various types of 1200 V SiC MOSFETs when applied to the PSFB converter and 650 V GaN FETs when applied to the three-level type converter. The ZVS energy was calculated by using the voltage across the switch and the output capacitance provided by the manufacturer, such as Infineon, On-semiconductor, Navitas, TI, and GaN systems [21], [22], [23], [24], [25]. It is seen from Fig. 3 that the required ZVS energies for 1200 V SiC MOSFETs are much larger than those for 650 V GaN FETs, which is mainly because of the higher voltage of 800 V across the 1200 V SiC MOSFETs. This forces the PSFB converter to use a larger leakage inductance for achieving ZVS at the light load compared to three-level type converters that use 650 V GaN devices. However, large leakage inductances limit the maximum output power due to duty cycle losses, and thereby it limits the switching frequency, which is a critical barrier for achieving high power densities. In practice, the use of 1200 V SiC MOSFET for the PSFB converter with a high switching frequency over 500 kHz is not feasible due to the design issue associated with ZVS energy and duty cycle losses. In the meantime, the half-bridge three-level (HBTL) converter, shown in Fig. 2(b), can be considered.

TABLE I
Comparison of Topologies for 800 V LDC

Topology	HBTL [26]	ISHB Zeta [27]
Turn ratio*	6:1	
Voltage rating of switch	390 V	
Number of diodes	4	2
Number of capacitors	2	4
Number of transformers	1	2
Duty range	$0 < D < 0.5$	$0 < D < 1$
ZVS energy	10.84 μJ	18.71 μJ

*Designed in order that voltage rating of the secondary diode is less than 70 V. (P_O = 1.2 kW, V_{in} = 460 ∼ 780 V, V_O = 11.5 ∼ 15.1 V).

As a candidate topology for 800 V LDC [26]. The HBTL converter with 650 V GaN devices has lower requirements of ZVS energy compared to the PSFB converter with 1200 V SiC. However, it may not achieve ZVS turn-on under light load conditions due to duty cycle losses when the switching frequency is over 500 kHz. In addition, it requires additional two clamp diodes with fast reverse recovery. To the authors' knowledge,

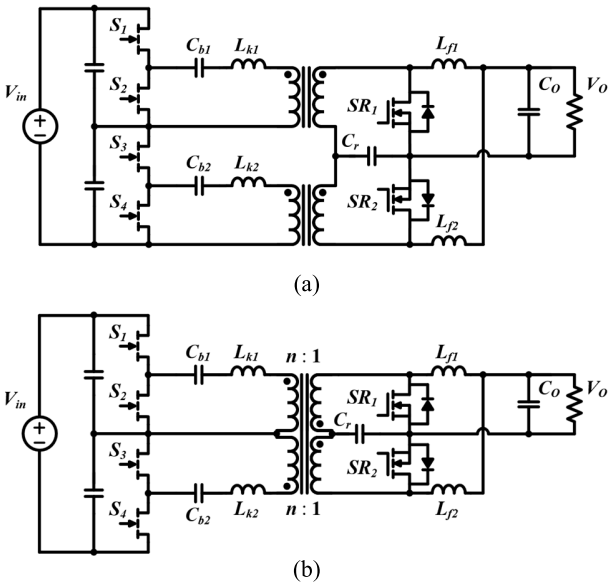


Fig. 4. Circuit diagram of the proposed ISHB zeta converter. (a) With interleaving effect. (b) With integrated transformer.

there are few studies about circuit topologies for LDCs for 800 V battery systems. The input series half-bridge (ISHB) zeta converter [27] shown in Fig. 2(c) has half the switch voltage rating, which makes it possible to use 650 V GaN FETs, thereby being able to operate at a high switching frequency. Further, the maximum duty cycle of the ISHB zeta converter is larger than the one of the PSFB converter, which allows the use of larger leakage inductance. This turns out to be a crucial advantage to achieve the wide range ZVS in a high switching frequency over 500 kHz. In addition, it has zero current switching (ZCS) turn-off in the diodes and zero magnetizing current offset. As shown in Table I, the HBTL and ISHB zeta converters were compared with the same specifications. Both topologies can use 650 V GaN FETS, because of the three-level structure. The ISHB zeta converter requires more capacitors and transformers except for diodes. However, because the ISHB zeta converter has a wide duty range, it can be designed to have a larger ZVS energy than the HBTL converter.

In this article, a 650 V GaN-based LDC that is suitable for 800 V battery system is proposed. The proposed converter is a modified ISHB zeta converter [28], [29]. Fig. 4 shows circuit diagrams of the proposed converter. As shown in Fig. 4(a), two half-bridges in the primary side are interleaved with 180° phase-shift. Fig. 4(b) shows the final structure of proposed converter with integrated transformer. The interleaving effect reduces the current rating of the secondary blocking capacitor and output capacitor by a factor of three. Additionally, the utilization of an integrated transformer with partial flux cancelation reduces the size of the transformer. The proposed converter has a wide ZVS range in the switches, ZCS turn-off of rectifier diodes, and zero magnetizing current offset. Magnetic integration of two transformers using the planar core with printed circuit board (PCB) winding results in loss and footprint reduction. A 3-D finite element analysis (FEA) simulation is carried out to verify the validity of the proposed integrated planar transformer. The experimental results from a 1.2 kW, 700 kHz GaN-based prototype of the proposed converter are provided.

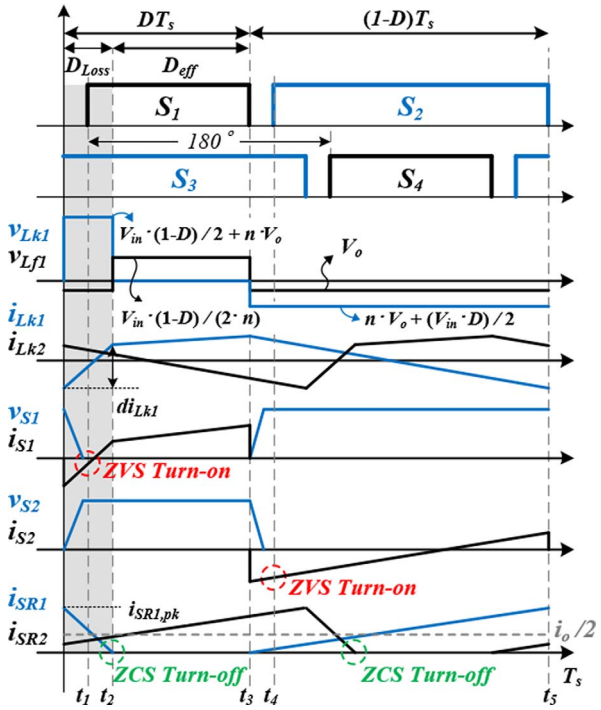


Fig. 5. Key waveforms of the proposed converter.

III. Operating Principles of the Proposed Converter

Figures 5 and 6 show key waveforms and operation states of the proposed converter. In order to simplify the analysis, several assumptions are made as follows.

1) All parasitic components except for those specified in Fig. 6 are neglected.
2) Magnetizing inductor and filter inductor are very large.
3) All blocking capacitors have a sufficiently large capacitance to be considered as maintaining a constant voltage.

A. Operating Principle

Mode 1 ($\sim t_1$): In this mode, S_1 and S_2 are turned off. The secondary switch SR_1 is conducting. Voltage V_{in} (1-D)/2 + $n{\cdot}V_o$ is applied to L_{k1} since v_{Cr} is the same as output voltage. Current i_{Lk1} is linearly reduced with positive slope. The stored energy in L_{k1} makes C_{oss1} discharge to 0 and C_{oss2} charged to V_{in}/2, respectively.

Mode 2 ($t_1 \sim t_2$): Achieving ZVS turn-on of S_1, current i_{Lk1} flows through the channel of S_1 with positive slope. In this mode, the duty cycle loss caused by leakage inductor reduces the power transfer period (Mode 3). This mode ends when current i_{SR1} reaches to 0 A.

Mode 3 ($t_2 \sim t_3$): From t_2, input power is delivered to output side. Secondary switch SR_1 is turned off and V_{SR1} is applied $V_{\text{in}}{\cdot}$(1-D)/2${\cdot}n{+}V_O$.

Mode 4 ($t_3 \sim t_4$): Mode 4 starts when S_1 is turned off. The secondary switch SR_1 starts conducting. Voltage $n{\cdot}V_o$ - $V_{\text{in}}{\cdot}D/2$ is applied to L_{k1}. Therefore, current i_{LK1} is linearly reduced with

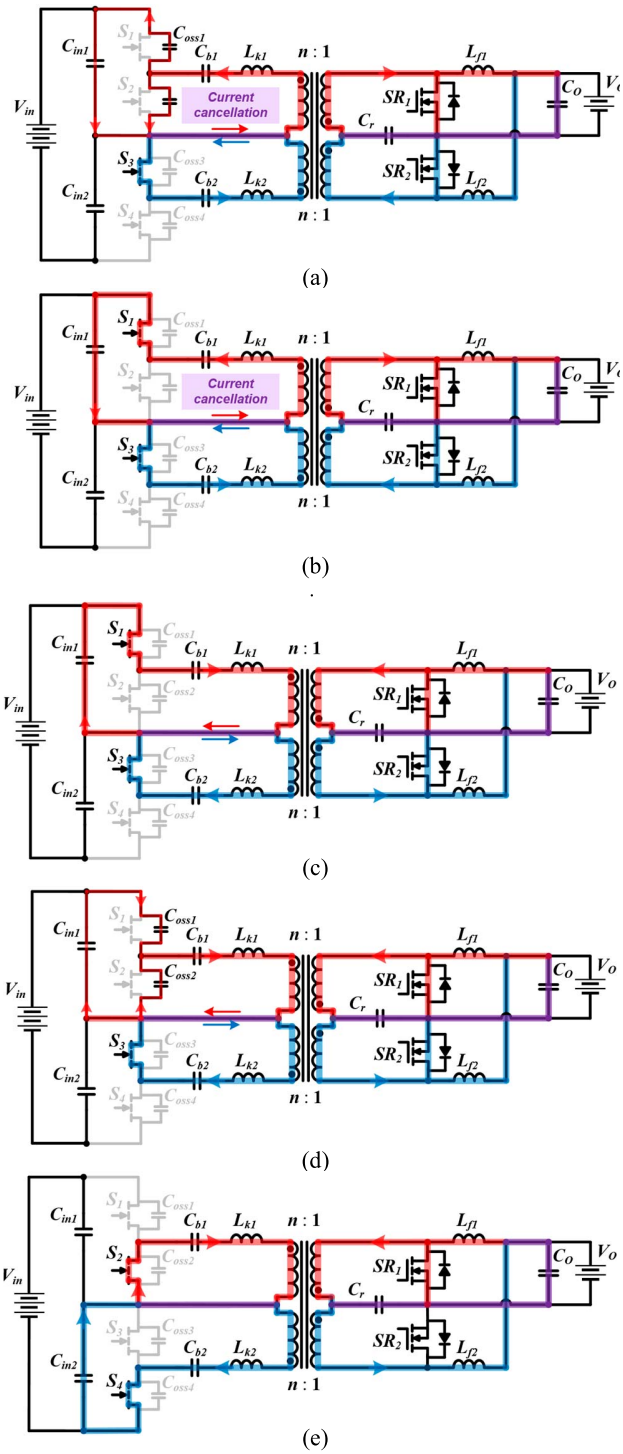


Fig. 6. Operation states of the proposed converter. (a) Mode 1 ($\sim t_1$). (b) Mode 2 ($t_1 \sim t_2$). (c) Mode 3 ($t_2 \sim t_3$). (d) Mode 4 ($t_3 \sim t_4$). (e) Mode 5 ($t_4 \sim t_5$).

negative slope. The stored energy in filter inductor L_{f1} makes C_{oss1} charged to $V_{in}/2$ and C_{oss2} discharged to 0, respectively. The stored energy in filter inductor is much larger than the leakage inductor energy for achieving ZVS turn-on. This mode ends when S_2 is turned on.

Mode 5 ($t_4 \sim t_5$): After C_{oss2} is completely discharged, ZVS turn-on of S_2 is achieved, and current i_{Lk1} keeps decreasing with negative slope. SR_1 operates as free-wheeling diode. This mode ends when S_2 is turned off. Current $i_{Lk1,\,(t5)}$ is used as energy for discharging C_{oss1}.

B. Voltage Transfer Ratio

In isolated PWM-based converters, as the switching frequency increases, the ratio of duty cycle losses to the switching period increases. Therefore, to find the actual voltage transfer ratio, duty cycle loss caused by the leakage inductance should be considered. Duty cycle loss D_{Loss} is defined as follows:

$$D_{\text{Loss}} = D - D_{\text{eff}}. \tag{1}$$

Effective duty D_{eff} means the period during which positive voltage is applied to the filter inductor. By applying volt-second balance principle on the leakage inductor L_{k1} the following equations are obtained:

$$\left(\frac{V_{\text{in}} \cdot (1-D)}{2} + n \cdot V_o\right) \cdot D_{\text{Loss}} = \left(n \cdot V_o - \frac{V_{\text{in}} \cdot D}{2}\right) \cdot (1-D). \tag{2}$$

During the 1-D period, each di_{Lk1} is expressed from inductor voltage equation as follows:

$$\text{di}_{L_{k1}} = \left(\frac{V_{\text{in}} \cdot (1-D)}{2} + n \cdot V_o\right) \cdot \frac{D_{\text{Loss}} \cdot T_s}{L_{k1}}. \tag{3}$$

Since the average current of the secondary switch is identical to the average load current in the steady state, the following equation is obtained:

$$\text{di}_{SR1} = i_{SR1,\text{pk}} = \frac{I_o \cdot T_s}{(1 - D_{\text{eff}})}. \tag{4}$$

During D_{Loss} period, due to the relationship as follows:

$$n \cdot \text{di}_{L_{k1}} = \text{di}_{SR1}. \tag{5}$$

The quadratic formula can be used to find the effective duty by substituting the values from (3) to (4) into (5).

$$D_{\text{eff}} = \frac{(D-1) + \sqrt{(D-1)^2 - 4 \cdot \left(D - \frac{I_o \cdot L_{k1}}{0.5 \cdot V_{\text{in}} \cdot (1-D) + n \cdot V_o}\right)}}{2}. \tag{6}$$

By applying volt-second balance principle on the filter inductor L_{f1}, the following equations are obtained:

$$\frac{V_o}{V_{\text{in}}} = \frac{(1-D)}{2 \cdot n \cdot (1 - D_{\text{eff}})} \cdot D_{\text{eff}}. \tag{7}$$

The voltage transfer ratio equation is completed by substituting the effective duty obtained from (6) into (7).

Figure 7 shows the voltage transfer ratio according to the leakage inductance. As shown in Fig. 7, assuming an ideal transformer, the voltage transfer ratio increases linearly. However, increasing the leakage inductance results in a higher duty cycle loss, leading to a reduction in the output voltage. In general, a large leakage inductance increases the energy to achieve ZVS turn-on in the primary switch. However, it decreases the maximum output voltage by increasing the duty cycle losses.

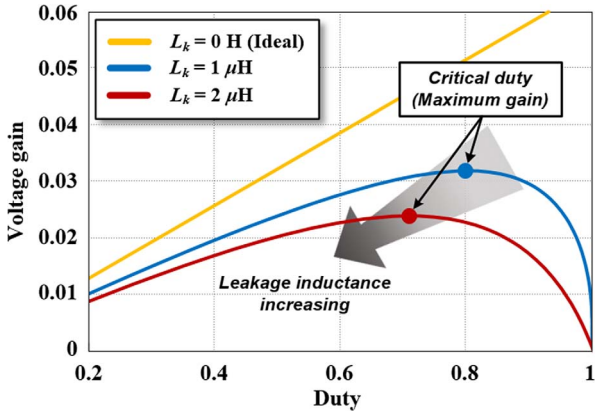


Fig. 7. Voltage transfer ratio according to leakage inductance.

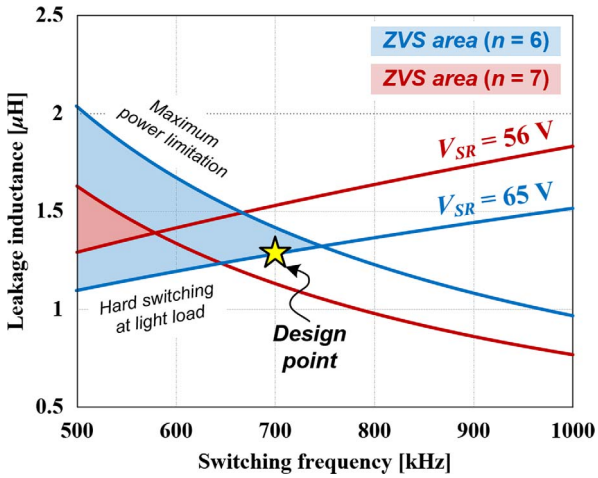


Fig. 8. Leakage inductance versus switching frequency to achieve voltage regulation and ZVS turn-on.

C. ZVS Condition

The ZVS turn-on in the main switches S_1 and S_4 is achieved by the stored energy in the leakage inductor. The stored energy in the leakage inductor is lower than the stored energy in the filter inductor. Therefore, in order to achieve ZVS turn-on in the main switch at light loads, the leakage inductor should be designed as follows:

$$\frac{1}{2}\cdot L_{k1}\cdot i^2_{Lk1,(t5)} \geq (C_{\text{oss}} + C_{\text{stary}})\cdot\left(\frac{V_{\text{in}}}{2}\right)^2 \tag{8}$$

where current $i_{Lk1,(t5)}$ is expressed using the inductor voltage equation as follows:

$$i_{Lk1,(t5)} = \frac{I_o}{2\cdot n} - \frac{V_{\text{in}}/2\cdot D - n\cdot V_o}{L_{k1}}\cdot(1-D). \tag{9}$$

Figure 8 shows the leakage inductance versus the switching frequency curve according to the turn ratio. The positive slope line is the boundary condition of the minimum leakage inductance to achieve ZVS turn-on at light loads. If the leakage inductance value is lower than this positive slope line, ZVS turn-on cannot be achieved at light loads. As the switching frequency increases, the turn-off time of the main switch decreases, resulting in a reduction

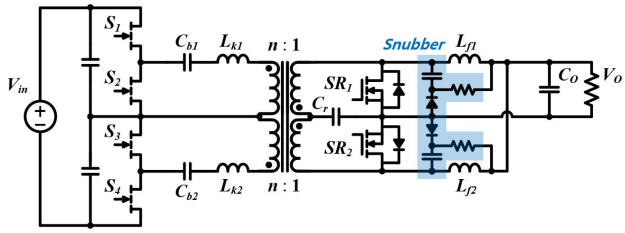


Fig. 9. Circuit diagram of proposed converter with RCD snubber.

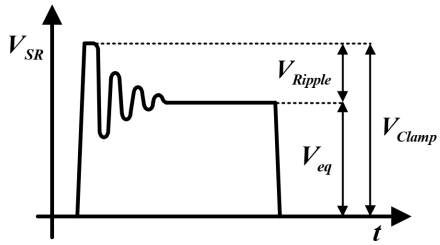


Fig. 10. Voltage of secondary switch with RCD snubber circuit.

in the value of $i_{Lk1,(t5)}$ in (9). This signifies a decrease in the amount of energy required to achieve ZVS turn-on. The amount of energy for ZVS turn-on can be confirmed in (8). Hence, an increased switching frequency demands a larger value for leakage inductance. The negative slope line is the boundary of the maximum power limitation. If the leakage inductance value is larger than this negative slope line, the maximum power limitation occurs because of the increased duty cycle losses. Hence, as the switching frequency increases, the effective duty cycle decreases, leading to a reduction in the available maximum value for leakage inductance. This relationship can be observed in the graph derived from (7). Therefore, in order to operate at maximum power and achieve ZVS turn-on at light loads, it is necessary to select a switching frequency and a leakage inductance in the region between the two lines. This area decreases as the turn ratio is increased. According to the Maxwell simulation results, the stray capacitor was calculated as 32.5 pF. The switching frequency and leakage inductance of the proposed converter were selected to be 700 kHz and 1.2 μH, respectively.

D. RCD Snubber Design

The voltage spike occurs at the moment when the secondary switch turn-off because of the leakage inductance and resonant behavior of the output charge (C_{oss}) of the secondary switch. This surge voltage is induced across the drain source of the secondary switch. It increases the voltage stress of the secondary switch. The high voltage rating of the secondary switch leads to a high parasitic resistance ($R_{\text{ds(on)}}$). Maintaining a low voltage rating for the secondary switch is important to satisfy the high efficiency of the converter. Thus, the snubber circuit composed of resistor, capacitor, and diode (RCD) is employed to prevent the secondary voltage from exceeding a desired level with acceptable loss [30]. The power circuit with snubber is described in Fig. 9 When the secondary switch is turned off, the voltage of drain-source graph is expressed as shown in Fig. 10. V_{eq} value is the total voltage including the blocking capacitors.

V_{eq} is defined by the following equation:

$$V_{eq} = \frac{V_{in}}{2 \cdot n} - \frac{V_{Cb1}}{n} - V_{Cr}. \tag{10}$$

Step 1: Selection of Maximum Switch voltage (V_{Clamp})

The V_{Clamp} was selected as 90 V in consideration of a 10% margin at the breakdown voltage of selected secondary switch.

Step 2: Design of Snubber Resistor (R_S)

The power of the leakage inductor is consumed by the resistance of the RCD snubber. Consequently, the resistance value of the RCD snubber is calculated using the following equation:

$$R_s < \frac{2 \cdot V_{ripple} \cdot V_{Clamp}}{L_{k1} \cdot {i_{Lk1}}^2 \cdot f_{sw}}. \tag{11}$$

Step 3: Design of Snubber Capacitor (C_S)

The snubber capacitance is calculated using the following equation:

$$C_s > \frac{V_{Clamp}}{V_{ripple} \cdot f_{sw} \cdot R_s}. \tag{12}$$

Step 4: Selection of Snubber Diode (D_S)

The snubber diode should have a larger current rating than the snubber current and a higher voltage rating than the secondary switch.

The voltage spike is influenced not only by the leakage inductance of the transformer but also PCB trace inductance, damping of parasitic resistance, and even the packaging of component. Consequently, it is important to measure the actual voltage with the installed state on PCB and adjust the snubber circuit accordingly.

IV. Proposed Customized Core Structure for Integrated Transformers

A. Proposed Core Structure

The ISHB zeta converter has four magnetic components including two inductors and two transformers, which increases the total volume of the system. In order to reduce the volume, the two transformers are integrated into a single core. Fig. 11 illustrates the proposed integration procedure along with the core structure. First, as shown in Fig. 11(a), two separate UI cores of the two transformers are excited by interleaving voltages. Hence, magnetic flux in each core has 180° phase-shift. Second, by simply combining the two cores into a single core, as shown in Fig. 11(b), the flux ripple in the center leg is reduced because of the interleaving between the two fluxes. In order to achieve high power density, the height limit of the transformer is set to 10.6 mm. This makes the perimeter of outer legs larger, meaning that the mean length turn (MLT) of winding is longer compared to squares with the same cross-sectional area. Moreover, the large overlap winding area between layers makes parasitic capacitance larger. To reduce winding loss and parasitic capacitance, the perimeter of the outer legs should be reduced. By configuring the side leg in a square shape, the MLT of the proposed core is smaller compared to the simple integrated core as shown in Fig. 11(c). As shown in Fig. 11(b), the blue pattern part is unutilized. In order to utilize that part, the length of the

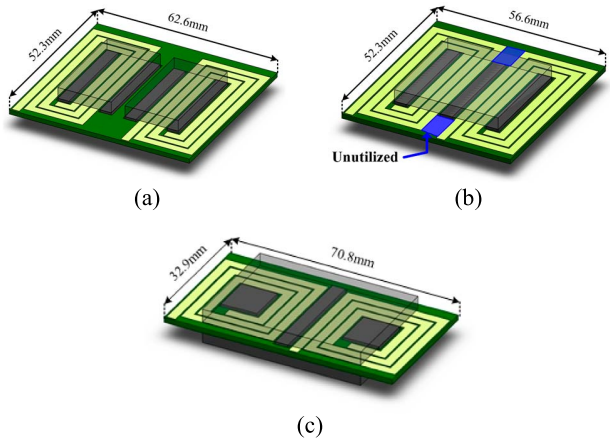


Fig. 11. Transformer primary windings and core structure: the cross-section area of each leg in the structure is the same. (a) Separated cores. (b) Simple integrated core. (c) Proposed integrated core.

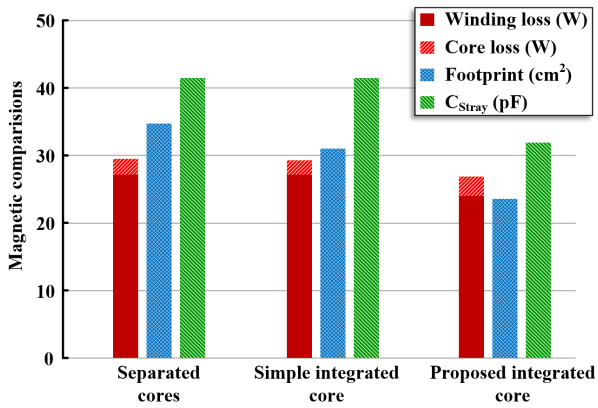


Fig. 12. Comparison of the magnetic structures.

center leg is extended by the sum of the side leg width and the pattern length [31]. Fig. 12 shows comparison of three types of cores. The results of comparison are obtained from the Maxwell simulation. Due to the simple integration of the two cores into one and removing half part of the center leg, the simple integrated transformer has a 9.6% footprint reduction and 11.8% core loss reduction compared to that with separated cores. By changing the core structure with the proposed integrated core, although the core loss increases the total power loss, total footprint, and the stray capacitance are reduced by 10.3%, 28.9%, and 23.2%, respectively, compared to that with separated cores.

B. Design of the Proposed Core

The ratio of the center flux ripple to the outer flux ripple depends on the duty cycle of the interleaved voltage excitation and is expressed as follows [32], [33]. The ratio of the center flux ripple to the outer flux ripple can be expressed as follows:

$$\frac{\Delta\phi_c}{\Delta\phi_o} = \begin{cases} \dfrac{1-2D}{1-D}, & D < 0.5 \\ \dfrac{2D-1}{1-D}, & D > 0.5 \end{cases}. \tag{13}$$

The flux ripple in the center leg is always smaller than 70% of that in the outer leg during the operating duty cycle range,

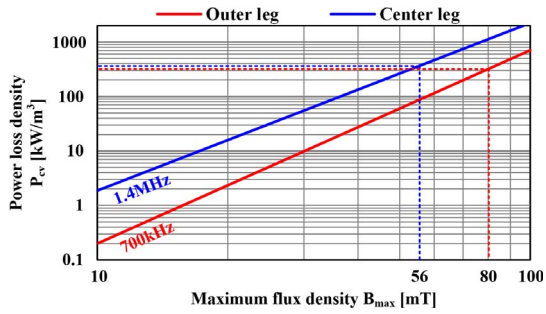


Fig. 13. Power loss density versus flux density in different frequencies.

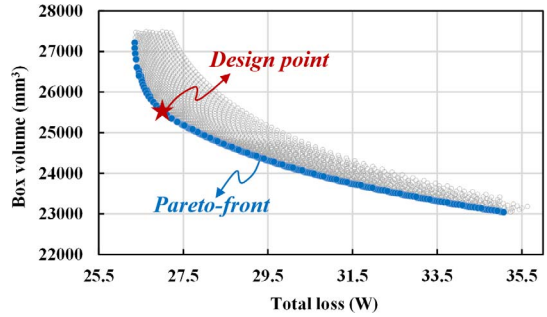
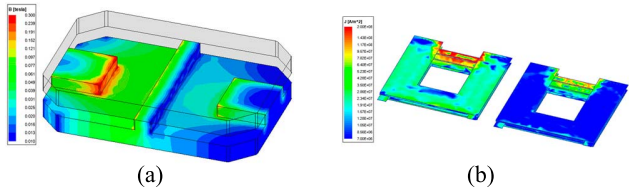


Fig. 14. Optimization result of the proposed integrated transformer.

TABLE II
COMPONENTS RATINGS AND DESIGN PARAMETERS

Components		Values
Switch	Primary (S_1~S_4)	GS66508B (GaN systems) 650 V/50 mOhm
	Secondary (SR_1~SR_2)	IAUT300N10S5N015 (Infineon) 100 V/1.5 mOhm
Transformer	Core	Customized ML91 (Hitachi)
	L_m/L_k	80 μH/1 μH
	N_p:N_s	6:1
	B_{max}	75 mT
	J	45 A/mm^2
	Dimension	49 × 33.9 × 10.6 mm
Filter Inductor	Core	Customized ML91 (Hitachi)
	L_f	700 nH
	B_{peak}	280 mT
	Dimension	13.5 × 39.9 × 10.6 mm
Capacitor	C_{b1}, C_{b2}	CGJ6M3X7T2D334K200AA 200 V/0.33 μF/8EA
	C_r	CGA5L1X7R1H106K160AC 50 V/10 μF/6EA
	C_o	CGA5L1X7R1H106K160AC 50 V/10 μF/4EA
Snubber	R_s	MMB02070C1502FB200/10EA
	C_s	GCM31B7U2E103JX01
	D_s	S320

which means that the maximum flux density in the center leg is smaller than 35% of that in the outer leg due to the doubled cross-section area of 2Ac. Moreover, the cross-section area of



(a) (b)

Fig. 15. FEA simulation results of transformer. (a) Flux distribution. (b) Current distribution.

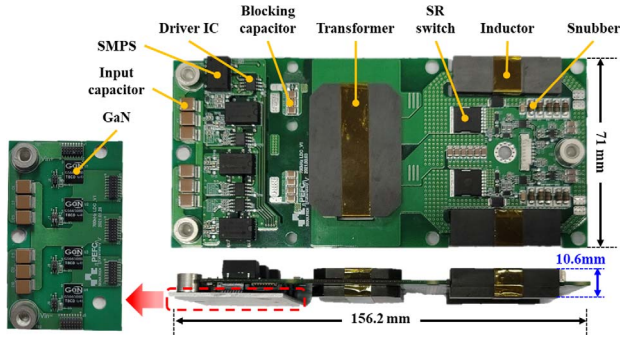
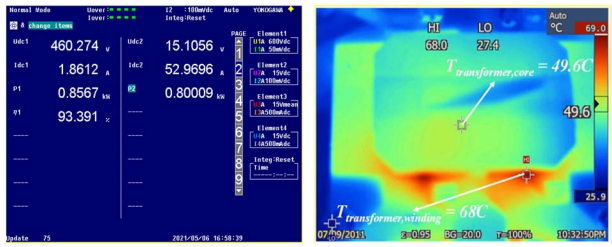


Fig. 16. 1.2 kW prototype of the proposed ISOP converter (10.2 kW/L).

TABLE III
PROTOTYPE SPECIFICATIONS

Item	Values
Power	1.2 kW
Input voltage	460 ~ 780 V
Output voltage	11.5 ~ 15.1 V
Switching frequency	700 kHz
Power density	10.2 kW/L



(a) (b)

Fig. 17. Experimental result (a) Peak efficiency. (b) Transformer heat.

the center leg, Ac, is reduced by half. Although the maximum flux density in the center leg is lower than that in the outer leg, the power loss density in the center and outer leg should be considered because the frequency in the center leg is twice compared to that in the outer leg. In order to compare the power loss in the legs, the power loss density versus flux density in different frequencies is shown in Fig. 13. The graph is made based on the datasheet of material ML91s from Hitachi Metals. Due to the high operating frequency, the flux density should be smaller than 100 mT. For example, the maximum flux density in the outer leg is 80 mT. Then the maximum flux density in the center leg is 56 mT, which is 70% of that in the outer leg. As shown in

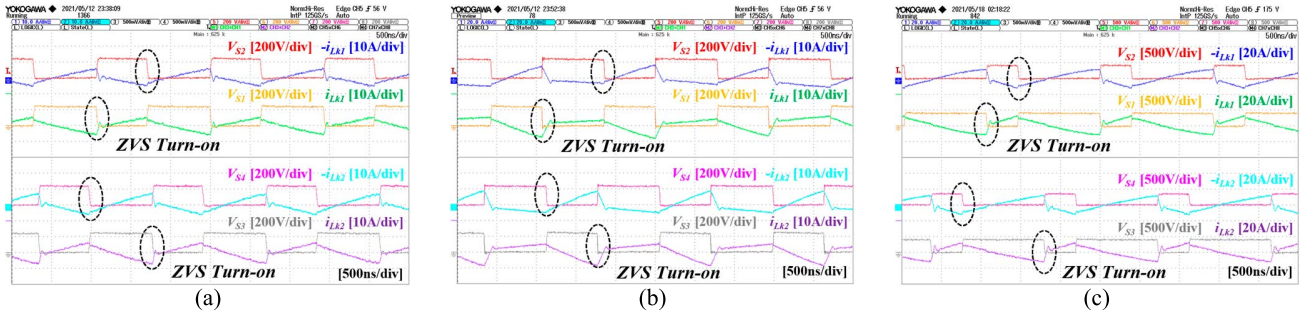


Fig. 18. Experimental waveforms with primary side. (a) $P_o = 400$ W, $V_{in} = 460$ V, $V_o = 15.1$ V. (b) $P_o = 1200$ W, $V_{in} = 460$ V, $V_o = 15.1$ V. (c) $P_o = 1200$ W, $V_{in} = 780$ V, $Vo = 15.1$ V.

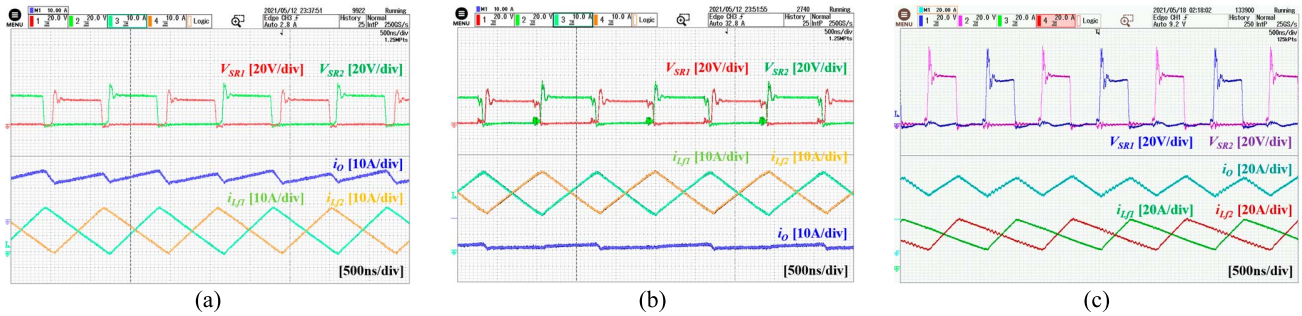


Fig. 19. Experimental waveforms with secondary side. (a) $P_o = 400$ W, $V_{in} = 460$ V, $V_o = 15.1$ V. (b) $P_o = 1200$ W, $V_{in} = 460$ V, $V_o = 15.1$ V. (c) $P_o = 1200$ W, $V_{in} = 780$ V, $Vo = 15.1$ V.

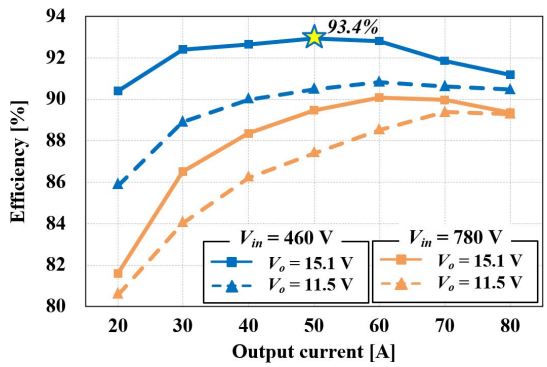


Fig. 20. Measured efficiencies of the proposed converter (measured by Yokogawa WT3000).

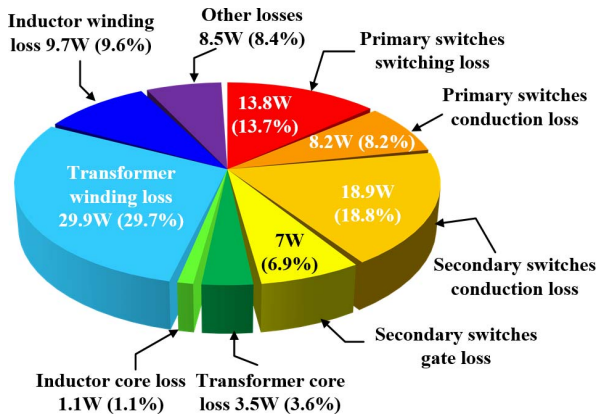


Fig. 21. Loss breakdown of proposed converter when $V_{in} = 460$ V, $V_o = 15.1$ V, and $P_o = 1.2$ kW.

Fig. 13, the power loss density in the legs is similar. Then finally, in the transformer core, all the legs can have the same cross-section area.The volume-loss design points shown in Fig. 14 include Pareto-front. A design point is selected among Pareto-front using figure-of-merit mentioned in [12], [13].

$$\text{FOM} = \text{Total Volume} \times \text{Power Loss}.$$

C. FEA Simulation Result

The integrated transformer specifications are shown in Table II where the values of peak flux density and current density (J) are from the design point selected in the previous section. In order to verify the integrated core structure, a 3-D FEA simulation in Maxwell was performed. From the results in Fig. 15(a), it is easy to see that the simulated peak flux density in the center and outer leg respectively are around 75 and 52.5 mT which coincides with the designed values. As shown in Fig. 15(b), the simulated current density is higher than 45 A/mm^2 because of the proximity effect.

V. Experimental Results

In order to verify the proposed converter, a 1.2 kW, 700 kHz GaN-based prototype was built. Fig. 16 shows a photograph of the prototype of the proposed converter. The proposed LDC uses two PCBs. The lower PCB, includes the GaN devices with a metal PCB. The upper PCB consists of the gate driver circuit, magnetic components, and rectification stage. The height of the magnetic components is determined by the bottom surface of the

TABLE IV
COMPARISION OF LDC FOR 800-V BATTERY SYSTEM

	[10]	[34]	[35]	[36]	Proposed LDC
Topology	ISOP PSFB	3Phase System + Interleaved Buck	TS-DEACF + AHB	CFDAB	ISHB zeta
Mode changing	O	X	O	O	X
Power rating	5 kW	5 kW	600 W	3.25 kW	1.2 kW
Input voltage	225 ∼ 800 V	800 V	350 ∼ 800 V	180 ∼ 900 V	460 ∼ 780 V
Output voltage	16 ∼ 32 V	12 V	13.9 V	6 ∼ 16 V	11.5 ∼ 15.1 V
Peak efficiency	95.7%	93.7%	92.7%	97%	93.4%
Full load efficiency	94%	> 90%	90.4%	94%	91.6%
Switching frequency	100 kHz	50 kHz	70 kHz	80 kHz	700 kHz
Power density	5 kW/L	.	.	.	10.2 kW/L

metal PCB and the height of the SMPS, which measures 10.6 mm. Table II presents the selected components and magnetics design parameters. As primary side switches, 650 V GaN FETs were used. Synchronous rectification was implemented at secondary side to reduce the conduction loss. The magnetics was designed with low-profile of 10.6 mm to achieve high power density. The experimental specifications of the prototype are shown in Table III. Fig. 17(a) shows the peak efficiency measured using the Yokogawa WT3000. Fig. 17(b) shows the temperature measurement of the transformer. The highest heat generation occurs at the PCB winding, reaching a temperature of 68°. The core's temperature measures at 49.6°. Figs. 18 and 19 show experimental waveforms. The proposed converter has the smallest energy for ZVS turn-on when the filter inductor operates at the boundary conduction mode (BCM) mode [16]. When the filter inductor operates at the DCM mode, ZVS energy can be increased by increasing the dead time. Therefore, achieving ZVS turn-on at the BCM mode means that the ZVS turn-on can be achieved over the entire load range. Fig. 18 shows the voltage of primary switches and leakage inductor current, while Fig. 19 shows the voltage of secondary switches, filter inductor current, and output current. From Fig. 19(a), we can observe that the minimum value of the filter inductor current is zero. It can be recognized that the converter is operating in BCM mode with $P_o = 400$ W, $V_{\text{in}} = 460$ V, and $V_o = 15.1$ V specifications. Fig. 18(a) indicates that despite BCM mode operation, ZVS turn-on can be achieved. Fig. 19(b) represents full-load specifications. Due to interleaving effect, output current ripple is very small. At this point, the operational duty cycle is 0.58. Fig. 19(b) shows waveforms at full load condition with input voltage of 780 V. The maximum voltage of the secondary switches was measured up to 93 V. Fig. 20 shows the measured efficiencies. At $V_{\text{in}} = 460$ V and $V_o = 15.1$ V, the peak efficiency and full load efficiency are 93.4% and 91.6%, respectively. Fig. 21 shows the loss breakdown of the proposed converter. About 47.6% of losses occur in the semiconductors. In case of magnetics, core loss is very small. However, due to high current density of 45 A/mm^2, the total winding losses of the PCB winding is 39.3% of the total losses.

Table IV shows a comparison of LDCs that can be applied to the 800 V battery system. The LDCs in Table IV require relay or operational mode changes to operate the wide voltage range. The proposed LDC can operate in a relatively wide input–output voltage range without mode changes. Currently, there is limited research on LDCs for 800 V batteries operating at high switching frequencies of several hundred kHz, resulting in insufficient information regarding power density.

VI. CONCLUSION

In this article, a GaN-based LDC for 800 V EV is proposed. The voltage rating of the primary switch is half of the input voltage due to the input series output parallel (ISOP) structure, which made it possible to use GaN devices. The proposed converter has wide operating duty range, which allowed the use of large leakage inductance, resulting in wide ZVS range. This in turn allowed an increase in switching frequency, which is crucial in achieving high power density. The proposed integrated transformer demonstrated reductions of 10.3% in power losses and 27.7% in footprint while achieving a low profile of 10.6 mm height. Finally, the 1.2 kW, 700 kHz prototype achieved a power density of 10.2 kW/L and a peak efficiency of 93.4% at 800 W.

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