Single-Stage Totem-Pole AC–DC Converter Based on Boost Half-Bridge Structure for Battery Chargers

Tat-Thang Le, *Member, IEEE*, Jaeyeon Lee, *Member, IEEE*, and Sewan Choi, *Fellow, IEEE*

***Abstract*—In this article, a new single-stage bridgeless totem-pole ac–dc converter is proposed. The proposed converter is composed of two single-stage boost half-bridge ac–dc converters with the interleaved operation. Besides, while preserving the advantages of the *L*-type half-bridge-based single-stage totem-pole ac–dc converter, the proposed converter has the ability of phase-shedding operation, which helps to increase the total efficiency of the converter due to reduced switching and core losses by half under medium and light loads. A hybrid harmonic injection in phase shift and duty cycle according to battery voltage is proposed, which not only improves total harmonic distortion to smaller than 4% under the whole load range but also extends the zero-voltage switching range of the converter under a wide voltage range. The proposed control method can be utilized in the general dual-active-bridge-based single-stage converter. Experimental results from a 1.5-kW prototype are provided to validate the proposed concepts.**

***Index Terms*—Boost half-bridge, dual-active-bridge (DAB), interleaved, phase shedding, single-stage ac–dc converter, totem-tole bridgeless power factor correction (PFC), zero-voltage switching (ZVS).**

I. Introduction

RECENTLY, single-stage ac–dc power converters have become an attractive research topic for many applications including uninterrupted power supplies, energy storage systems, and electric-vehicle (EV) on-board battery chargers' applications. Since the power factor correction (PFC) circuit and isolated dc–dc converter are integrated, the single-stage topologies possibly achieve higher efficiency due to reduced power conversion stages, lower cost due to reduced components, and smaller size due to reduced bulky dc-link capacitor [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33].

Single-phase matrix-based ac–dc converters [1], [2], [3], [4], [5] that use back-to-back switches are alternative topologies for bidirectional operation. This topology has a large conduction loss since all the switches conduct the grid current during both negative and positive half-cycle. The back-to-back switches also increase the control complexity and system cost.

The single-stage converters with the bridgeless structure have been proposed in [6], [7], [8], [9], [10], [11], [12], [13], and [14], given that the conduction loss is significantly reduced since the current is conducted through the minimum number of switches compared to the conventional PFC circuits. Also, it has a smaller component count of semiconductor devices, smaller weight and volume compared to the unfolding bridge structure [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], and simple control compared to the matrix-based structures.

The challenges associated with the aforementioned single-stage converters include zero-voltage switching (ZVS) conditions and light load efficiency when it operates under a wide voltage range. The bridgeless totem-pole based on *L*-type half-bridge structure in [6] and [10] is shown to have the prominent features of not only electrolytic capacitorless but also ripple-free grid current, no zero-crossing current spike, and simple control with fixed frequency operation, unlike the other bridgeless structure. Detailed analyses on ZVS and total harmonic distortion (THD) performances under a wide voltage range have not been discussed, which were shown to be important, especially in battery charger applications. The efficiency at light load is an important consideration because the converter spends two-thirds of the total charging time for the absorption and float stages with the partial load [34]. This becomes more serious in dual-active-bridge (DAB)-based single-stage converters due to the voltage mismatch between primary and secondary when the voltage ratio varies. Even though some techniques try to increase the light load efficiency by extending the ZVS range to reduce turn-ON switching losses, the turn-OFF and conduction losses are still dominant when operating under a wide voltage range. A phase-shedding operation is a common technique to optimize the converter efficiency at a light load [35], [36]. There is no further discussion on the phase-shedding operation of the aforementioned single-stage ac/dc converters.

This article proposes a single-stage bridgeless totem-pole ac–dc converter based on boost half-bridge topology with a wide ZVS range and the phase-shedding function. The comparison between *L*-type half-bridge [6] and boost half-bridge structures is comprehensively studied to show the advantage of the proposed converter. The features of the proposed converter are as follows:

Manuscript received 23 March 2023; revised 28 June 2023 and 29 August 2023; accepted 7 October 2023. Date of publication 13 October 2023; date of current version 6 December 2023. This work was supported in part by the Korea Institute of Energy Technology Evaluation and Planning grant funded by the Korea Government under Grant 20212020800020, and in part by the Seoul National University of Science and Technology. Recommended for publication by Associate Editor K. Basu. *(Corresponding author: Sewan Choi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3323946.

Digital Object Identifier 10.1109/TPEL.2023.3323946

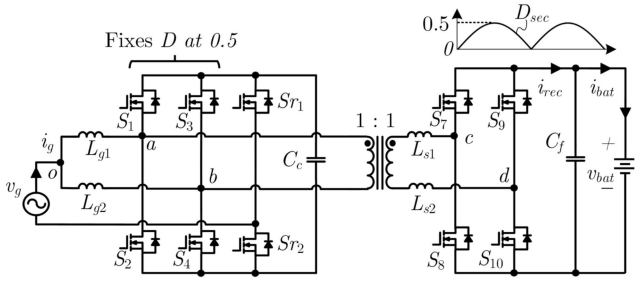

Fig. 1. Conventional single-stage interleaved totem-pole AC–DC converter based on *L*-type half-bridge structure [6].

TABLE I
COMPARISON OF *L*-TYPE HALF-BRIDGE AND BOOST HALF-BRIDGE CONVERTERS

	Conventional converter [6]	Proposed converter
Control method	$d_p = 0.5$ $d_s(t) = 0.5\lvert\sin(\theta)\rvert$ (θ is phase angle $= \omega t$) Power is controlled by phase shift, φ	
Equivalent electrical model	L_{s1}, v_{ab}, v_{cd}, L_{s2}	L_{s1}, v_{an}, v_{co}
ZVS turn on	Narrow ZVS range	Wider ZVS range
Phase-shedding capability	No	Yes

1) Bridgeless totem-pole structure.
2) Electrolytic capacitorless with high-frequency (HF) isolation.
3) Low THD with a simple proposed harmonic injection method, which also guarantees the ZVS range of the converter under a wide voltage range.
4) Phase-shedding operation not only for reducing the switching loss but also for improving the ZVS range under light load, resulting in higher efficiency at light load.

A prototype of a 1.5-kW converter was built and tested to validate the proposed concept. From the proposed converter with comprehensive analysis, it is possible to generalize to the interleaved multiphase structure for the single-stage ac–dc converter based on a boost half-bridge converter.

II. TOPOLOGY DERIVATION

It starts from the conventional single-phase single-stage totem-pole ac–dc converter based on *L*-type half-bridge topology which was first introduced in [6] as shown in Fig. 1. This converter operates as a DAB-based converter where the power is controlled by the phase shift between two sides of the transformer. Two interleaved legs on the grid side are switched with a fixed 50% duty for achieving the free ripple of the grid current, while the switches on the battery side are switched for the PFC by controlling the duty function in Table I. The switches S_{r1} and S_{r2} are operated as the grid voltage rectifiers. The advantage of these topologies includes high power density by use of electrolytic capacitorless with HF isolation and no zero-crossing current spike at ac main zero-crossing [6]. The main drawback of this topology is low efficiency at light load due to high circulating power and losing ZVS.

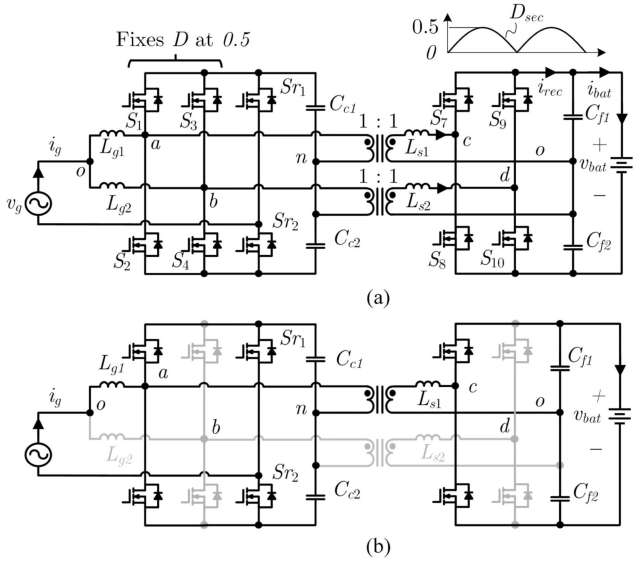

Fig. 2. Proposed bidirectional single-stage interleaved totem-pole AC–DC based on boost half-bridge structure. (a) Proposed converter. (b) Phase-shedding operation.

Fig. 2 shows the proposed bidirectional single-stage totem-pole ac–dc, which is composed of two interleaved boost half-bridge converters. While maintaining the same advantage as the converter [6] by keeping the same control method, the proposed converter has a wider ZVS range compared to [6]. A detailed comparison of the ZVS condition of the two converters is shown in the next section. Moreover, the converter can turn OFF one phase for improving efficiency under light load.

It is noted that our approach's method is to design a modular three-phase structure, composed of three single-phase single-stage modules as shown in [8]. The output currents of the three modules exist as the second harmonic of the grid current, with a 120° phase shift. Since the operations of the three modules are the same, the sum of the three output currents results in a pure dc battery current. This article focuses on only one module to show the advantage of proposed topology.

A. Half-Bridge Structure With Split Capacitor

Fig. 3 shows the two basic operation modes of the half-bridge structure with the split capacitor. When S_{L7} turns ON, as shown in Fig. 3(a), $v_{co} = v_{Lm} = v_{Cf1}$. When S_{L8} turns ON, as shown in Fig. 3(b), $v_{co} = v_{Lm} = -v_{Cf2}$. It is noted that the capacitance of C_{f1} and C_{f2} has a small value, so there are no grid frequency components stored in these capacitors. The average voltage across magnetizing inductor of the transformer equals zero in one switching cycle as shown in Fig. 3(c). This balancing condition can be expressed as

$$\int_0^{T_s} v_{Lm}(t) = 0 \rightarrow d_s T_s v_{cf1} = (1 - d_s) T_s v_{cf2}. \quad (1)$$

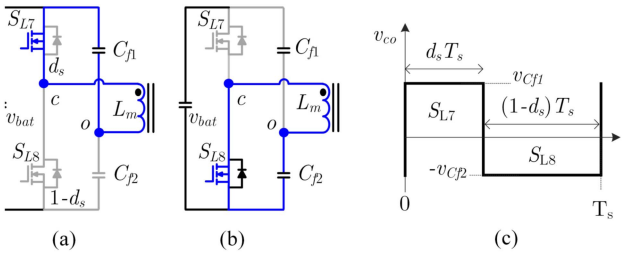

Fig. 3. Operation modes of the half-bridge structure with split capacitor. (a) S_{L7} turns ON. (b) S_{L8} turns ON. (c) Transformer voltage waveform.

On the other hand

$$v_{cf1} + v_{cf2} = v_{\text{bat}}. \tag{2}$$

From (1) and (2), v_{cf1} and v_{cf2} are obtained as follows:

$$\begin{cases} v_{Cf1} = (1 - d_{\text{s}})v_{\text{bat}} \\ v_{Cf2} = d_{\text{s}}v_{\text{bat}}. \end{cases} \tag{3}$$

Equation (3) shows the v_{Cf1} and v_{cf2} vary depending on the duty cycle d_s. These results will be utilized for analyzing the equivalent voltage sources of the proposed topology in the following section.

B. Analytical Model

The analysis model of each converter is built in the time domain by using the MATLAB program, which provides the closed-form solutions to show the performances of converters including transformer current waveforms, power flows, soft-switching characteristic, and THD of the grid current. Figs. 4 and 5 show the key waveforms of two converters under the same parameters and switching method in a positive half-cycle of grid voltage. The negative half-cycle has a similar operation. The phase angle θ is from 0 to π. Fig. 6 shows the flow chart of the analytical model that includes three loops. The internal loop is to calculate all parameters during one switching cycle. The middle loop is to calculate the instantaneous power and grid current depending on θ. And the outer loop is for analysis in different phase shifts. This analytical model can be utilized for general single-stage ac–dc DAB-based converters. The steps of the analytical model are described as follows:

Step 1: To determine the electrical model of converters. Generally, the DAB-based converters can be represented by two voltage sources across the series inductance. The simplified electrical models of the two converters are shown in Table I. The electrical model of the conventional converter contains v_{ab}, v_{cd}, and L_{s1} and L_{s2}, meanwhile, that of the proposed converter includes v_{ao}, v_{cn}, and L_{s1}.

Step 2: To determine the equivalent voltage sources. Calculations of the equivalent voltage sources v_{ab}, v_{cd}, v_{an}, and v_{co} are determined from the switching function of primary duty $d_p(\theta)$ and secondary duty $d_s(\theta)$ as shown in Figs. 4(a), (b) and 5(a), (b). The main difference between the two converters is shown in this step. The peak values of v_{ab}, v_{an}, v_{cd}, and v_{co} are v_{Cc}, v_{Cc1}, v_{cf}, and v_{cf1}, respectively, which are determined as the function of the duty cycle, as shown in (4) and (5). It is noted

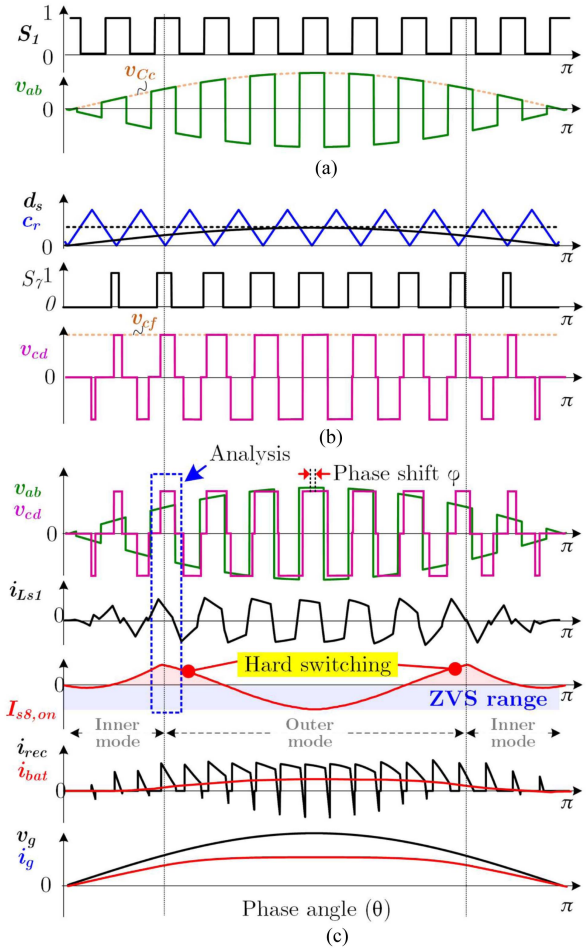

Fig. 4. Key waveform of the AC–DC converter based on *L*-type half-bridge structure [6] (described in reduced switching frequency form).

that the v_{cf1} varies depending on d_s as shown in Fig. 5(b), which helps to achieve the ZVS condition of battery-side switches $S_{7,8}$ especially when the battery voltage becomes low as shown in Fig. 5(c). The analysis of the ZVS condition is detailed in the next section

$$\begin{cases} v_{Cf1}(\theta) = (1 - d_{\text{s}}(\theta))v_{\text{bat}} \\ v_{Cf2}(\theta) = d_{\text{s}}(\theta)v_{\text{bat}} \end{cases} \tag{4}$$

$$\begin{cases} v_{Cc1}(\theta) = (1 - d_p(\theta))v_{Cc}(\theta) = v_g(\theta) \\ v_{Cc2}(\theta) = d_p(\theta)v_{Cc}(\theta) = d_p/(1 - d_p(\theta))v_g(\theta). \end{cases} \tag{5}$$

The equivalent voltage sources in a switching period (0 to T_s) are described as follows:

$$v_{ab}(t) = \begin{cases} v_{Cc}(\theta) & if(0 < t \le d_pT_s) \\ -v_{Cc}(\theta) & if(d_pT_s < t < T_s) \end{cases} \tag{6}$$

$$v_{cd}(t) = \begin{cases} 0 & if(0 < t \le 0.25T_s - 0.5d_sT_s) \\ v_{\text{bat}} & if(0.25T_s - 0.5d_sT_s < t \le 0.25T_s + 0.5d_sT_s) \\ 0 & if(0.25T_s + 0.5d_sT_s < t \le 0.75T_s - 0.5d_sT_s) \\ -v_{\text{bat}} & if(0.75T_s - 0.5d_sT_s < t \le 0.75T_s + 0.5d_sT_s) \\ 0 & if(0.75T_s + 0.5d_sT_s < t \le T_s) \end{cases} \tag{7}$$

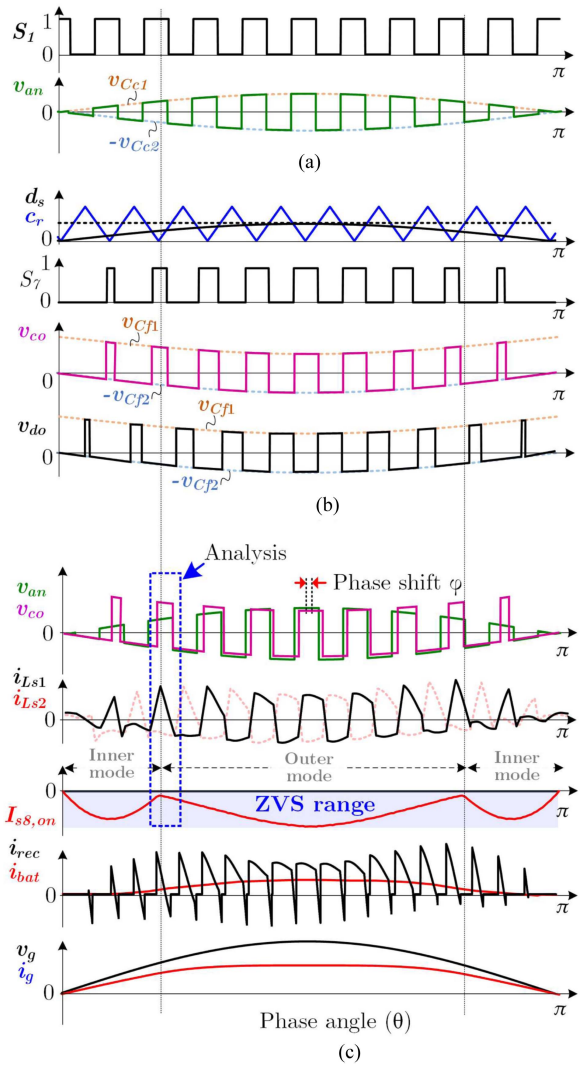

Fig. 5. Key waveform of the proposed AC–DC converter based on boost half-bridge structure (described in reduced switching frequency form).

$$v_{an}(t) = \begin{cases} v_{Cc1}(\theta) & if(0 < t \le d_p T_s) \\ -v_{Cc2}(\theta) & if(d_p T_s < t < T_s) \end{cases} \tag{8}$$

$$v_{co}(t) = \begin{cases} -v_{Cf2}(\theta) & if(0 < t \le 0.25T_s - 0.5d_s T_s) \\ v_{Cf1}(\theta) & if(0.25T_s - 0.5d_s T_s < t \le 0.25T_s + 0.5d_s T_s) \\ -v_{Cf2}(\theta) & if(0.25T_s + 0.5d_s T_s < t \le T_s). \end{cases} \tag{9}$$

We assume that $v_{ab}(t)$ and $v_{an}(t)$ have zero phase shift; then $v_{cd}(t)$ and $v_{co}(t)$ are shifted with the amount of $d_\varphi T_s$ for the power transfer, where $d_\varphi = \varphi/360$. Finally, v_{cd} and v_{co} are obtained as follows:

$$v_{cd}(t) = v_{cd}(t \to d_\varphi T_s) \tag{10}$$

$$v_{co}(t) = v_{co}(t \to d_\varphi T_s). \tag{11}$$

Equations (10) and (11) are conducted by using *circshift* function in MATLAB.

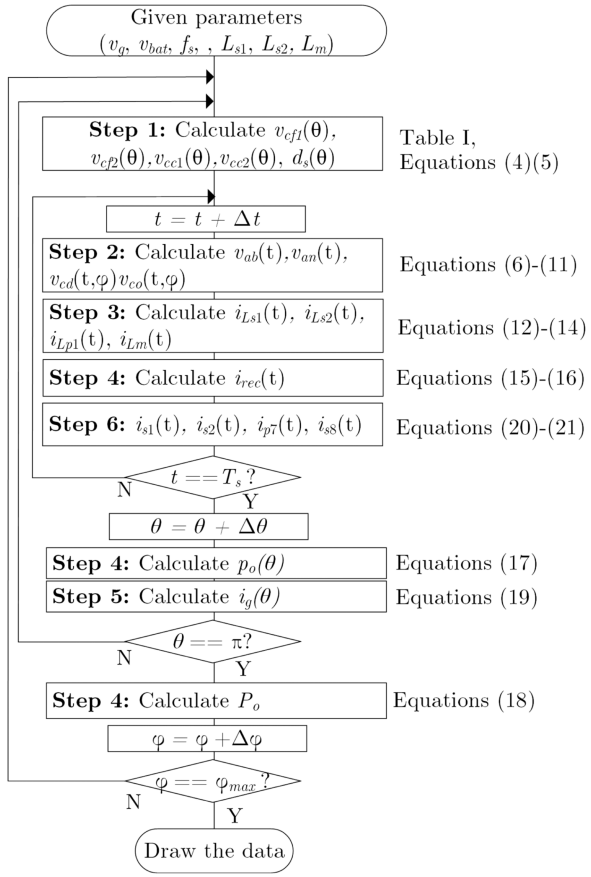

Fig. 6. Flow chart of the proposed analytical model.

Step 3: To calculate the current through series inductance $i_{Ls1}(t)$ and primary side current $i_{Lp1}(t)$ in a switching period. Current $i_{Ls1}(t)$ through the series inductance is calculated according to the voltages across the series inductor in an equivalent circuit

$$\text{In } L\text{-type half-bridge: } \frac{di_{Ls1}(t)}{dt} = \frac{nv_{ab}(t) - v_{cd}(t)}{L_{s1} + L_{s2}} \tag{12}$$

$$\text{In boost half-bridge: } \frac{di_{Ls1}(t)}{dt} = \frac{nv_{an}(t) - v_{co}(t)}{L_{s1}} \tag{13}$$

$$i_{Lp1}(t) = i_{Ls1}(t)/n + i_{Lm}(t). \tag{14}$$

The primary-side current $i_{Lp1}(t)$ is obtained by (14). The magnetizing inductance $i_{Lm}(t)$ is calculated depending on $v_{ab}(t)$ and $v_{an}(t)$ of L-type half-bridge and boost half-bridge-based converters, respectively.

Step 4: To calculate the output power. It is easy to define the rectifier current $i_{\text{rec}}(t)$ from $i_{Ls1}(t)$. In the boost half-bridge converter, two phases are interleaved, and therefore the $i_{Ls2}(t)$ and $v_{do}(t)$ are simply determined by shifting the $i_{Ls1}(t)$ and $v_{co}(t)$ with an amount of 180° in one switching cycle, respectively

$$\text{In } L\text{-type half-bridge: } i_{\text{rec}}(t) = \begin{cases} i_{Ls1}(t) & if(v_{cd} > 0) \\ -i_{Ls1}(t) & if(v_{cd} < 0) \\ 0 & if(v_{cd} = 0) \end{cases} \tag{15}$$

$$\text{In Boost half-bridge: } i_{\text{rec}}(t) = \begin{cases} i_{Ls1}(\text{t}) & if(v_{co} > 0) \\ i_{Ls2}(\text{t}) & if(v_{do} > 0) \\ 0 & if(v_{do} \le 0 \& v_{co} \le 0). \end{cases} \tag{16}$$

The average output power during one switching period is obtained as

$$p_o(\theta) = v_{\text{bat}} \frac{1}{T_s} \int_0^{T_s} i_{\text{rec}}(t) dt \tag{17}$$

$$P_o = \frac{1}{\pi} \int_0^{\pi} p_o(\theta) d\theta. \tag{18}$$

Now, the output power could be expressed as the function of θ. It is noted that the powers of both converters are the same under the same parameters (leakage, input, output voltages, and phase shift). The final power of the converter can be obtained as in (18).

Step 5: To calculate the grid current and THD analysis. Assume that the power loss is ignored, the grid current is obtained by

$$i_g(\theta) = \frac{p_o(\theta)}{v_g(\theta)}. \tag{19}$$

THD of the grid current is analyzed from (19) which is detailed in Section III.

Step 6: Switching current and ZVS condition analysis. The secondary-side switching currents depend on the secondary transformer current. The primary-side switching currents depend on the primary transformer current, magnetizing current, and grid current.

In *L*-type half-bridge converter:

$$i_{s1}(t) = \begin{cases} 0 \quad if(v_{ab}(t) > 0) \\ -(i_{Ls1}(t)/n + i_{Lm}(t) - i_{Lg1}(t)) \quad if(v_{ab}(t) \le 0) \end{cases}$$

$$i_{s2}(t) = \begin{cases} i_{Ls1}(t)/n + i_{Lm}(t) - i_{Lg1}(t) \quad if(v_{ab}(t) > 0) \\ 0 \quad if(v_{ab}(t) \le 0) \end{cases}$$

$$i_{s7}(t) = \begin{cases} -i_{Ls1}(t) \; if(v_{cd}(t) > 0) \\ 0 \quad if \quad (v_{cd}(t) \le 0) \end{cases}$$

$$i_{s8}(t) = \begin{cases} 0 \quad if(v_{cd}(t) > 0) \\ i_{Ls1}(\text{t}) \quad if(v_{cd}(t) \le 0). \end{cases} \tag{20}$$

In boost half-bridge converter:

$$i_{s1}(t) = \begin{cases} 0 \quad if(v_{an}(t) > 0) \\ -(i_{Ls1}(t)/n + i_{Lm}(t) - i_{Lg1}(t)) \quad if(v_{an}(t) \le 0) \end{cases}$$

$$i_{s2}(t) = \begin{cases} i_{Ls1}(t)/n + i_{Lm}(t) - i_{Lg1}(t) \quad if(v_{an}(t) > 0) \\ 0 \quad if(v_{an}(t) \le 0) \end{cases}$$

$$i_{s7}(t) = \begin{cases} -i_{Ls1}(t) \quad if(v_{co}(t) > 0) \\ 0 \quad if(v_{co}(t) \le 0) \end{cases}$$

$$i_{s8}(t) = \begin{cases} 0 \quad if(v_{co}(t) > 0) \\ i_{Ls1}(t) \quad if(v_{co}(t) \le 0). \end{cases} \tag{21}$$

From the calculation of switching currents, the initial turn-ON current of each switch can be easily determined. Detail analysis of the ZVS condition is described in the next section.

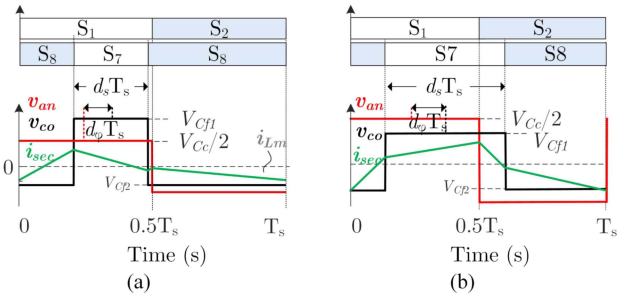

Fig. 7. Two-mode operation of the boost half-bridge-based converter: (a) inner mode and (b) outer mode.

C. Inner Mode and Outer Mode

Fig. 7(a) and (b) shows the key waveform of inner mode and outer mode of the boost half-bridge converter, respectively. These two modes depend on d_s and d_φ. The inner mode is determined when $d_s + 2|d_\varphi| < 0.5$ and the outer mode is determined when $d_s + 2|d_\varphi| > 0.5$. It should be noted that achieving ZVS becomes more challenging at the boundary between the inner and outer modes. This holds true for both boost half-bridge and *L*-type half-bridge-based converters. The detail analysis of ZVS current of primary- and secondary-side switches are presented in the next section.

D. ZVS Turn-On Condition

For simple analysis of ZVS condition, this article ignores the effect of dead time and parasitic capacitance of switches. In general DAB-based converters, the ZVS condition of the primary-side switches is difficult to achieve when $v_{\text{bat}} > nv_{Cc,\text{pk}}$. Meanwhile, the secondary-side switches are difficult to achieve when $v_{\text{bat}} < nv_{Cc,\text{pk}}$. Therefore, in this article, the ZVS condition of primary-side switches (S_1–S_4) and secondary-side switches (S_5–S_8) are analyzed for $v_{\text{bat}} > nv_{Cc,\text{pk}}$ and $v_{\text{bat}} < nv_{Cc,\text{pk}}$, respectively.

Secondary side switches: The worst point for achieving ZVS of both topologies is determined when $d_s/2 + |d_\varphi| = 0.25$. This is a boundary between inner and outer modes as shown in Figs. 4 and 5. Fig. 8 shows the ZVS analysis at near the worst point. The main idea for extending the ZVS in the secondary side switch (S_8) is the slope of the transformer current i_{sec} during the time S_8 turns OFF is small. This helps i_{sec} goes to negative before S_8 turns ON. This negative current is also the turn-ON current of S_8

$$|\text{Slope}_L| = \frac{V_{\text{bat}} - V_{Cc}}{2L_{s1}} \tag{22}$$

$$|\text{Slope}_B| = \frac{V_{cf1} - V_{Cc}/2}{L_{s1}} = \frac{(1-d_s)V_{\text{bat}} - V_{Cc}/2}{L_{s1}}. \tag{23}$$

It is noted that $|\text{Slope}_B| > |\text{Slope}_L|$ when d_s varies from 0 to 0.5; therefore, the boost half-bridge converter is easier to achieve ZVS the *L*-type half-bridge. Indeed, Fig. 8(a) shows the failure of ZVS in secondary-side switches in the *L*-type half-bridge structure. Under the same conditions of power and duty, the slew rate current of the boost half-bridge is larger than the *L*-type half-bridge, which helps to reduce the transformer

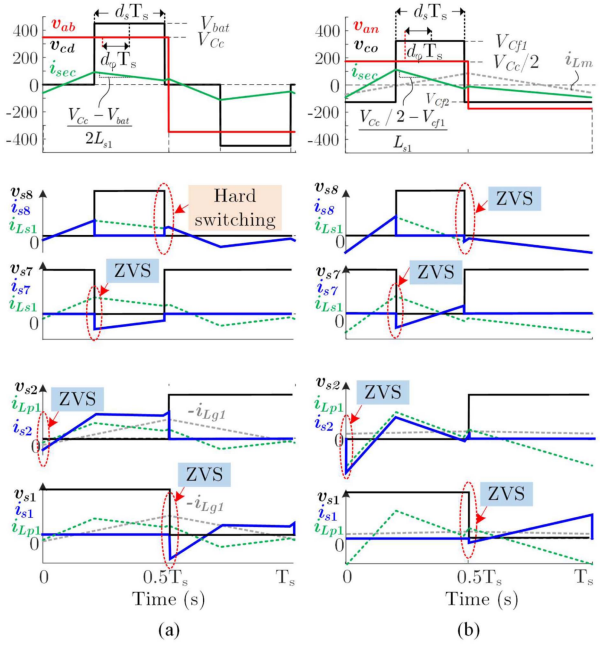

Fig. 8. ZVS condition of the switches at a remarkable point ($\theta = \pi/6$, φ=35°, $v_{\rm bat} < nv_{Cc,\rm pk}$): (a) L-type half-bridge-based and (b) boost half-bridge-based converters.

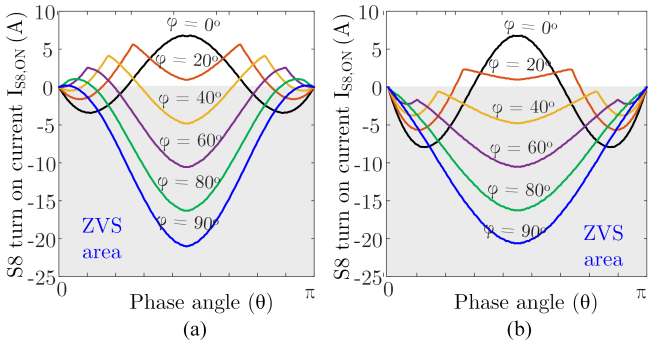

Fig. 9. ZVS condition of the switches in secondary side, $S_{7,8,9,10}$ when $v_{\rm bat} < nv_{Cc,\rm pk}$ (at $v_{\rm bat} = 460$ V) with harmonic injection into φ: (a) L-type half-bridge-based and (b) boost half-bridge-based converters.

current $i_{\rm sec}$ to negative before the S_8 turns ON, resulting in achieving ZVS turn-ON of S_8 while maintaining the ZVS condition of the other switches as shown in Fig. 8(b). Fig. 9 shows the comparison of the ZVS range of two structures under a wide load range. It is also noted that the secondary-side switches of the boost half-bridge structure have a wider ZVS range when $v_{\rm bat} < nv_{Cc,\rm pk}$.

Primary-side switches: ZVS turn-ON conditions of primary switches are difficult to achieve when $v_{\rm bat} > nv_{Cc,\max}$. The turn-ON current of primary-side switches is calculated depending on primary winding current i_{p1}, magnetizing current i_{Lm1}, and grid current i_{Lg1} are expressed as (24) and (25). ΔI_{Lm} and ΔI_{Lg} are current ripples through L_m and L_g, respectively. I_{Lg} is the average current of L_g during one switching cycle. The ZVS condition of the converter can be improved by several approaches including reduction of the filter inductor, reduction of the magnetizing

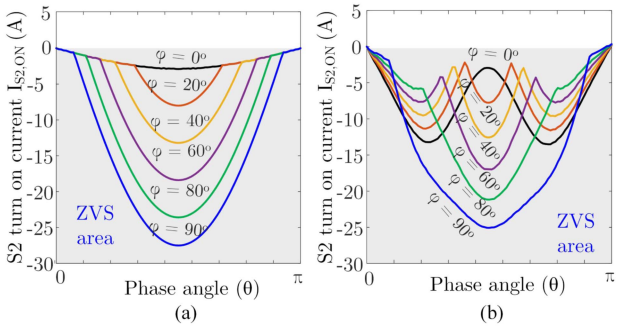

Fig. 10. ZVS condition of the switches in primary side, $S_{1,2,3,4}$ when $v_{\rm bat} > nv_{Cc,\rm pk}$ (at $v_{\rm bat} = 800$ V) with harmonic injection into d_s: (a) L-type half-bridge-based and (b) boost half-bridge-based converters.

inductor, and increase of series inductance

$$i_{S2,\rm on} = i_{S2}(0) = -i_{\rm pri}(0) + i_{Lg1}(0)$$
$$= -i_{\rm sec}(0) - i_{Lm}(0) + i_{Lg1}(0) \quad (24)$$
$$\rightarrow i_{S2,\rm on} = -i_{\rm sec}(0) - \frac{\Delta I_{Lm}}{2} - \frac{\Delta I_{Lg}}{2} + I_{Lg1}. \quad (25)$$

In DAB-based converters, the series inductance is mainly designed for increasing the power transfer capability as well as reducing the rms current of the converter [37]. In early work, the ZVS range of these switches can be extended by reducing the L_g. However, the smaller L_g is, the larger the core loss and turn-OFF loss become; therefore, they are optimally designed depending on the tradeoff between these losses [6]. In this article, the ZVS condition can be extended by reducing both L_g and the magnetizing inductance of transformer L_m. However, L_g is limited for reducing the current ripple when supporting the phase-shedding operation (when only a single leg is operated) of the converter. Fig. 10 shows the ZVS range of the primary-side switches of two topologies.

E. Phase-Shedding Operation

Under the light load, the converter achieves higher efficiency by shedding one phase which reduces due to the reduction of the switching and core losses by half. The converter in [6] is shown to be impossible to do the phase-shedding operation.

The proposed converter can simply operate the phase-shedding operation by turning OFF the switches of one phase as shown in Fig. 2(b). Moreover, the phase-shedding operation also helps to enlarge ZVS range under the low-power range due to operating only one phase with a large phase shift. There is no problem with transient during the mode change since the process of mode change is conducted at zero voltage of the grid. In order to completely isolate the turned-OFF phase, the blocking capacitor is added to the primary side of the transformer [38].

III. Hybrid Harmonic Injection Method

This section presents the harmonic component analysis by using the analytical model from Section II. From the analysis results, a hybrid harmonic injection method is proposed for

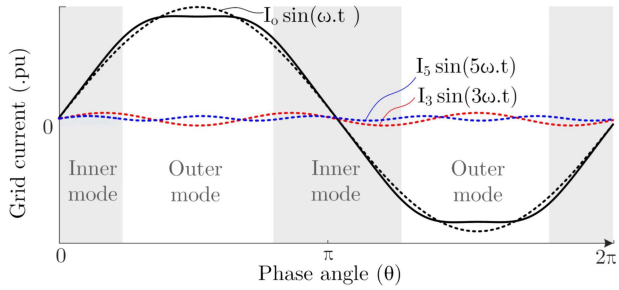

Fig. 11. Harmonic components analysis of the grid current in conventional control method.

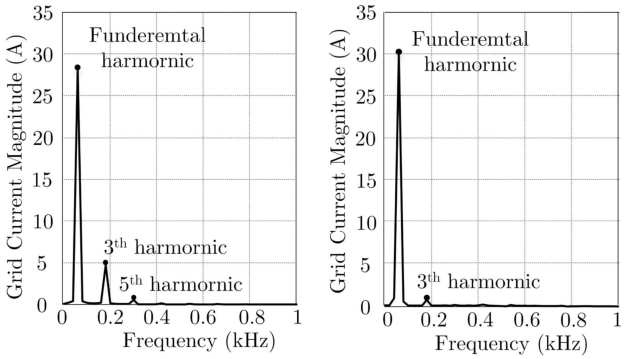

Fig. 12. Harmonic content of the grid current (a) without harmonic injection and (b) with proposed harmonic injection (simulation results).

improving the grid current THD, considering the ZVS condition under a wide voltage range.

A. Harmonic Components Analysis

It starts from the switching method in Table I. The power is a nonlinear function with the duty cycle and phase shift; therefore, even though d_s varies as the sinusoidal function according to θ, the grid current is not a sinusoidal waveform. It is classified into two modes when d_s and d_φ vary according to θ and power level, which includes inner mode and outer mode as shown in Fig. 11. In the inner mode, the power is nearly linear with the function of both φ and d_s. However, in the outer mode, the power is nonlinear with the function of both d_φ and d_s. When the duty cycle d_s reaches to near 0.5, the power of the converter becomes flat. Also, when phase shift increases, the rate of power transfer capability decreases. This is the normal characteristic of the power flow of a DAB-based converter. Consequently, the grid current contains several harmonic components even though d_s is modulated as the sinusoidal waveform as shown in Fig. 11. Fig. 12(a) shows the fast fourier transform (FFT) analysis of the grid current, which contains the fundamental, third, and fifth harmonic components

$$i_g = I_o \sin(\omega t) + I_3 \sin(3\omega t) + I_5 \sin(5\omega t + \pi). \tag{26}$$

The worst case of grid current was considered as a square waveform. The Fourier transformation of a square waveform can be expressed as shown in (27). Assume that the fundamental component is $I_o = 4I_m/\pi$. The magnitude of third and fifth

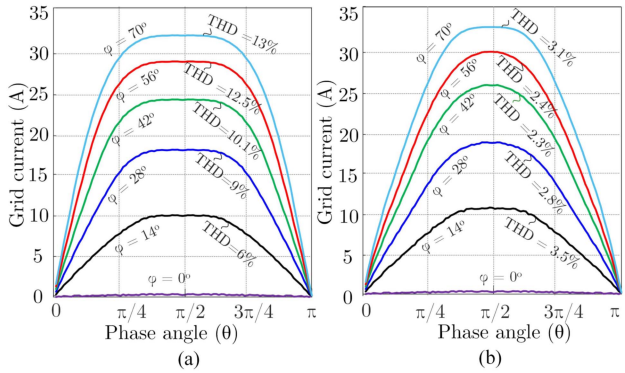

Fig. 13. THD of grid current under different power level ($v_{\rm bat} = 700$ V) (a) without harmonic injection and (b) with proposed harmonic injection.

harmonic components of the grid, I_3 and I_5, are limited to values smaller than $I_o/3$ and $I_o/5$, respectively

$$i_g(t) = \frac{4I_m}{\pi}\left(\sin(\theta) + \frac{1}{3}\sin(3\theta) + \frac{1}{5}\sin(5\theta) + \dots.\right). \tag{27}$$

Fig. 13(a) illustrates the grid current at various power levels when no harmonic injection method is used. The THD exceeds 5% for most of the power range.

B. Proposed Harmonic Injection Methods

There are two methods for improving the THD of the grid current. The first method is to inject the third and fifth harmonic components into φ as shown in Fig. 14(a). The second method is to inject the third and fifth harmonics components into duty d_s as shown in Fig. 14(b). Fig. 14(c) shows the simulation results of grid current with and without harmonic injection. Injecting the harmonic in φ or d_s will affect the ZVS condition of the converter. Fig. 15 presents a comparison of ZVS condition between the two methods when $v_{\rm bat} < nv_{Cc,\rm pk}$. It is evident that with the harmonic injection in d_s, the converter loses ZVS in the range near boundary of inner mode and outer mode. The main reason for this is the reduction of d_s in this range to compensate for the third harmonic component, which reduces the slope of the transformer current. This current is still possible before S_8 turns ON. On the other hand, when injecting the third and fifth harmonic in φ, the d_s does not reduce, which helps the transformer current go to negative before S_8 turns ON. Consequently, injecting harmonics in the φ yields a better ZVS range when $v_{\rm bat} < nv_{Cc,\rm pk}$. Similarly, when $v_{\rm bat} > nv_{Cc,\rm pk}$, injecting the harmonic in d_s provides a better ZVS range compared to injecting the harmonic in φ. Figs. 9(b) and 10(b) show the ZVS condition of proposed converter under entire load range when $v_{\rm bat} < nv_{Cc,\rm pk}$ and $v_{\rm bat} > nv_{Cc,\rm pk}$, respectively.

The ZVS conditions, according to different voltage ranges and harmonic injection methods, are summarized in Table II.

In order to improve THD of the grid current while maintaining the ZVS condition under a wide voltage range, a hybrid injection method is proposed in which the harmonic components are

TABLE II
SUMMARY OF THE ZVS CONDITION FOR ALL SWITCHES, WITH AND WITHOUT THE PROPOSED METHODS

		L-type half-bridge-based				Boost-type half-bridge-based (proposed)			
		$v_{bat} < nv_{Cc,pk}$		$v_{bat} > nv_{Cc,pk}$		$v_{bat} < nv_{Cc,pk}$		$v_{bat} > nv_{Cc,pk}$	
		Primary switches	Secondary switches	Primary switches	Secondary switches	Primary switches	Secondary switches	Primary switches	Secondary switches
Without harmonic injection		O	X	O	O	O	O*	X	O
With harmonic injection	In phase shift, φ	O	X	O	X	O	O*	X	O
	In duty, d_s	O	X	X	O	O	X	O*	O

X: Hard switching. O: Guarantee the ZVS condition. O*: Losing ZVS when phase-shift φ becomes low (low power)

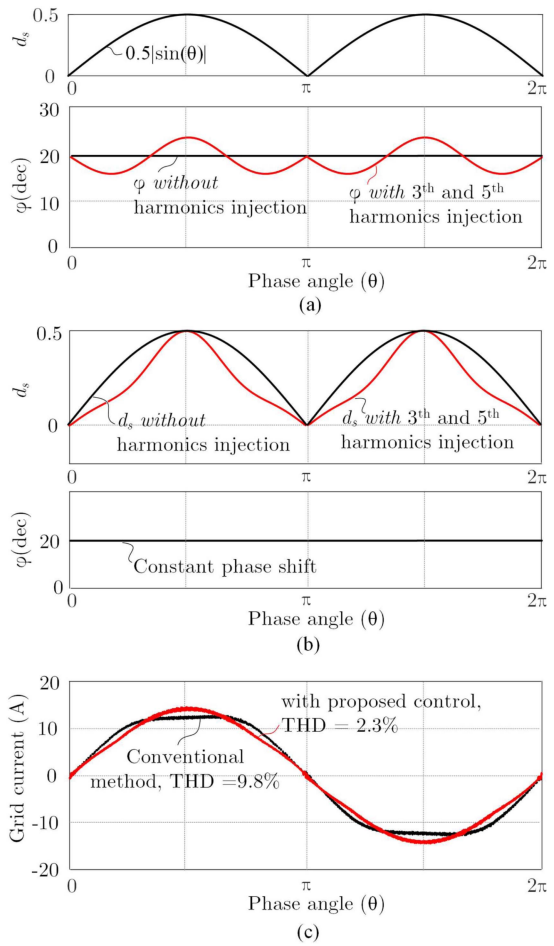

Fig. 14. Simulation of grid current showing the improvement of grid current in case of with and without third and fifth harmonic injection (a) to inject harmonic harmonic components into φ when $v_{\rm bat} < nv_{Cc,\rm pk}$, (b) to inject harmonic components into d_s when $v_{\rm bat} > nv_{Cc,\rm pk}$, (c) and grid current wave form.

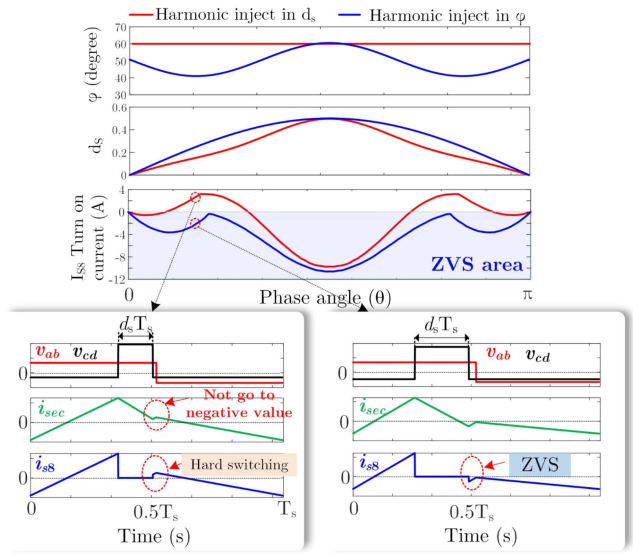

Fig. 15. Comparison of ZVS range between two harmonic injection methods of the proposed converter $v_{\rm bat} < nv_{cc,\rm pk}$.

injected into φ and d_s when $v_{\rm bat} < nv_{Cc,\rm pk}$ and $v_{\rm bat} > nv_{Cc,\rm pk}$, respectively.

Fig. 13(b) shows the grid current under different power in cases of with the proposed control method. It is noted that THD of the grid current is always less than 4% under the whole power level.

The final control block diagram of the converter is shown in Fig. 16. $c_{p,x,}$ and $c_{s,x}$ are carrier waveforms for the primary- and secondary-side legs, respectively. x is 12 with respect to the two phases, those are interleaved by 180°. The active power is regulated based on the phase shift between $c_{p,x,}$ and $c_{s,x}$.

Third and fifth harmonic components are injected into the d_s or φ depending on the information of battery voltage. Figs. 17 and 18 show the simulation results which confirm our proposed harmonic injection method, in which the third and fifth harmonic components were measured and controlled to be zero; the gid current is purely sinusoidal waveform after the harmonic injection method is applied.

IV. DESIGN OF CONVERTER

In this article, a 1.5-kW prototype is implemented to confirm the operation of the proposed converter. The detailed specification is shown in Table III.

A. Grid Inductor

When two phases operate, the grid current ripple is theoretically equal to zero due to the two-phase interleaved effect with a fixed duty cycle of 0.5, regardless of the value of L_{g1} and L_{g2}. In the phase-shedding mode, the maximum grid current ripple is equal to ripple through L_{g1} as follows:

$$\Delta I_{Lg1,\rm pk} = \Delta I_{Lg2,\rm pk} = \frac{v_{g,\rm pk}}{L_g}\frac{T_s}{2} \tag{28}$$

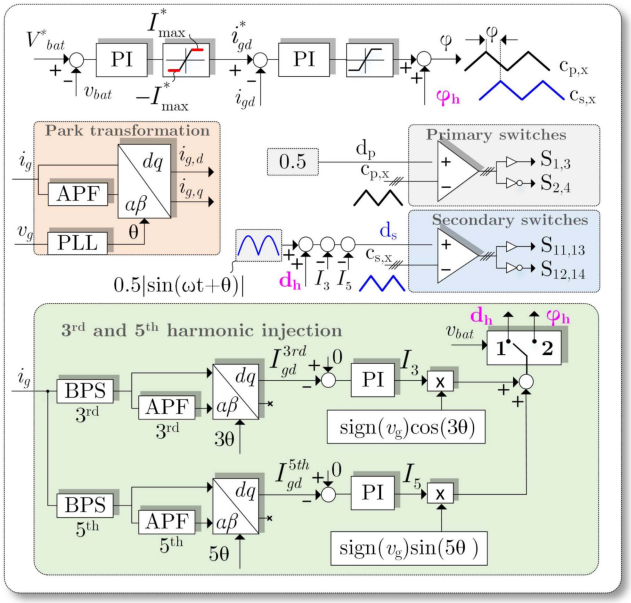

Fig. 16. Control block diagram.

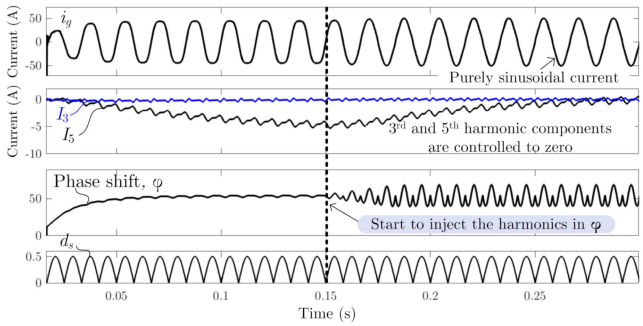

Fig. 17. Simulation results of harmonic injection in φ.

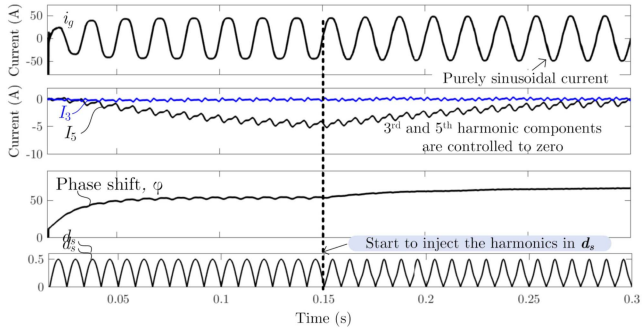

Fig. 18. Simulation results of harmonic injection in d_s.

where $v_{g,\mathrm{pk}}$ is the peak voltage of the grid. In this article, ΔI_{Lg1} is designed around 20% of grid current. From (28), the designed value of L_{g1} and L_{g2} is 300 μH.

TABLE III
SPECIFICATIONS OF PROTOTYPE

Items	Values	Selected devices
Grid voltage	120 Vac	–
Battery voltage	200–500 V	–
Maximum power	1.5 kW	–
Switching frequency	160 kHz	–
Switches (S_{L1}–S_{L8}, S_{H1}–S_{H8})		NVBG040N120SC1
Clamp capacitor C_{C1}, C_{C2}	0.47 μF × 12 =5.64 μF	CKG57NX7R2J474 M500JH (12ea)
Transformer turn ratio	N_s/N_p = 14/14	
Series inductor $L_{s1} = L_{s2}$	20 μH	
Magnetizing inductor L_m	30 μH	
Grid inductors $L_{g1} = L_{g2}$	300 μH	–

B. Magnetizing Inductance

From (25), the ZVS condition of the primary-side switches depends on both current ripple through L_m and L_g as follows:

$$\frac{\Delta I_{Lm}}{2} + \frac{\Delta I_{Lg}}{2} = \frac{1}{2} v_g(\theta) \frac{T_s}{2} \left(\frac{1}{L_m} + \frac{1}{L_{g1}} \right). \tag{29}$$

In this article, L_m is mainly designed for extending the soft-switching region. Decreasing L_m extends the soft-switching region. However, smaller magnetizing inductance causes larger rms current and larger peak turn-OFF current. Therefore, L_m should be properly designed considering the tradeoff between total switching loss and conduction loss [6]. Through the Matlab analysis model, the optimal L_m is selected to be around 40 μH for minimizing total switching and conduction losses. The converter may lose ZVS when the grid voltage is less than 15% of its peak value; however, the switching loss is small due to the low switching voltage and current.

C. Transformer Turn Ratio

The transformer turns ratio is established based on both the peak voltage of the clamp capacitor ($v_{Cc,\mathrm{pk}}$) and the nominal voltage of the battery. With $v_{Cc,\mathrm{pk}} = 2v_{g,\mathrm{pk}} = 338$ V, and considering the nominal voltage of a 400 V class battery to be approximately 360 V, a transformer turn ratio of 1:1 is chosen. The transformer turn ratio of 1:1 facilitates a straightforward transformer design, attributable to the symmetrical winding structure.

D. Series Inductor

A larger series inductance results in a lower (rms) current and a reduction in power transfer capability, while a smaller series inductance leads to a higher current and greater power transfer capability. The series inductance is chosen based on minimizing the rms current meanwhile ensuring the power transfer capability in the whole load range. A detailed analysis approach is presented in [11]. In this prototype, the optimal L_s value is selected at around 20 μH. The transformer is designed with the interleaved winding method for reducing the ac loss of the transformer; however, this reduced the leakage inductance of the transformer. Therefore, an auxiliary inductor is used in series

TABLE IV
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER SINGLE-STAGE TOPOLOGIES

		Proposed converter	[6] [8]	[1]	[18]	[19]	[21]
Topology		Bridgeless totem-pole, boost half-bridge-based	Bridgeless totem-pole, Ltype half-bridge-based	Matrix-based ac–dc converters	Unfolding bridge votlage-fed DAB		
Controller		Simple (phase shift + duty)	Simples (phase shift + duty)	Simples (phase shift + duty)	Complex (variable frequency+ dual phase shift)	Complex (multi-mode control)	Complex (based on look-up table)
Harmonic injection method		Hybrid harmonic injection into phase-shift and duty	Into duty	Into duty	–	–	–
ZVS range		Wider ZVS in low output voltage range	Wide ZVS range	Wide ZVS range	Wide ZVS range	Wide ZVS range	Wide ZVS range
Conduction loss		Lower	Lower	Higher	Higher	Higher	Higher
Phase-shedding capability		Yes	No	No	No	No	No
Protot - ype	Grid voltage	120 Vac	220 Vac	–	208 Vac	220 Vac	230 Vac
	Output voltage	200–500 Vdc	460–800 Vdc	–	200–450 Vdc	400 Vdc	370–450 Vdc
	Power	1.5 kW	3.85 kW	1.44 kW	7.2 kW	1 kW	3.7 kW
	Switching device	SiC	SiC	IGBT	Si, GaN HEMTs	SiC	SUPREMOS MOSFET
	Peak efficiency	96.8%	97.01%	89.96 %	>97.01%	95%	96.2%

with the transformer so that the total inductance is equal to the designed value of 20 μH. Auxiliary inductance is added on the secondary side, which helps to increase the effect of magnetizing current to the ZVS condition.

E. Clamp Capacitor

The clamp capacitor is designed for reducing the HF current ripple and allowing the low-frequency ripple to pass through. Therefore, the design method is only to filter the HF voltage ripple. The voltage ripple is obtained as follows, which is designed to be less than 5% of the maximum voltage of clamp voltage:

$$\Delta V_{Cc} = \frac{I_c}{C_c}\frac{T_s}{4} < 1\% \text{ of } V_{Cc,\max} \tag{30}$$

$$C_{c1} = C_{c2} = \frac{I_c}{0.02V_{Cc1,\max}}\frac{T_s}{4} = \frac{11}{0.02\times 169}\frac{1}{4\times 160000} = 5\mu F. \tag{31}$$

I_c is the absolute average current of the clamp capacitor at the highest power ($\theta = 90^o, P = 1.5$ kW). Finally, $C_{c1} = C_{c2} = 5\ \mu$F.

V. EXPERIMENT RESULTS

Fig. 19 shows a photograph of the implemented 1.5-kW prototype of the proposed converter. Table III shows the main specifications, the design parameters, and selected prototype devices. Two transformers are integrated to reduce the core size. It is noted that the coupling coefficient of the integrated core should be near zero for eliminating the effect between the two phases when it operates the phase shedding. The detailed design of the integrated transformer can be found in [14]. Figs. 20(a), 21(b), and 22(c) show experimental waveforms of the converter under the different battery voltages of 150, 350, and 500 V. It is noted from v_g and i_g waveforms that the converter achieved inherent PFC. The battery current i_b has a low-frequency component (double grid frequency). Grid current i_g has zero ripple

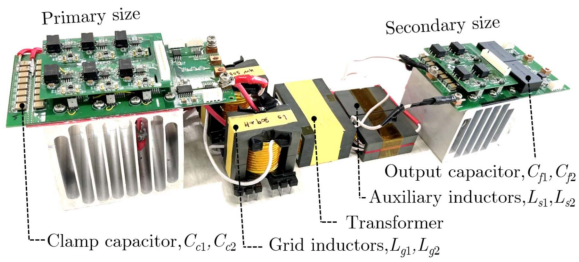

Fig. 19. Photograph of single-stage totem-pole AC–DC based on boost half-bridge structure.

current. Two-phase transformer currents i_{Ls1} and i_{Ls2} are balanced without using balancing control. The experimental results are in close agreement with the analysis and simulation results shown in Fig. 2.

Figs. 21 and 22 show the harmonic injection in the phase shift and the duty cycle in case of low and high v_b, respectively. The THD of grid current is less than 5%. This hybrid harmonic injection according to the battery voltage helps to extend the ZVS turn-ON range of the converter.

When $v_b < nv_{Cc,\text{pk}}$, secondary-side switches (S_7,S_8,S_9,S_{10}) can achieve soft switching (ZCS, ZVS, and partial ZVS) with negative current turn-ON as shown in Fig. 23. Waveforms showing that those switches cannot fully achieve ZVS in some range because the ZVS energy is not enough to discharge the body capacitor. Fig. 24 shows the switching characteristic of primary-side switches S_2 when $v_b > nv_{Cc,\text{pk}}$. The turn-ON current of this switch is calculated as shown in (15) depending on i_{Lp1} and i_{Lg1}. The converter achieves soft switching in the range where the grid voltage is less than 15% of its peak value. From Fig. 25, it can be seen that even though each phase operates in continuous conduction mode, the input currents of the two phases are balanced without the need for balancing control. This is due to the wide ZVS range of operation of the converter, which eliminates the self-turn-ON phenomenon. The issue of

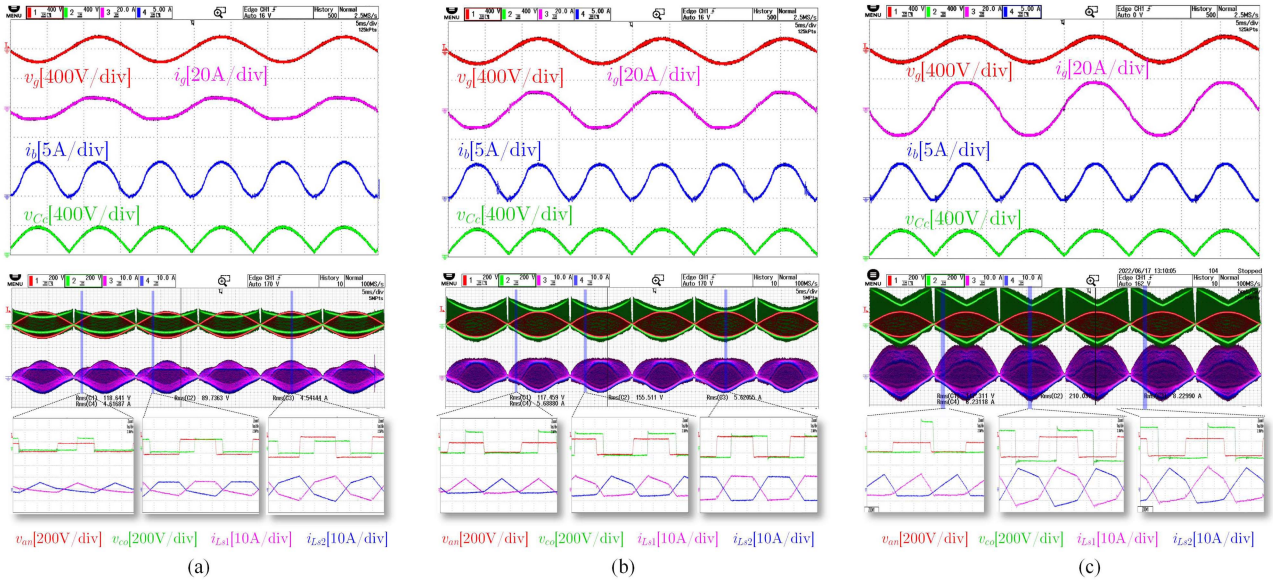

Fig. 20. Experimental waveforms of the converter under full load with the switching method 1. (a) $v_b = 150$ V, $P = 0.57$ kW. (b) $v_b = 350$ V, $P = 1$ kW. (c) $v_b = 500$ V, $P = 1.5$ kW.

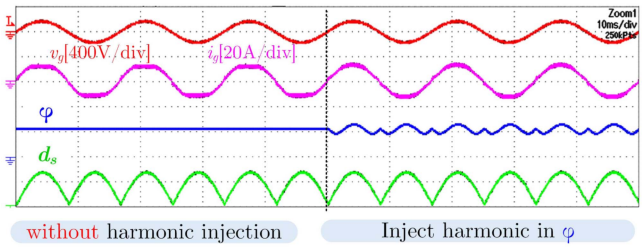

Fig. 21. Harmonic injection in φ when $v_b < nv_{Cc,\mathrm{pk}}$.

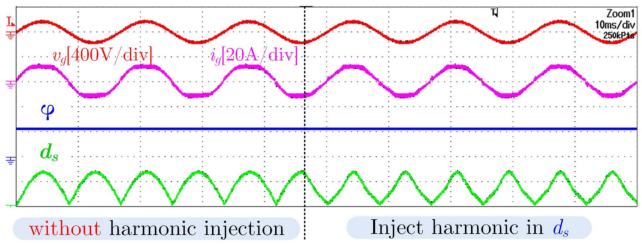

Fig. 22. Harmonic injection in d_s when $v_b > nv_{Cc,\mathrm{pk}}$.

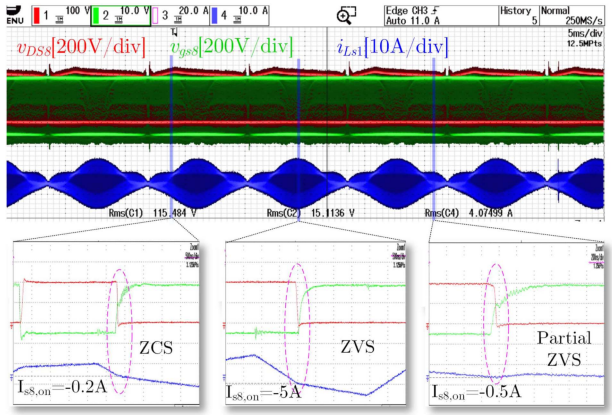

Fig. 23. ZVS analysis of S_2 when $v_b < nv_{Cc,\mathrm{pk}}$ ($v_b = 200$ V, $nv_{Cc,\mathrm{pk}} = 338$ V).

unbalancing can also be caused by a mismatch in duty cycle and a large tolerance of series inductances. Therefore, the converter should have a well-symmetrical circuit layout design and the same series inductance in both phases.

Fig. 26 shows the current and voltage waveforms of the converter in the case with and without phase-shedding operation a. Under a low-power range, only one phase is operated. The power of the converter before and after phase-shedding operation is kept the same at 500 W. The mode change is executed at the zero-crossing point; therefore, there is no transient issue. The transformer current of the shed phase is zero, there is no effect on the other phase. The conduction loss of the operating phase is increased. However, the total loss of the converter reduces due to reduced switching and core losses by half.

Fig. 27 shows the measured efficiency of the proposed converter under different voltages. Peak efficiency is 96.8% when $v_b = 350$ V. The efficiencies under medium and light load are significantly improved compared to the case of *without* phase-shedding operation (dash line). Fig. 28 shows the loss break down analysis of the proposed converter at $v_{\mathrm{bat}} = 350$ V and $P_o = 1.2$ kW. The conduction and switching losses of the switches are obtained by using PSIM simulation. The losses of the transformer and inductor, including core loss and ac copper losses, are obtained by using three-dimensional (3-D) and 2-D Ansys Maxwell simulation, respectively.

Fig. 29 shows the efficiency comparison of two topologies at different battery voltage v_{bat}. In general, the electrical rating of both topologies is similar, the voltage second of the transformer and inductor in both topologies is the same, and therefore the magnetic loss is the same. When the battery voltage is low

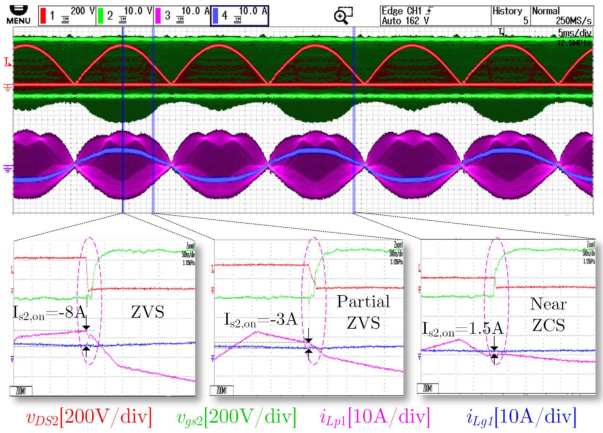

Fig. 24. ZVS analysis of S_8 $v_b > nv_{Cc,\mathrm{pk}}$ ($v_b = 450$ V, $nv_{Cc,\mathrm{pk}} = 338$ V).

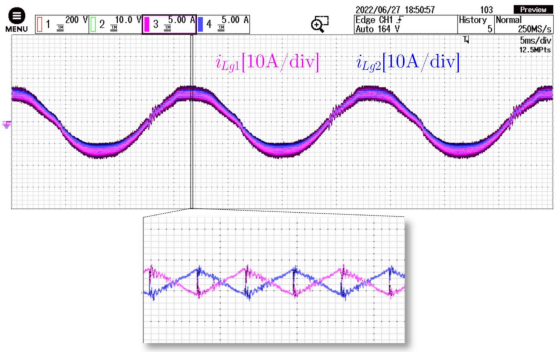

Fig. 25. Experimental result shows the balanced input currents without any balancing control.

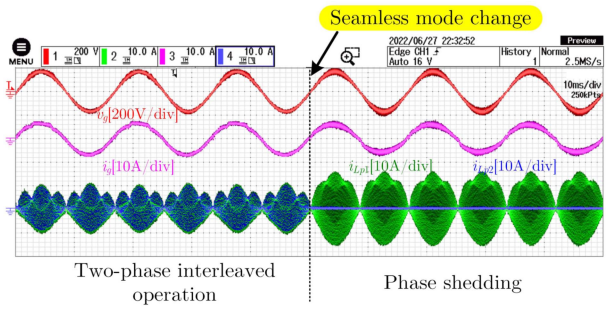

Fig. 26. Phase-shedding operation with seamless mode change.

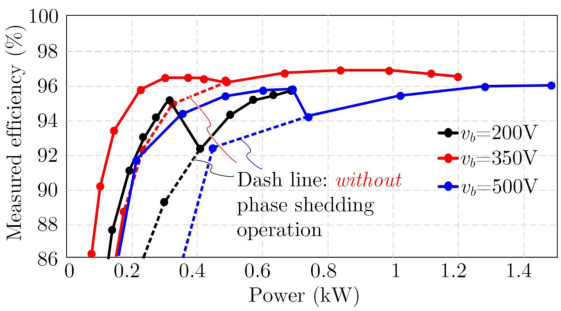

Fig. 27. Efficiency of the proposed converter (measured by Yokogawa WT3000).

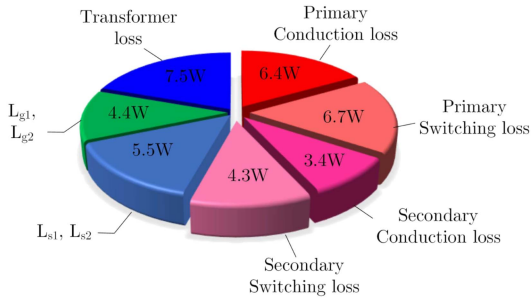

Fig. 28. Loss breakdown of the proposed converter ($v_g = 120$ V, $v_b = 350$ V, $P_o = 1.2$ kW).

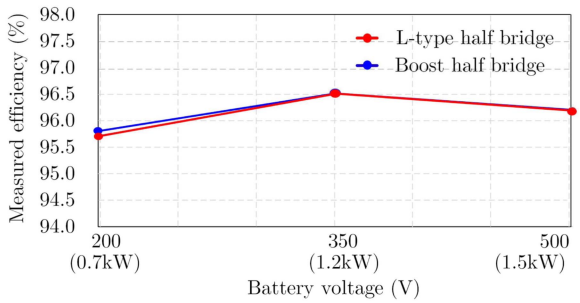

Fig. 29. Efficiency comparison of two topologies at different voltages.

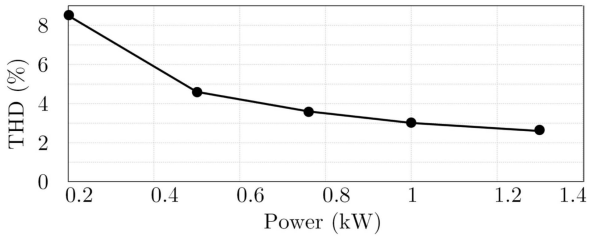

Fig. 30. Measured THD of grid current i_g under different tested load conditions.

(200 V, $P = 0.7$ kW), the efficiency of the proposed converter has slightly increased compared to *L*-type half-bridge.

Fig. 30 shows the measured THD of grid current I_g under different tested load condition. At rated power, the grid current THD is 2.8%, and it stays below 5% when the power exceeds 30% of rated power. Please note that the prototype was not tested with an EMI filter. Therefore, at light loads (less than 40% of the rated power), the THD is low due to the ripple caused by the HF switching components in the system.

Table IV compares the proposed converter with other single-stage topologies presented in [1], [6], [18], [19], and [21]. It is noted that the proposed converter has simple control scheme, which requires only two control variables. Additionally, the converter boasts a wider ZVS range at low output voltage ranges, thanks to its boost half-bridge structure, as compared to [6]. The detailed harmonic injection methods were not discussed in [1], [18], [19], or [21]. Furthermore, the totem-pole operation of the proposed converter results in lower conduction losses, in contrast to [1], where the grid current passes through all back-to-back switches, and [18], [19], and [21], where the grid

current passes through two switches or diodes in series. The voltage-fed topologies in [1], [18], [19], and [21] place higher current stress on the primary-side switch, which also leads to higher conduction losses compared to our proposed converter. Finally, the proposed converter can operate phase shedding, resulting in high efficiency in the light load range, which is challenging to achieve with other topologies.

VI. Conclusion

This article proposed a new single-stage bridgeless totem-pole ac–dc converter for battery chargers. Performances of *L*-type half-bridge and boost half-bridge structures are comprehensively compared to emphasize the advantage of the proposed converter, given that it has a wider ZVS range and the ability of phase-shedding operation. A hybrid harmonic injection method is proposed to not only improve THD to lower than 5% under the whole load range but also extends the ZVS range of the converter under a wide voltage range. According to the battery voltage range, the high-order harmonic component can be injected to phase shift or duty. It is shown to be simple and practical for implementation.

Experimental results from a 1.5-kW prototype are provided to validate the proposed concepts. The converter can achieve a peak efficiency of 96.8% and maintains high efficiency under medium and light loads. The measured efficiency of the phase shedding significantly increases in light to medium load conditions. The proposed control method can be generally applied to the DAB-based single-stage ac–dc converter.

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