A 1.2 V 12 b 60 MS/s CMOS Analog Front-End for Image Signal Processing Applications

Young-Deuk Jeon, Young-Kyun Cho, Jae-Won Nam, Seung-Chul Lee, and Jong-Kee Kwon

This paper describes a 1.2 V 12 b 60 MS/s CMOS analog front-end (AFE) employing low-power and flexible design techniques for image signal processing. An op-amp preset technique and programmable capacitor array scheme are used in a variable gain amplifier to reduce the power consumption with a small area of the AFE. A pipelined analog-to-digital converter with variable resolution and a clock detector provide operation flexibility with regard to resolution and speed.

The AFE is fabricated in a 0.13 μm CMOS process and shows a gain error of 0.68 LSB with 0.0352 dB gain steps and a differential/integral nonlinearity of 0.64/1.58 LSB. The signal-to-noise ratio of the AFE is 59.7 dB at a 60 MHz sampling frequency. The AFE occupies 1.73 mm^2 and dissipates 64 mW from a 1.2 V supply. Also, the performance of the proposed AFE is demonstrated by an implementation of an image signal processing platform for digital camcorders.

Keywords: AFE, VGA, ADC, op-amp preset technique, programmable capacitor array scheme, power management technique, flexibility, low voltage, low power.

I. Introduction

Although the demand for CMOS image sensors has rapidly increased since the early 2000s, CCD sensors have continued to be used in consumer electronics such as digital cameras, digital camcorders, and mobile handsets due to their low noise characteristic. In these applications, power consumption and area of image signal processors are among the most important factors affecting performance [1]. Typically, digital signal processors use a core voltage according to CMOS process. However, analog front-ends (AFEs) which use analog signal processors have been integrated with I/O devices or high-voltage CMOS technology driven above 1.8 V for a large dynamic range [2]-[7]. This has some drawbacks including the power, area, and speed performance. To cope with these problems, implementation with low supply voltage can be a key element to reduce power consumption and area. Since the most conventional AFEs were designed considering a maximum single-ended input signal of around 1.0 V, a supply voltage of 1.2 V is enough for an AFE based on a differential architecture. Also, in order to support various image sensors and frame rates, AFEs must be able to work with different resolutions and operating speeds.

In this work, low-power and flexible design techniques are presented through the implementation of a 1.2 V 12 b 60 Msample/s (MS/s) CMOS AFE in a 0.13 μm CMOS process. This paper is organized as follows. Section II describes the AFE architecture. In section III, several circuit techniques applied to subblocks are proposed. Measured and field test results are presented in section IV, and conclusions are given in section V.

II. Proposed AFE Architecture

Figure 1 shows a block diagram of the proposed AFE for

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Young-Deuk Jeon (phone: +82 42 860 5968, email: ydjeon@etri.re.kr), Young-Kyun Cho (email: ykcho@etri.re.kr), Jae-Won Nam (email: msttia@etri.re.kr), Seung-Chul Lee (email: schlee@etri.re.kr), and Jong-Kee Kwon (jkkwon@etri.re.kr) are with the Convergence Components & Materials Research Laboratory, ETRI, Daejeon, Rep. of Korea.

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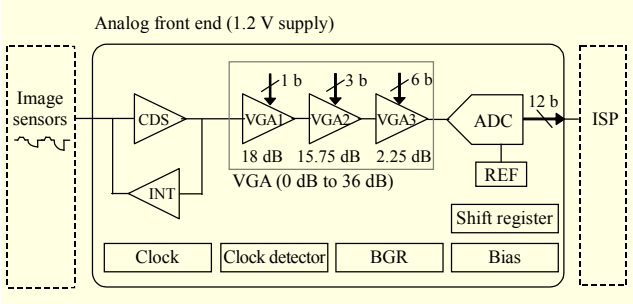

Fig. 1. Block diagram of the proposed AFE.

image sensors. The AFE consists of a correlated double sampler (CDS), integrator (INT), three-stage variable gain amplifier (VGA), 12 b analog-to-digital converter (ADC), band-gap reference (BGR), shift register, bias circuit, clock detector, and clock generator. The CDS uses a ping-pong structure with a single amplifier and two sets of capacitor arrays to increase the amplification period and reduce the power consumption [2], [5]. The integrator with a conventional switched capacitor (SC) architecture is adopted to cancel black level offsets of the image sensor [8]. The VGA is composed of three stages for a 36 dB gain range [9]. The gains of VGA 1 and VGA 2 are changed by selecting feedback capacitors with 18 dB steps of a 1 b digital code and 2.25 dB steps of a 3 b digital code, respectively. In the circuits, the Miller capacitors are digitally controlled to compensate the –3 dB bandwidth, f_{-3dB}, and phase margin variations that are caused by changing the feedback factor. The gain of VGA 3 is 2.25 dB with 0.035 dB steps depending on a 6 b digital code. For a low power and a small area, the VGA adopts an op-amp preset technique and programmable capacitor array (PCA) scheme. The ADC has a pipelined architecture changing resolutions from 8 b to 12 b. The power consumption of the ADC is optimized at the architecture level according to the resolution selection. The clock detector, which recognizes the internal clock frequency generated by the clock generator, controls the current of the bias circuit supplied to all analog blocks. This function optimizes the power consumption of the AFE according to the operational frequency.

III. Circuit Design and Implementation

1. CDS with Offset Calibration

The CDS performs correlated double sampling to remove offset noise of a CCD pixel. The CDS is implemented with an SC circuit based on a ping-pong configuration as shown in Fig. 2. To meet input noise specification, the sampling capacitors of 4 pF are used. All the capacitor arrays are connected to a single-ended CDS input signal, which is

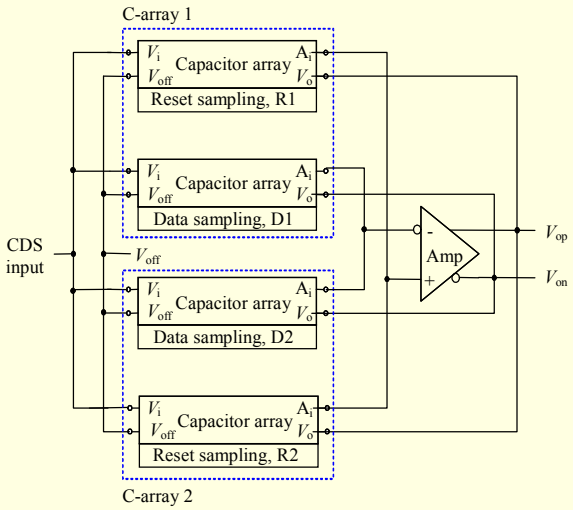

Fig. 2. CDS with ping-pong configuration.

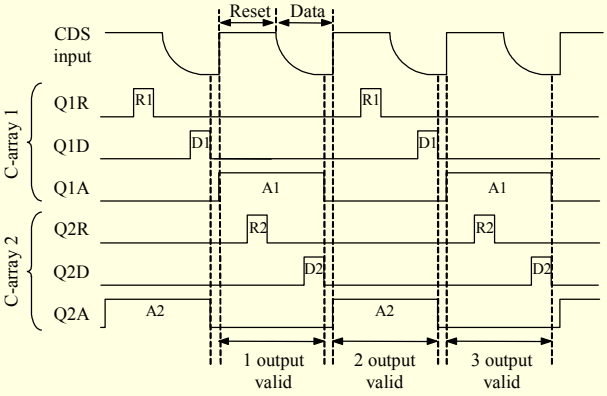

Fig. 3. CDS timing diagram.

composed of a reset value and a data value in turn. Since the maximum analog signal voltage from the image sensors is more than 1.0 V, the sampling switches are implemented with I/O transistors which are driven at a 2.5 V. This improves the image signal linearity and ensures the reliability of the input stage. The other input signal, V_{off}, is generated by the integrator to calibrate the black level offset. An amplifier sharing technique is used to reduce power consumption.

Figure 3 shows a timing diagram of the CDS with the ping-pong configuration. A conventional CDS with a set of capacitor arrays samples the reset value onto a capacitor array during the reset period. During the data period, the CDS subtracts the reset from the data level and amplifies the difference. In this case, the amplification time is identical to the data period. On the other hand, since the CDS with the ping-pong configuration has two capacitor arrays, the amplification operation is performed for the signals after sampling the reset and data values.

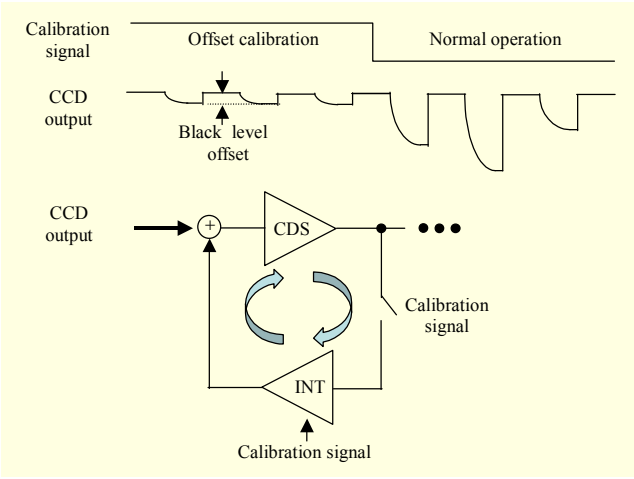

Fig. 4. Black level offset calibration.

The operation of the CDS is carried out as follows. The CDS sequentially samples the reset value (R1) and data value (D1) of the CCD output with the upper sampling network. At the same time, the CDS amplifies the difference (A2) of the reset and data values from a previous pixel with the lower sampling network using the amplifier. In the next phase, the CDS amplifies the difference (A1) with the upper sampling network. Thus, the amplification time of the CDS is 2 times longer than that of the conventional CDS. As a result, the power dissipation and size of the amplifier are decreased.

Although the CDS removes the reset value, the black level offsets of the pixels are still contained in the data value. Figure 4 shows a black level offset calibration. During a calibration period, a feedback loop consisting of the CDS and the integrator measures the average value of the black level from all black pixels. Next, during a normal operation period, the input of the integrator is disconnected from the CDS output, and the output of the integrator is held. Then, the CDS transfers the image signal to the VGAs without the black level offset.

2. VGA with Op-amp Preset Technique

The proposed op-amp preset technique applied to a VGA is illustrated in Fig. 5. It uses a two-stage op-amp with folded-cascode and common source architectures to obtain a high DC gain and large output swing using a 1.2 V supply [10]. Switches SW4, SW5, and SW6, and capacitor C_I are added to implement the proposed technique in a conventional circuit. Capacitor C_P is the sum of the parasitic capacitances at node T2, and C_L is the load capacitor of the second-stage op-amp output. In conventional SC op-amps, the input signal is sampled on the sampling capacitor, C_S, while the feedback capacitor, C_F, is discharged to the common mode voltage, V_{CM}, during the sampling phase, Q1. The second-stage op-amp is simply reset

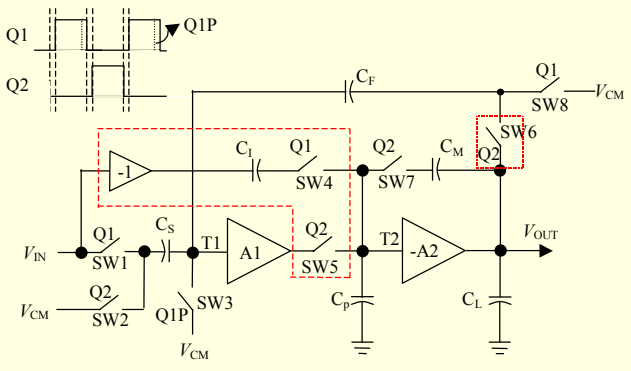

Fig. 5. Op-amp preset technique based on the SC architecture.

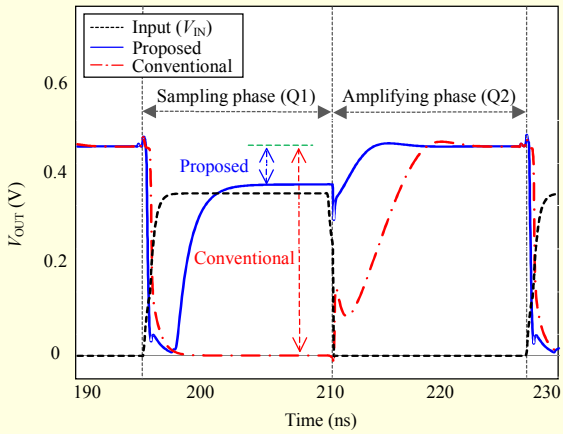

Fig. 6. Comparison of the proposed and conventional techniques.

to V_{CM} and does not contribute any functionality. However, in the proposed technique, the second-stage op-amp resets to around the settling value during Q1, which improves the slewing of the op-amp. During Q1, the analog input signal is sampled on C_S by the clock Q1P. At the same time, in order to operate only the second-stage op-amp, SW4 is turned on, and SW5 and SW6 are turned off. Then, the analog input is applied to C_I through the inverting op-amp with a DC gain of –1 and is divided by the ratio of C_I and C_P at node T2. The inverting op-amp is easily implemented by the cross-coupled connection of the differential input.

The voltage of T2, V_{T2}, is amplified by the DC gain of the second-stage op-amp, –A2; therefore, the output voltage during Q1, V_{OUT_Q1}, is given by

$$V_{OUT\_Q1} = -A2 \times V_{T2} = A2 \times V_{IN} \times C_I / (C_I + C_P). \quad (1)$$

Voltage V_{OUT_Q1} can be controlled by C_I, as C_P and A2 are decided on the circuit.

During the amplifying phase, Q2, the switches SW 2, SW 5, SW 6, and SW 7 are turned on, and the sampled analog input is amplified by the ratio of C_F and C_S as in a conventional circuit. In this case, the amplified output moves from V_{OUT_Q1}. Thus,

the acquisition time of the SC op-amp is decreased because of the reduced slewing time, and low-power consumption can be achieved.

The simulated output waveform of the proposed SC op-amp is compared with a conventional one in Fig. 6. The results show that the proposed technique reduces the acquisition time of the op-amp by about 30% at 60 MS/s without additional power consumption.

3. VGA 3 with PCA Scheme

Figure 7 shows VGA 3 with the proposed PCA scheme to minimize the number of capacitors and switches. The PCA can adjust the dB-linear gain that follows the first-order approximation $(1+x)/(1-x)$ [11], [12]. It is composed of the unit capacitor array, which is segmented between the upper 3 b and lower 3 b capacitors by a split capacitor. The value of the unit capacitor is 60 fF. In the PCA, the capacitors connected between nodes X and A_{IN} are indicated to C_X, and the capacitors connected between nodes A_{IN} and Y are indicated to C_Y. The total capacitance (C_X+C_Y) of the PCA is identical to 472.5 fF of C_T. In Q1, the analog input signal is sampled on C_S, C_T, and C_X. The remaining capacitors, C_Y, of the PCA are connected to V_{CM}. In Q2, the bottom plates of C_S and C_Y are connected to the op-amp output, and C_T and C_X are connected to V_{CM}. Therefore, the voltage gain, G_{VGA3}, of VGA 3 can be expressed as

$$G_{VGA3} = (C_S+C_T+C_X)/(C_S+C_T-C_X). \quad (2)$$

Due to the additional capacitor, C_T, VGA 3 has a larger feedback factor of $(C_S+C_T-C_X)/(C_S+2\times C_T)$, which reduces power consumption and kT/C noise compared with a conventional one [11].

4. Pipelined ADC with Variable Resolution Technique

The AFE also includes a 12 b 60 MS/s fully-differential pipelined ADC having an internal reference generator and a bias circuit as shown in Fig. 8. It is composed of five 2.5 b stages followed by a 2 b flash ADC, and a sample-and-hold amplifier is omitted because the VGA 3 driving the ADC has a hold function. The 6 b digital code, D_{C1} to D_{C6}, generated by a mode control circuit enables each stage to change the resolution of the ADC with 12 b, 10 b, and 8 b.

The resolution of conventional ADCs can be varied by turning off the function blocks from the last stage. The conventional architecture can be easily implemented in the circuits but has a disadvantage of low power efficiency because the power consumption of the front stages is higher than that of rear stages.

On the other hand, the resolution of the proposed ADC can be changed by turning off the function blocks from the first

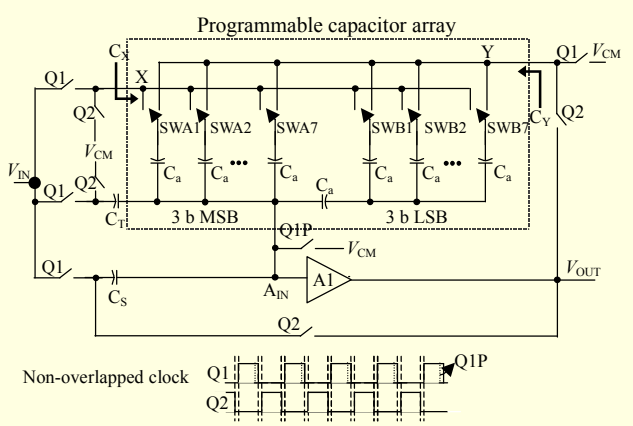

Fig. 7. VGA 3 with the proposed PCA scheme.

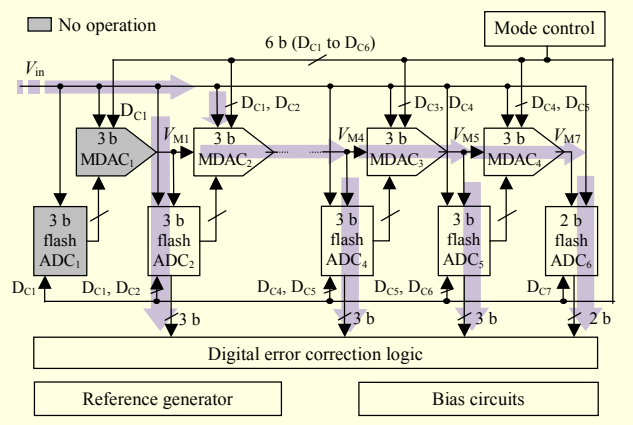

Fig. 8. Fully-differential pipelined 12 b ADC architecture with variable resolution of 10 b.

stage. Figure 8 shows a 10 b ADC operation in variable resolution mode. If the 6 b code, D_{C1} to D_{C6}, is 011111, the first stage including the MDAC1 and flash ADC1 is disabled, and the analog input signal is directly applied to the second stage. The first stage, which is bypassed, goes into power-down mode to reduce the power consumption. In this case, although the 12 b ADC is operated at a 10 b resolution, the power dissipation of the ADC is optimized to a 10 b resolution.

5. Clock Detector with Power Management Technique

The sampling clock frequency of the AFE can be varied from 18 MHz to 60 MHz to support the various resolutions of image sensors and multiframe rates of applications. According to the operation frequency, the bias current of the AFE must be controlled to optimize the power consumption. The clock detector performs the function of detecting the clock frequency and controlling the bias circuits with digital codes.

The clock detector consists of a time-to-voltage converter (TVC) with a capacitor, a current source, two switches, and a

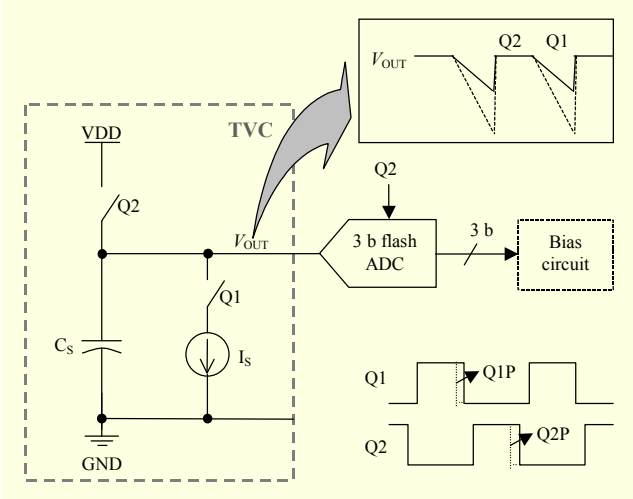

Fig. 9. Clock detector based on TVC and 3 b ADC.

3 b flash ADC as shown in Fig. 9. The operation of the clock detector is carried out as follows. First, the top plate of the capacitor, C_S, in the TVC is connected to VDD to reset to the initial condition during Q2. Next, the capacitor is discharged by the current source, I_S, reaching a final value inversely proportional to the clock frequency during Q1. The voltage of the capacitor top plate, V_{OUT}, shows a saw tooth waveform. When the clock frequency is low, the slope of the waveform is larger, like the dotted line in the figure. The 3 b flash ADC samples the V_{OUT} at the end of Q1 and generates the corresponding digital code in Q2. The 3 b digital code controls the amount of current supplying the analog blocks, such as the CDS, the integrator, the VGAs 1 to 3, and the ADC.

IV. Experimental Results

The proposed AFE was fabricated in a 0.13 μm 1P6M CMOS process as shown in Fig. 10. The active die area of the AFE is 1.73 mm^2 (2.43 mm × 0.71 mm). The measured differential non-linearity (DNL) and integral non-linearity (INL) at 12 b accuracy are plotted in Fig. 11. The DNL is +0.62/-0.64 LSB, and the INL is +1.52/-1.58 LSB.

Figure 12 shows the measured FFT plot and dynamic performance of the AFE. The signal-to-noise ratio (SNR) and signal-to-noise-and-distortion (SINAD) are 59.7 dB and 57.6 dB at a 2 MHz input and 60 MHz sampling frequency, respectively. In the measured dynamic performance versus sampling frequency plot for a 2 MHz input frequency, the prototype AFE maintains an SNDR of better than 57.6 dB up to 60 MS/s.

Figure 13 shows the measured gain and gain error of the AFE against a 10 b control code. The AFE offers up to 36.03 dB of dB-linear gain range with 0.0352 dB gain steps

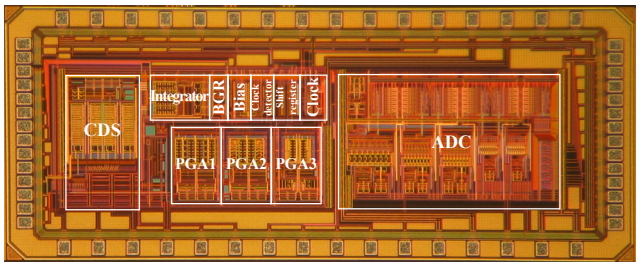

Fig. 10. Chip photograph.

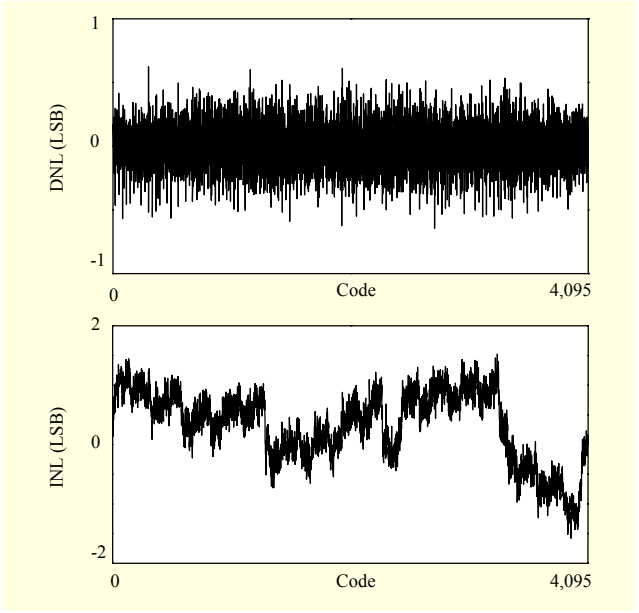

Fig. 11. Measured DNL and INL.

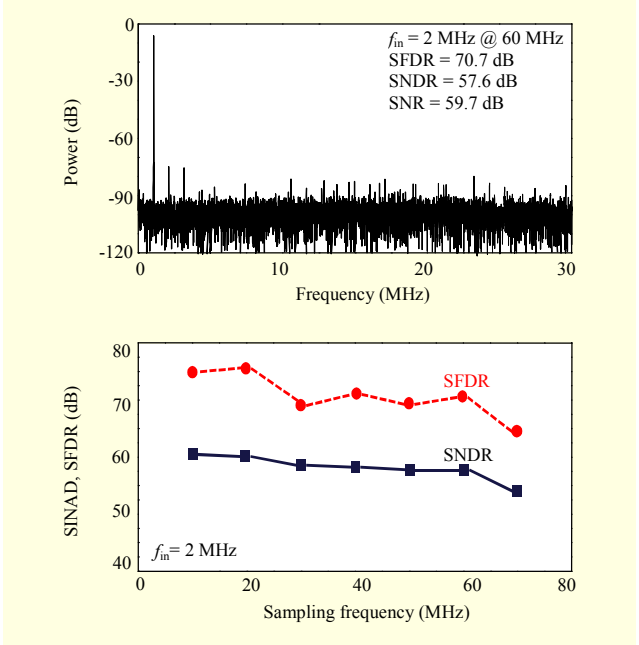

Fig. 12. Measured FFT plot and dynamic performance.

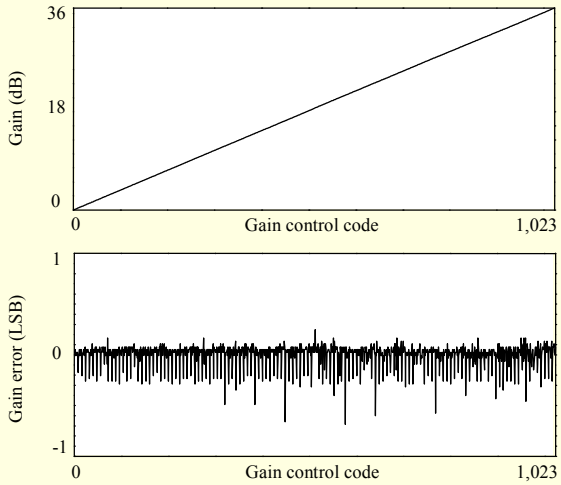

Fig. 13. Measured gain and gain error of the AFE.

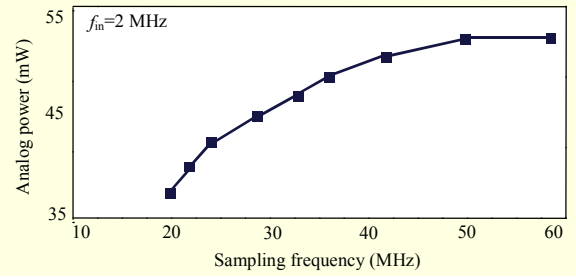

Fig. 14. Measured analog power vs. sampling frequency.

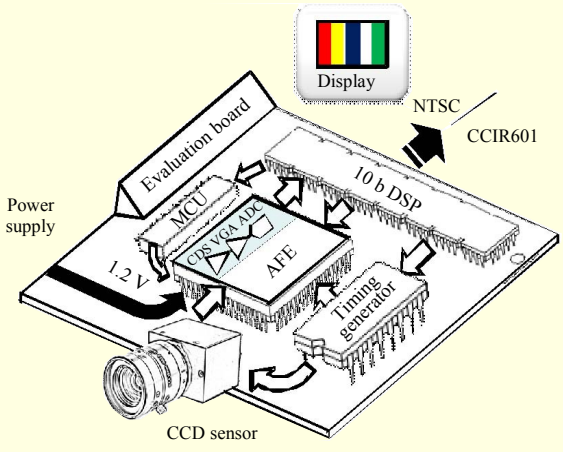

Fig. 15. Functional block diagram of the image signal processing platform.

and a gain error of less than ±0.68 LSB.

The measured analog power consumption of the AFE is plotted in Fig. 14. Since the clock detector controls the current of the analog blocks, the analog power consumption is reduced as the operation frequency is decreased to 20 MHz.

Fig. 16. Image captured by the prototype camera module.

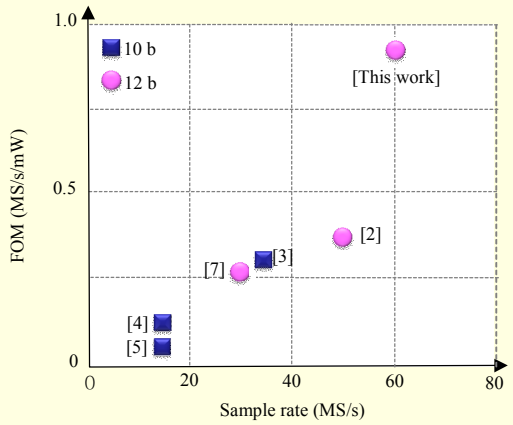

Fig. 17. Performance comparisons.

An image signal processing platform for a digital camcorder was implemented to evaluate the performance of the proposed AFE. A functional block diagram of the platform is shown in Fig. 15. A compact 1/3 inch CCD image sensor with 410k pixels was used to capture images, and the timing generator circuitry generates the necessary signal to clock the CCD.

The output of the imager is acquired by the CDS/VGA circuit and digitized by the ADC. The internal parameters of the AFE are controlled by the microcontroller. The digitized CCD data is sent to the digital signal processor (DSP), and the output of the DSP meets the analog NTSC specifications and CCIR601 format to allow images to be viewed through a TV monitor or stored in a memory card. Figure 16 shows an image reproduced through the image signal processing platform.

Figure 17 shows the performance of the AFE compared to that of conventional AFEs. The total power consumption of the proposed AFE including analog and digital blocks is 64 mW at 60 MHz and a 1.2 V supply. The figure of merit (FOM) of the AFE is defined as

$$\text{FOM} = f_{CK} / P_{DISS}, \quad (3)$$

Table 1. Summary of the AFE specifications.

Process	0.13 μm 1P6M CMOS
Resolution	12 b / 10 b / 8 b
Conversion rate	60 MS/s
Supply voltage	1.2 V
Power consumption	64 mW
DNL, INL	+0.62/-0.64 LSB, +1.52/-1.58 LSB
SINAD	57.6 dB @ f_{in}=2 MHz, f_{CK}=60 MHz
SNR	59.7 dB @ f_{in}=2 MHz, f_{CK}=60 MHz
Gain range/step	0 dB to 36.03 dB / 0.0352 dB
Gain error	0.68 LSB
Active die area	1.73 mm^2 (2.43 mm × 0.71 mm)
FOM	0.94 MS/s/mW

where f_{CK} is the sampling frequency and P_{DISS} is the power dissipation. The FOM of the proposed AFE is 0.94 MS/s/mW. It is the highest value of the AFEs with similar resolution. The measured specifications of the prototype AFE are summarized in Table 1.

V. Conclusion

A 1.2 V 12 b 60 MS/s CMOS AFE with low-power and flexible design techniques has been proposed in this paper. The power consumption of the AFE can be reduced by the op-amp preset technique and PCA scheme. The variable resolution ADC and clock detector schemes provide optimum operation conditions according to the clock frequency and resolution variations of the AFE. These results indicate that the proposed AFE is applicable to portable high-performance digital still cameras and digital camcorders.

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Young-Deuk Jeon received the BS and MS degrees in electronic engineering from Sogang University, Seoul, Korea, in 1998 and 2000, respectively. Since September 2005, he has been with ETRI, Korea. He is working mainly on mixed-mode integrated circuit design as a researcher. His current interest is in communication systems based on high-resolution low-power CMOS data converters and low-voltage low-power CMOS analog circuit design.

Young-Kyun Cho received the BS degree from Ajou University, Suwon, Korea, in 2001, and the MS degree from POSTECH, Pohang, Korea, in 2003, both in electrical and electronics engineering. He is currently with ETRI, Daejeon, Korea, as a member of research staff. His research interests are novel devices, mixed signal circuits and Nyquist-rate ADCs. Mr. Cho was the recipient of the Best Paper Award at the IEEE Nanotechnology Materials and Devices Conference in 2006.

Jae-Won Nam received the BS and MS degrees in electrical communications engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2006 and 2008, respectively. Since February 2008, he has been with ETRI, Korea, a non-profit government-funded research organization. He is working mainly on mixed-mode integrated circuit design as a member of engineering staff. His current interests are high-resolution high-speed with low-voltage low-power CMOS A/D converters and analog interfaces for sensor or MEMS systems.

Seung-Chul Lee received the BS and MS degrees in electronic engineering from Sogang University, Seoul, Korea in 1998 and 2000, respectively. Since July 2000, he has been with ETRI, Korea, a non-profit government-funded research organization. He is working mainly on mixed-mode integrated circuit design as a senior researcher, and his current interest is in communication systems based on high-resolution high-speed CMOS data converters and low-voltage low-power CMOS analog circuit design.

Jong-Kee Kwon received the BS and MS degrees in electronics engineering from Yeungnam University, Korea, in 1981 and 1983, respectively, and the PhD in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), in 2004. Since 1984, he has been with ETRI, Korea, a government supported institute, working mainly on the development of analog integrated circuits (ICs). As the technical manager of the Mixed-Signal Product Engineering Department at ETRI, he is currently involved in the development of high-speed, high-performance mixed-signal ICs including low-voltage/low-power analog functions, amplifiers, high-speed/high-resolution data converters, PLL/VCO, ESD I/O, and analog interfaces for sensor or MEMS systems.