An Embedded Passive Gain Technique for Asynchronous SAR ADC Achieving 10.2 ENOB 1.36-mW at 95-MS/s in 65 nm CMOS

Jae-Won Nam, *Student Member, IEEE*, and Mike Shuo-Wei Chen, *Member, IEEE*

***Abstract*—This paper demonstrates an asynchronous successive-approximation-register (SAR) analog-to-digital converter (ADC) architecture with an embedded passive gain technique for low-power and high-speed operation. The proposed passive gain technique relaxes the noise requirement of the comparator and reuses the existing capacitor DAC in SAR for minimal overhead. An additional time-out scheme is adopted to advance the SAR conversion whenever the comparator takes longer time to resolve, which improves the overall conversion rate. To prove the concept, an 11-bit ADC prototype was fabricated in 65 nm CMOS technology. The prototype measured a peak effective number of bits (ENOB) of 10.2 and a spurious-free dynamic range (SFDR) of 75.2 dB at a 95-MS/s sampling rate with 1.36-mW power consumption from a 1.1 V supply. The measured static differential nonlinearity (DNL) and integral nonlinearity (INL) were less than $\pm$ 0.84 LSB with a differential input swing of 1.6 V_{pp}.**

***Index Terms*—Complementary metal-oxide-semiconductor (CMOS), passive gain, successive approximation register (SAR) analog-to-digital converter (ADC).**

I. Introduction

SUCCESSIVE-APPROXIMATION-REGISTER (SAR) analog-to-digital converters (ADCs) favor technology scaling due to mostly digital implementations, and allow a wide range of resolutions and sampling speeds, making them ideal for both wired and wireless applications. SAR ADCs are also power-efficient, as the successive approximation algorithm avoids redundant comparisons and typically utilizes only one comparator. Furthermore, the conversion speed constraint is mitigated by the asynchronous SAR architecture, which was proposed in [1] and demonstrated for high speeds and medium resolution. However, the SAR architecture is limited by the noise and finite settling time of the comparator and capacitor DAC, which makes further enhancing ADC resolutions at high sampling rates difficult. The DAC settling time constraint can be mitigated with a non-binary search algorithm [2] and asynchronous implementation [3]. Optimizing the comparator performance typically involves increasing the power consumption to lower the input referred noise [4] and reduce the overall comparator propagation delay. On the ADC architecture level, there are alternatives to help improve the conversion speed, such as a pipelined SAR architecture [5], [6] or a multi-bit per conversion SAR architecture [7]. Either case incurs extra active circuits and hence higher power consumption. Therefore, more efficient ways to resolve the speed-resolution-power trade-offs are required.

This work aims to further advance the asynchronous SAR architecture into a high-resolution, high-sampling rate regime, where sampling (kT/C) and comparator noise become dominant factors that demand extra speed and power overhead. To alleviate the speed-resolution-power trade-off, an asynchronous SAR ADC with an embedded passive gain architecture [8] is thus proposed and prototyped in 65 nm CMOS technology to not only speed up conversion but also to relax the comparator noise requirement. The prototype achieves 95-MS/s and $>$ 10-bit ENOB with 1.36-mW power consumption in the silicon measurement.

This paper is organized as follows: Section II introduces the proposed passive gain technique and provides an analysis of the power trade-offs, noise, and conversion speed of this technique. Section III describes the implementation details of the ADC. The measurement results are presented in Section IV, followed by the conclusion in Section V.

II. Analysis of Proposed Gain Technique

A. Motivation

This section describes the key concept of the proposed passive gain topology for SAR ADC, and provides the performance analysis and comparison with a conventional asynchronous SAR ADC architecture. Specifically, the overall noise, conversion speed, and power efficiency of the proposed technique will be discussed.

A conventional N-bit asynchronous SAR ADC is illustrated in Fig. 1(a). The input signal is sampled onto a capacitor array, followed by a comparator and an asynchronous SAR logic. The comparator compares the polarity of the residue voltage in successive stages, where the residue voltage is generated via the capacitor array. The key idea of passive-gain-assisted SAR architecture is to insert an additional gain stage in between the capacitor array and the comparator, as shown in Fig. 1(b). Due to the additional gain, the desired input is amplified, allowing relaxed comparator noise and faster settling speeds of the comparator. In addition, the relaxed requirement on the comparator design allows us to choose smaller input

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The authors are with the Department of Electrical Engineering University of Southern California, Los Angeles, CA 90089 USA (e-mail: jaewon.nam@usc.edu).

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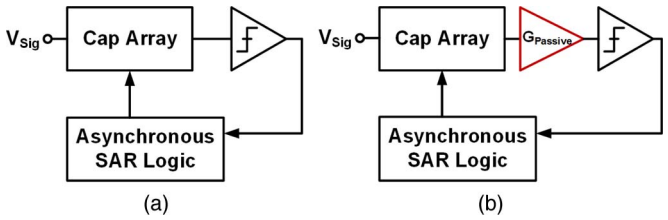


Fig. 1. (a) Conventional asynchronous SAR ADC and (b) proposed asynchronous SAR ADC with passive gain stage.

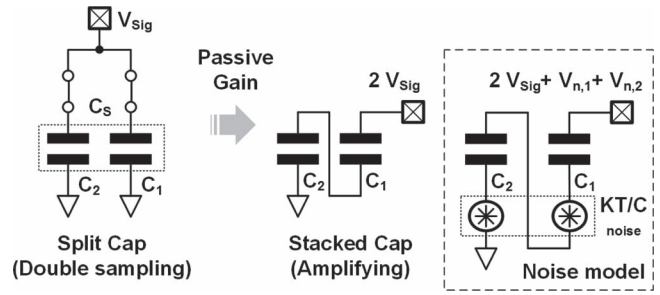


Fig. 2. Proposed passive gain scheme.

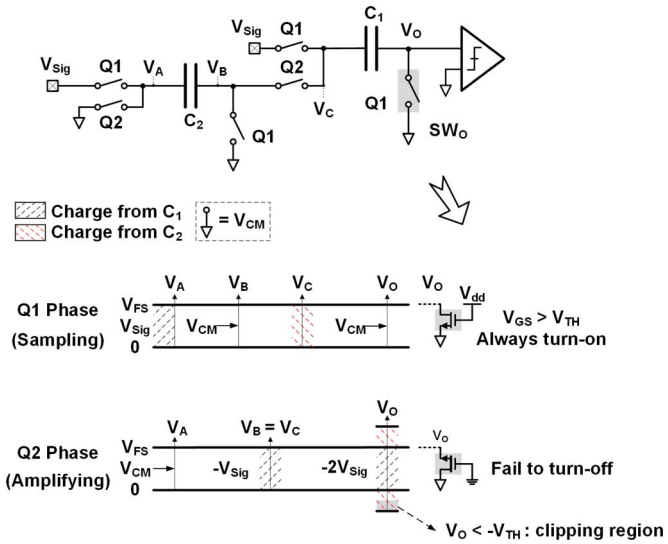


Fig. 3. Signal swings out of tolerable range after capacitor stacking.

pair, which results in reduced input capacitance. In order to maximize power efficiency, we propose to implement a passive gain stage that avoids static current consumption. In the simplest configuration, the input signal is simultaneously sampled on two capacitors during the sampling phase and stacked up during the amplification phase (see Fig. 2). After capacitor-stacking, the output voltage is twice the sampled input voltage. The capacitor-stacking technique has been used in DC-to-DC conversion [9] and pipelined ADCs [10] with limited resolution.

However, as the passive gain technique amplifies the magnitude of the sampled signal, the enlarged signal can cause improper operation of the internal MOSFET switches, especially when the ADC input is designed close to the rail-to-rail range. As shown in Fig. 3, the passively amplified signal can be clipped whenever the voltage at the comparator input falls below ground level by the threshold voltage (V_{TH}) of the bottom-plate switch (SW_O). In this case, the switch starts to conduct current when it should be off. To ensure the proper switch

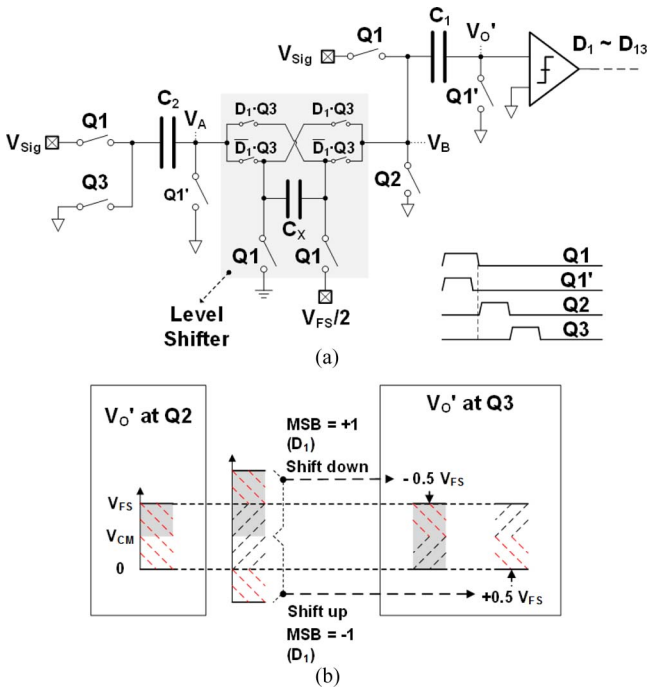


Fig. 4. (a) Proposed level shifting circuit and (b) bounded voltage swing range after level shifting up/down.

operation, an additional level-shifting circuit is implemented, as illustrated in Fig. 4(a). The idea is to connect a pre-charged capacitor, C_X, in between the two stacked capacitors (C_1 and C_2) with two possible directions. When the signal voltage is determined to go below ground, C_X should be connected in a direction that shifts the level up, and vice versa. The action of shifting the level up or down can be simply determined by the first MSB decision result (D_1), which is based on the output voltage of capacitor C_1 without capacitor-stacking. In the case of binary successive approximation, the capacitor is first initialized to half of the full scale voltage ($V_{\mathrm{FS}}/2$) during the input tracking phase, and thus ensures that the signal swing at every internal node after capacitor-stacking is always bounded within the supply rail, as shown in Fig. 4(b).

In the following subsections, we will discuss the impact of applying passive gain technique to SAR ADC. It has been found that the most significant impact of the passive gain technique is the relaxed comparator design constraint while maintaining a similar charge redistribution speed as in the conventional asynchronous SAR ADC.

B. Power Efficiency Enhancement

Assuming the passive gain stage provides a voltage gain of G_{Passive}, the input referred noise in front of the passive gain stage will scale down the comparator noise by a factor of G_{Passive}. Here, we focus only on the comparator noise; the sampling noise effects are discussed in the next subsection.

Considering a typical regenerative comparator [11], the input referred noise can be expressed as

$$P_{n,\mathrm{comp}} = \frac{1}{G_{\mathrm{Passive}}^2}\frac{kT}{C_L}\rho\gamma \tag{1}$$

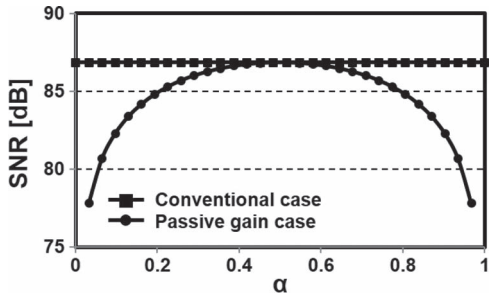


Fig. 5. SNR comparison between conventional and the proposed sampling network versus a capacitor weighting factor with 4 pF sampling capacitor and 1.6 V_{pp} input swing.

where γ is the thermal noise factor, ρ is a topology-dependent constant relying on the number of transistors contributing the noise, and C_L is the comparator's load capacitance. Given the same noise performance with $G_{\mathrm{Passive}} > 1$, the load capacitance can be scaled down by a factor of G^2_{Passive}. In terms of comparator speed, the regenerative comparator bandwidth is proportional to g_{m}/C_L [12]. Therefore, the transconductance (g_{m}) of regenerative transistors can be lowered by the same ratio as the load capacitor for a fixed bandwidth. Assuming g_{m} scales proportionally with the bias current given the same voltage bias, the comparator' s power consumption can be reduced by four times when G_{Passive} is two. In the SAR architecture, as the comparator' s power consumption is a dominant factor in the analog portion of the ADC, the proposed passive gain helps to improve the overall ADC power efficiency.

C. Noise Trade-Offs

In this subsection, we discuss the sampling and comparator noise when applying the passive gain technique. In the passive gain network, the analog input is first sampled via two separate switches and capacitors, and then configured in series during the SAR conversion phase. As a result, the kT/C sampling noise power from each capacitor ($\overline{V^2_{n,1}}$ and $\overline{V^2_{n,1}}$) should be summed while the input signal amplitude is doubled after capacitor-stacking as illustrated in Fig. 2. Assuming the sampling noise from C_1 and C_2 are uncorrelated due to separate switches, the signal-to-noise ratio (SNR) at the sampling network output in the conventional and passive gain cases can be expressed as

$$\mathrm{SNR}_{\mathrm{Conv}} = 10 \cdot \log_{10} \frac{P_{\mathrm{Sig}}}{kT/C_{S,\mathrm{Conv}}} \tag{2}$$

$$\mathrm{SNR}_{\mathrm{Passive}} = 10 \cdot \log_{10} \frac{G^2_{\mathrm{Passive}} \times P_{\mathrm{Sig}}}{kT/C_1 + kT/C_2} \tag{3}$$

where P_{Sig} is the input signal power, k is the Boltzmann constant, and T is temperature. To investigate the impact of capacitor-sizing on SNR, we constrain that the total sampling capacitor size in both cases are the same, i.e., $C_{S,\mathrm{Conv}} = C_S = C_{S,\mathrm{Passive}} = C_1 + C_2$. We then introduce a capacitor weighting factor (α), where $C_1 = \alpha C_S$, and sweep its value from 0 to 1, as illustrated in Fig. 5. The optimal point, i.e., $\mathrm{SNR}_{\mathrm{Conv}} = \mathrm{SNR}_{\mathrm{Passive}}$, is found when capacitors C_1 and C_2 are equal in size. Note that, $\pm 10\%$ mismatch between C_1 and C_2 degrades SNR by 1 dB from the peak value, as shown in Fig. 5. Here, we assume the passive gain is two in this noise analysis. In a real circuit implementation, there will be attenuation due to parasitic capacitance, which is discussed in more detail in Section III-B.

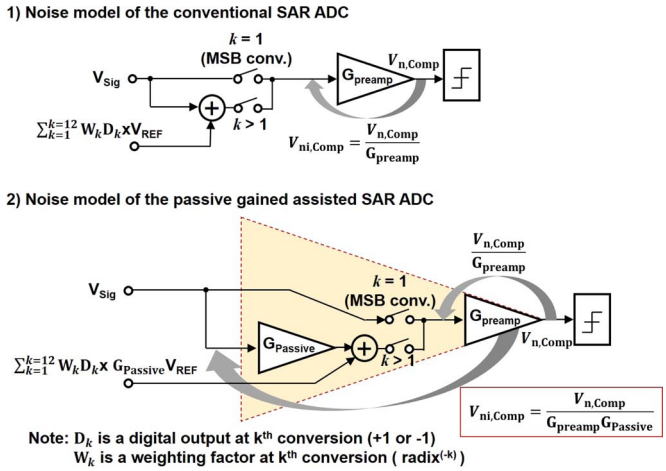


Fig. 6. Comparator noise models of the conventional and proposed passive gain assisted SAR ADC.

Regarding the comparator noise comparison before and after applying passive gain technique, the comparator noise modeling of the SAR architectures is drawn in Fig. 6. The only difference is that the reference voltage is amplified by a factor of G_{Passive} in a separate path in the passive gain case. Therefore, in terms of the overall input referred noise, the passive gain assisted SAR results in additional attenuation by a factor of G_{Passive}. Note that, in the real implementation, the amplified reference voltage is provided via external reference voltage regulator.

D. Conversion Speed

A typical N-bit SAR conversion speed is determined by input tracking time (T_{Track}), capacitor DAC (CDAC) charge redistribution time (T_{DAC}), comparator resolving time (T_{Comp}), and logic propagation delay (T_{Logic}). Assuming a single comparator is used, the ADC cycle time (T_{Cycle}) can be expressed as

$$T_{\mathrm{Cycle}} = T_{\mathrm{Track}} + \sum_{i=1}^{N} \left(T_{\mathrm{DAC}}[i] + T_{\mathrm{Comp}}[i] + T_{\mathrm{Logic}} \right). \tag{4}$$

In this subsection, we discuss the impact of T_{Comp} and T_{DAC} after applying the proposed passive gain technique. First, the required CDAC settling time at the ith SAR conversion cycle, $T_{\mathrm{DAC}}[i]$, can be determined by the effective capacitance seen from the reference voltage source in the ith conversion cycle and turn-on resistance of the switch, where we assume the index i goes in ascending order from MSB to LSB conversion cycle. Then, to compare the T_{DAC} difference between the conventional and passive gain capacitor networks, we fix the turn-on resistance, i.e., the switch size, in both cases and compare the settling time constant. Here, the series switches connected to the level-shifting capacitor (C_X) are neglected, because their turn-on resistance is order of magnitude smaller than that of the

reference switches in this prototype. Note that, in the final passive gain implementation, we replace C_2, annotated in Fig. 2, with CDAC to perform a SAR reference voltage subtraction, as will be elaborated in Section III-C. Since the passive gain approach splits the total sampling capacitor into two half-sized capacitor banks (C_1 and C_2 in Fig. 2) as discussed in the previous subsection, the settling time constant of the CDAC, i.e., C_2, can be theoretically reduced. However, due to the additional parasitic capacitance in the internal nodes of the final capacitor network implementation, the overall CDAC settling speed is comparable to the conventional case according to the post-layout simulation using 65 nm CMOS technology. Note that, since the associated parasitic capacitance is technology dependent, the settling speed of the passive gain capacitor network may improve over the conventional SAR case if SOI technology is chosen due to less parasitic capacitance.

Next, we examine the impact on comparator resolving time, i.e., $T_{\rm Comp}$. In the context of this paper, we define the comparator-resolving time as the time difference between the strobing instant and the comparator output resolved to full swing. In general, whenever the comparator input voltage is small, the comparator will take longer time to resolve. In the extreme case, it might even enter a metastable state. In order to evaluate the impact of passive gain on comparator-resolving time, a simple comparator topology composed of a pre-amplifier and strong-arm latch is used. Without considering the slewing effect, $T_{\rm Comp}$, for the ith SAR conversion cycle, can be approximated as [13]

$$T_{\rm Comp}[i] = \frac{1}{\omega_{-3\rm dB} G_{\rm latch}} \ln\left(\frac{V_{\rm FS}}{G_{\rm preamp} \cdot V_{IN,\rm Comp}[i]}\right) \quad (5)$$

where V_{IN} is a comparator input, $V_{\rm FS}$ is the full scale voltage, $\omega_{-3\rm dB}$ is the 3 dB bandwidth of the comparator, and $G_{\rm latch}$, $G_{\rm preamp}$ is the voltage gain of the regenerative latch and pre-amplifier, respectively. Since the ADC input can be close-to rail-to-rail, we will only apply a passive gain ($G_{\rm Passive}$) from (MSB-1) to LSB conversion to avoid exceeding the full swing limit at the comparator input. In order to examine the impact of the passive gain technique in asynchronous SAR, we follow a similar analytical strategy in [1], together with (5), to find out the maximum and minimum bound of $\sum_{i=1}^{N} T_{\rm Comp}[i]$, as it is input-signal dependent. We then compare the total resolving time ($T_{\rm Comp,passive}$) with that of the conventional asynchronous SAR conversion ($T_{\rm Comp,async}$) in both best and worst case, as expressed in (6) and (7), shown at the bottom of the page. As an example, we set $G_{\rm preamp} = 10$, $G_{\rm Passive} = 2$, and $N = 12$, $T_{\rm Comp,passive}/T_{\rm Comp,async}$ calculated from (6) and (7) are ~70% and ~80%, respectively

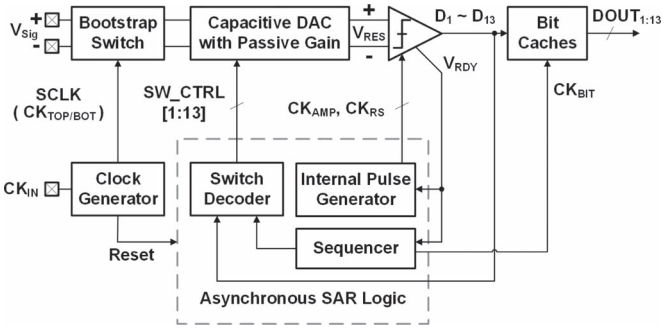


Fig. 7. Block diagram of the asynchronous SAR ADC with embedded passive gain stage.

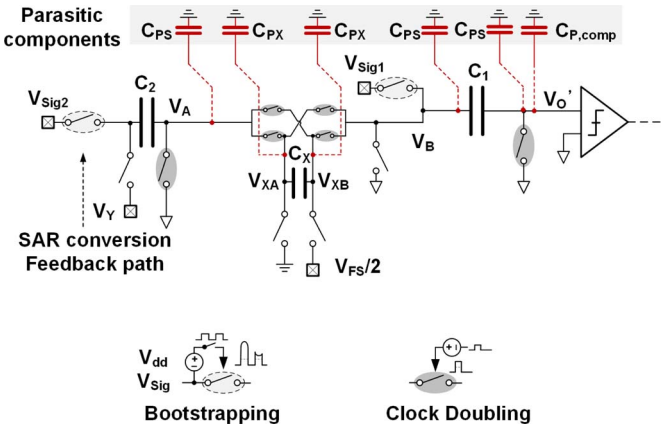


Fig. 8. Parasitic capacitors in the proposed sampling network.

III. Implementations

A. Proposed ADC Architecture

The block diagram of the proposed ADC is shown in Fig. 7. The ADC input sampling is performed by a bootstrapped switch for better linearity. The non-binary capacitor array with embedded passive gain is followed by the two-stage comparator, which also generates the data-ready signal ($V_{\rm RDY}$) needed for the asynchronous SAR operation. To alleviate the impact of the comparator metastability, a time-out circuit is employed inside $V_{\rm RDY}$ generator. The data-ready signal then drives the asynchronous SAR logic, which contains two key components. One is the internal pulse generator block, which creates reset pulses for the comparator and the CDAC switch decoder. The other is the sequencer block, which makes the multi-phase clocks strobe an array of bit caches for storing the comparator results. In the following subsections, we will elaborate the implementation and practical design considerations of the key building blocks.

B. Sampling Network

Since we use a pre-charged capacitor to perform level shifting, it inevitably adds extra noise during the pre-charging phase.

$$\left.\frac{T_{\rm Comp,passive}}{T_{\rm Comp,async}}\right|_{V_{\rm Sig}=V_{\rm FS}} = 1 - \frac{(N-1)\ln(G_{\rm Passive})}{\frac{N(N+1)}{2}\ln 2 - N\ln(G_{\rm preamp})} \quad (6)$$

$$\left.\frac{T_{\rm Comp,passive}}{T_{\rm Comp,async}}\right|_{V_{\rm Sig}=V_{\rm FS}/3} = 1 - \frac{(N-1)\ln(G_{\rm Passive})}{(N-1)\ln 3 + \frac{N^2+N+2}{2}\ln 2 - N\ln(G_{\rm preamp})}. \quad (7)$$

TABLE I
SIGNAL GAIN OF DIFFERENT PATHS IN THE SAMPLING NETWORK

Voltage gain	Description	Expression
G_{Sig1}	Signal gain from C_1	$-G_0 \times \left\{1+\frac{C_{\mathrm{PS}}}{C_2}+\left(\frac{C_2+2C_X}{C_2C_X}\right)C_{\mathrm{PX}}\right\}$
G_{Sig2}	Signal gain from C_2	$-G_0$
G_X	Gain of level shifter	$-G_0 \times \left(1+\frac{C_{\mathrm{PS}}}{C_2}\right)$
Note	$G_0 \approx \frac{C_1C_2C_X}{C_1C_2C_X+C_{\mathrm{P,comp}}(C_1C_2+C_1C_X+C_2C_X)+C_{\mathrm{PS}}(2C_1C_2+3C_1C_X+C_2C_X)+C_{\mathrm{PX}}C_1(C_2+2C_X)}$	

TABLE II
NOISE POWER BREAKDOWN

Noise source	Percentage
Quantization noise (P_Q)	72.1 %
Comparator noise ($V^2_{\mathrm{ni,Comp}}$)	18.2 %
kT/C noise	7.3 %
Switch noise ($V^2_{\mathrm{n,SW}}$)	2.4 %

Here, we assume the capacitor, C_X, resamples the reference voltage, $V_{\mathrm{FS}}/2$, whenever ADC samples the analog input. Therefore, the noise stored on C_X differs from sample to sample, and can be modeled as a Gaussian noise source with a total power of kT/C_X. In this case, an additional kT/C_X term should be included in the SNR calculation, i.e., the denominator of (3). Using the sampling capacitance value of this prototype implementation (C_1 and C_2 are equally 2 pF), we calculate SNR degradation over different C_X values. In this prototype, we choose C_X of 4 pF, which leads to ∼1-dB SNR degradation in comparison with the conventional SAR ADC architecture with sampling capacitance of 4 pF. Note that, if the leakage current of the switch is negligible over the time duration of interest, C_X only needs to sample the reference voltage once, for instance, during chip startup. In this case, the sampled noise can be treated as an ADC offset instead of extra sampling noise.

Due to the different sampling paths via C_1 and C_2, the worst case sampled voltage difference (V_{err}) can be expressed as $V_{\mathrm{err}} = (2\pi f_{\mathrm{IN}} V_{\mathrm{FS}}/2)\cdot \Delta t_{\mathrm{skew}}$, where Δt_{skew} is the aperture delay difference between the two paths, f_{IN} is the sinusoidal input frequency and V_{FS} is the full swing voltage. In order to cause V_{err} equal to half LSB of the ADC, we calculate Δt_{skew} to be 1.64 ps given the Nyquist input frequency. In this work, we have paid attentions to both layout and dummy insertion to ensure that the aperture delay difference is much less than that value.

Next, we will examine the signal attenuation due to parasitic capacitors in the proposed sampling network, as shown in Fig. 8. We derive the transfer function of each signal path from the sampled signals of C_1, C_2, and C_X to the comparator input, as they undergo slightly different parasitic capacitor networks. The gain of these signal paths are denoted as G_{Sig1} and G_{Sig2}, and G_X, and expressed as a function of those parasitic capacitances, as summarized in Table I. With the modified signal gain from each individual path, we can further modify the SNR equation, since the sampled input signal and noise goes through different paths. We derive the modified SNR in (8), where P_Q, $V^2_{\mathrm{ni,Comp}}$, $V^2_{\mathrm{n,SW}}$ are the quantization, input-referred comparator, and total switch noise appeared at the comparator input, respectively. In addition, In addition, all the different noise contributions given this particular prototype design are summarized in Table II. Note that the switch noise is dominated by the reference switches due to significantly smaller turn-on resistance of the series connected switches for level-shifting capacitor, C_X. Based on the modified SNR equation (8), shown at the bottom of the page, we choose the capacitor value (C_X) and switch sizes in the level-shifting circuit to reduce the parasitic capacitances in both the schematic and layout to ensure less than 1-dB SNR degradation. Additionally, we utilize bootstrapped switches and clock doublers with smaller switches to reduce the parasitic capacitance in the sampling network and enhance linearity, as marked in Fig. 8

C. Non-Binary Capacitor Array

Thus far, we have only considered the passive gain capacitor network with two capacitors and a level-shifting capacitor, as shown in Fig. 4(a). In the real implementation, we replace C_2 with a non-binary capacitor array that generates and subtracts the reference voltage as needed by the SAR algorithm. The complete capacitor network implementation is shown in Fig. 9. In essence, we incorporate the conventional CDAC as part of the passive gain technique for minimal overhead, and hence we refer to it as embedded passive gain technique. Note that, although the actual circuit implementation is fully differential, a single-ended CDAC operation is illustrated and analyzed in this paper for simplicity.

Depending on the pre-charged voltage across level-shifting capacitor (C_X) and ratio between the capacitors, it determines the weight of each decision bit, i.e., radix. We can express the final residue voltage (V_{RES}) after completing SAR algorithm as:

$$V_{\mathrm{RES}} = -2V_{\mathrm{Sig}} - \left(\frac{V_X}{V_{\mathrm{REF}}}D_1 + \sum_{k=2}^{13}\frac{C_{2,k-1}}{C_2}D_k\right)V_{\mathrm{REF}}. \quad (9)$$

$$\mathrm{SNR}'_{\mathrm{Passive}} = 10\log_{10}\frac{(G_{\mathrm{Sig1}}+G_{\mathrm{Sig2}})^2 \times P_{\mathrm{Sig}}}{G^2_{\mathrm{Sig1}}\frac{kT}{C_1}+G^2_{\mathrm{Sig2}}\frac{kT}{C_2}+G^2_X\frac{kT}{C_X}+V^2_{\mathrm{ni,Comp}}+V^2_{\mathrm{n,SW}}+P_Q}. \quad (8)$$

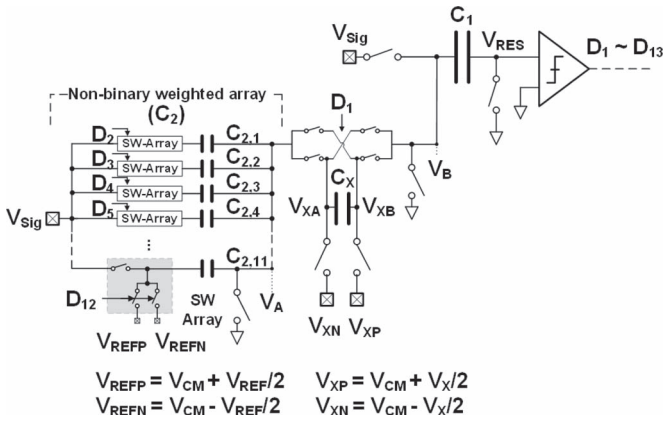


Fig. 9. Non-binary capacitor network combined with the passive gain scheme.

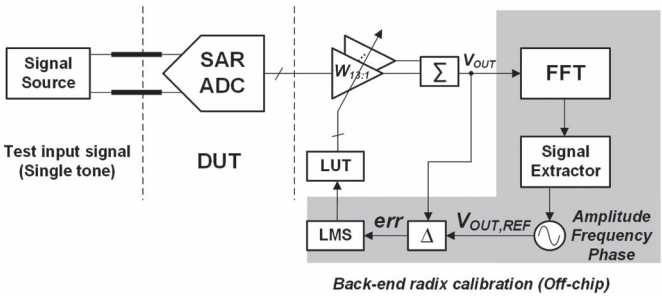


Fig. 10. Foreground radix calibration scheme.

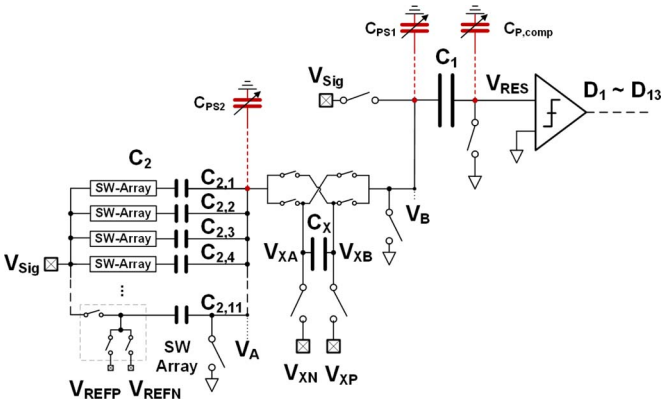


Fig. 11. Non-linear parasitic capacitors present in the capacitor network.

According to (9), the first radix is determined by the ratio between V_X and $V_{\rm REF}$, and the subsequent radix for LSBs is defined by capacitor ratio among each branch of the capacitor array. In this ADC prototype, a non-binary radix is adopted, which requires two extra redundant SAR comparison cycles. The advantages are: first, it allows incomplete DAC settling and, hence, shortens the overall conversion time [14], [15]. Second, since the passive gain will not occur until the (MSB-1) comparison, the first MSB comparison suffers from the larger comparator noise. Therefore, the decision result may be erroneous when the input signal is within the comparator' s input-referred noise range. The conversion redundancy then corrects for this comparison error using the subsequent bits. In fact, this redundancy can also correct for the potential sampling error during pre-charging reference voltage (V_X) onto capacitor (C_X), such as charge injection and clock feedthroughs. Since the error is signal independent and small due to large sized C_X, it will not affect the final ADC conversion accuracy. Even if it slightly changes the MSB radix, it can be compensated by the radix calibration. According to the SPICE simulation, the resulting error is less than 10% of the redundancy region. Furthermore, since we apply redundancy in the SAR conversion, i.e., sub-2 radix scheme, the capacitor mismatch within C_2 capacitor array is relaxed to reduce the area and layout complexity, instead of aiming at full 11-bit accuracy. In theory, the unit capacitor matching accuracy can be as relaxed as $\sim$10% if the redundancy is dedicated for compensating the capacitor mismatch [15].

To implement the non-binary radix, we use a metal-oxide-metal (MOM) capacitor array with non-integer weighted capacitances. In this prototype, we use a multi-finger capacitor structure, and the number of fingers is chosen judiciously such that the non-binary capacitor ratio can be achieved with identical finger lengths but a different number of finger segments. This improves the matching accuracy as it is close to unit-element matching.

Due to the capacitor mismatch or parasitic effects described in Section III-B, the actual radix might be slightly different from the ideal value. To mitigate those non-idealities, the actual non-binary radix can be calibrated via a post-processed least mean square (LMS) loop [1], as shown in Fig. 10. A known input signal, such as a sinusoidal wave, is injected to the ADC. The raw ADC output bits are then processed by FFT module to extract the reference waveform for LMS operation. Next, the radix values are adjusted iteratively such that the error energy between the reference waveform and reconstructed ADC output is minimized. Once the radix calibration is completed, the values are saved and used for the normal ADC operation. It is worth mentioning that most of the calibration logic, such as those resides within the gray-marked area in Fig. 10, only needs to execute once after the silicon chip and PCB test board is manufactured.

Another potential limitation of the passive gain technique is the impact of the non-linear capacitance present along the signal path inside the capacitor network implementation as shown in Fig. 11. The non-linear capacitance can result from the gate capacitance of the comparator and the diffusion capacitance of the active switches, as those parasitic capacitors are voltage-dependent. This issue particularly exacerbates when large comparators and switches are used for high-speed and high-resolution analog-to-digital conversion. The variation of the parasitic capacitance can change the signal gain, depending on the voltage across those parasitic capacitors. A similar situation occurs when using passive gain as the residue amplifier of the pipelined ADC [10]. This voltage-dependent gain will cause a distortion of the residue voltage when passing to the following pipelined stage. For the SAR ADC case, the voltage at the comparator input eventually converges toward the vicinity of the common-mode voltage, which suggests that the LSB comparisons will see a more or less constant transfer function in the end of SAR conversion, regardless of the sampled input voltage. So long as there is sufficient redundancy to compensate for the earlier decision error due to non-linear capacitance at comparator input, it will not degrade ADC linearity. However,

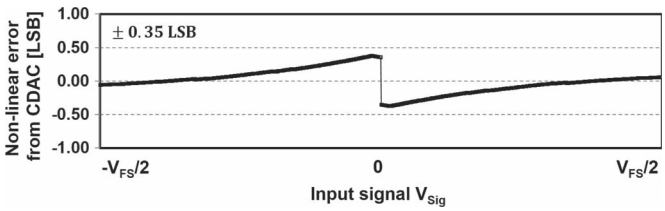
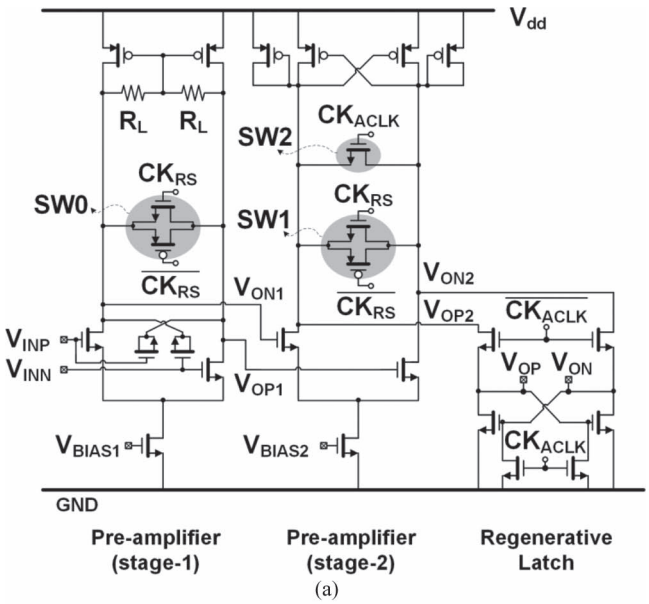


Fig. 12. Simulated INL error due to internal non-linear parasitic capacitors.

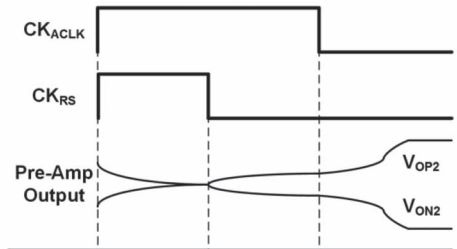
in the case of the proposed capacitor network implementation for providing passive gain, there are additional internal nodes due to capacitor stacking. Although the voltage at comparator input will still be converged toward the same common mode voltage, the internal nodes V_A and V_B as shown in Fig. 11 can be at different voltage levels in the end of SAR conversion, depending on the sampled input voltage. Therefore, the nonlinear parasitic capacitors ($C_{\rm PS1}$ and $C_{\rm PS2}$ in Fig. 11) can contribute certain signal-dependent error in the final ADC output code and cause distortion. Note that, the non-linear portion of the parasitic capacitance mainly comes from the active switches attached to V_A and V_B nodes. In this work, we utilize a clock doubler for the switch control signals in order to relax the switch size, and hence reduce the amount of the non-linear capacitance variation. To study the actual impact of the non-linear parasitic capacitance in the proposed SAR ADC architecture, SPICE simulation has been performed, and the INL curve is plotted in Fig. 12. About 4% capacitance variation has been observed against the full range of the voltage swing at V_A and V_B nodes and it causes about $\pm$0.35 LSB INL error, where LSB size is based on 11-bit accuracy as targeted in this work. This is because the parasitic capacitance at those internal nodes is dominated by the linear fringing capacitance from the MOM capacitors instead of switches. Note that, since the impact of the nonlinear parasitic capacitance is already within 11-bit accuracy, the radix calibration is not required to compensate for the non-linear effect of the parasitic capacitance.

D. Comparator

The comparator is composed of a two-stage pre-amplifier [16] and a regenerative latch, as shown in Fig. 13(a). In order to minimize the gain attenuation due to the comparator' s input capacitance, a capacitor neutralization technique is applied in the first stage by adding cross coupled MOS capacitors between the drain and the gate terminal of the input devices [17]. The first-stage pre-amplifier has the diode-connected load with a series resistor between the gate and drain terminal; the second stage uses both positive feedback and diode-connected transistors to provide a moderate gain and wide bandwidth. To mitigate the comparator memory effect while reducing the comparator-resolving time, the design utilizes one reset switch in the first stage and two reset switches in the second. A pulse generator is used to generate two clock pulses of various durations that drive those switches individually, which will be discussed in Section III-E. During the voltage equalization phase, all reset switches are turned on to provide low resistance between the two differential nodes, minimizing the memory effect from



(a)



State	Equalizing	Amplifying	Latching
SW0&1	Turn-on	Turn-off	Turn-off
SW2	Turn-on	Turn-on	Turn-off

(b)

Fig. 13. (a) Comparator implementation and (b) timing diagram of its switch control signals.

previous comparator decisions. In the signal pre-amplification phase, only the small-sized SW2 is turned on to provide a proper load resistance and to reduce the comparator-resolving time, as shown in Fig. 13(b). In this prototype, the comparator is designed to resolve half the LSB input within 250 ps, and consume around 500 μW of power. The 3 dB bandwidth, DC voltage gain, and input referred noise voltage of the comparator are around 1 GHz, 18 dB, and 160 μV, respectively.

To facilitate the asynchronous SAR logic, the data-ready signal $(V_{\rm RDY})$ generator and temporary decision data storage is required. When the comparator is in the reset and pre-amplification phase, both comparator outputs are tied to the ground via the reset switches in the regenerative latch stage. Once the latch is strobed, one of the two comparator outputs will increase toward supply rail. Therefore, we simply use a NOR gate to generate the data-ready signal, as shown in Fig. 14. Additionally, a NOR-based SR latch is used to temporarily store the decision results, allowing more timing margin for the bit caches. We intentionally designed a lowered triggering threshold $(V_{\rm trigger})$ for both the SR latch and the data-ready signal generator in order to reduce the propagation delay for high-speed operation, as shown in Fig. 14.

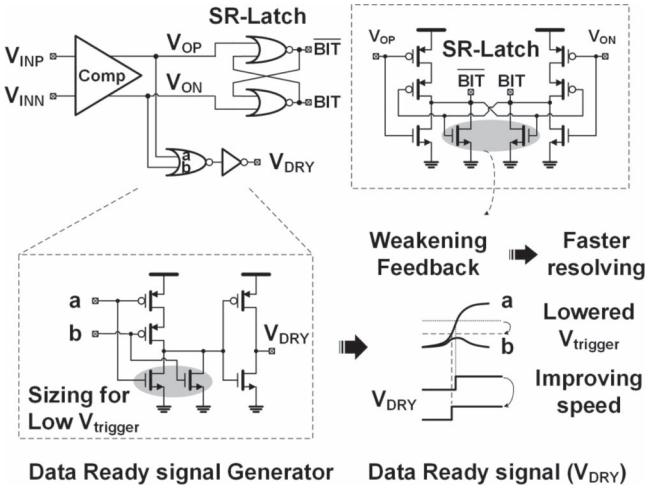


Fig. 14. Data ready signal generator and bit cache.

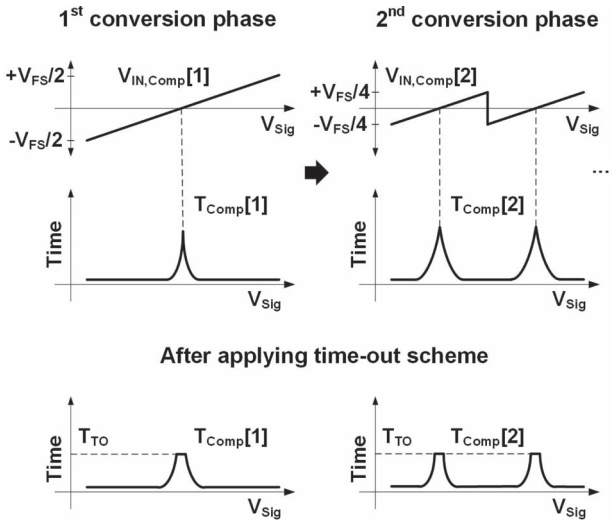


Fig. 15. Comparator conversion time reduction using time-out scheme.

E. Asynchronous Clock Generator With Time-Out Scheme

Since the propagation delay of the comparator can be excessively long when the comparator input is sufficiently small, a delay can occur in any of the SAR conversion cycles, depending on the sampled value of ADC input ($V_{\rm Sig}$), as illustrated in Fig. 15. Thanks to the redundant decision regions via the non-binary radix, decision errors in the earlier SAR conversion cycles can be corrected by later ones [18]. This suggests that the decision error within the redundant region can be tolerated and the comparison can be skipped to shorten the comparator-resolving time. Therefore, we use a time-out scheme to force skipping the comparison when the comparison time exceeds a certain threshold ($\Delta T_{\rm TO}$) determined by the required time for resolving 1-LSB input plus design margin.

The asynchronous clock generator with the time-out scheme is accomplished via a pulse generator triggered by either $V_{\rm RDY}$ from the comparator or the predetermined time-out pulse ($V_{\rm time-out}$), as shown in Fig. 16. There are two feedback paths in this pulse generator. The path that generates $V_{\rm time-out}$ utilizes an inverter chain with a total delay of $\Delta T_{\rm TO}$, which

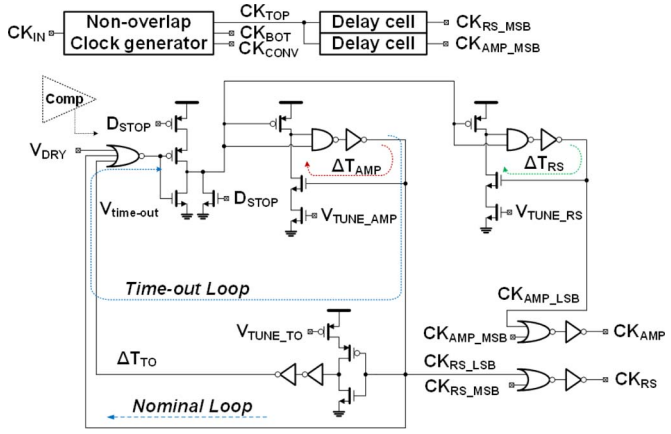


Fig. 16. Block diagram of asynchronous clock generator with the time-out circuits.

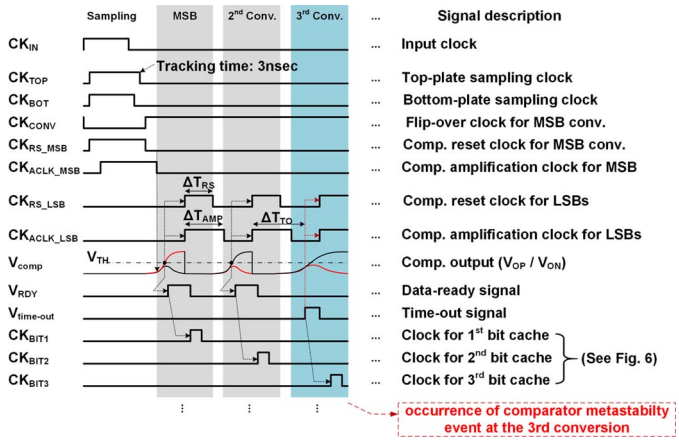


Fig. 17. Representative timing diagram of the ADC prototype with the occurrence of comparator metastability event at the third SAR conversion cycle.

determines the time-out period, and is tunable for prototyping purposes. Whenever the comparator is unable to resolve in time, $V_{\rm RDY}$ will not be flagged or will arrive later than $V_{\rm time-out}$. In this scenario, the pulse generator will still create pulses due to the 2nd feedback loop, which essentially skips the current comparison cycle and moves on to the next one.

Once input clock signal ($\rm CK_{IN}$) is injected from an external source with 3 ns allocated tracking time, the clock generator block creates all the internal clocks required in the asynchronous SAR conversions during the remaining ADC cycle time. Generated clock signals, such as the two pulses with different durations, namely $\Delta T_{\rm RS}$ and $\Delta T_{\rm AMP}$, used to drive the reset switches [SW1 and SW2, labeled in Fig. 13(a)] of the comparator and the initiating clock pulses ($\rm CK_{RS\_MSB}$ and $\rm CK_{ACLK\_MSB}$) to kickstart the asynchronous SAR conversion, as shown in Fig. 17. In this representative timing diagram, we show an event that the third conversion cycle takes longer-than-expected to resolve, and show how the $V_{\rm time-out}$ pulse helps to advance pulse generation, completing SAR conversion within the allocated conversion time.

IV. Measurement Results

A prototype chip was implemented in a single-poly nine-metal (1P9M) 65 nm CMOS process, and occupies an active die

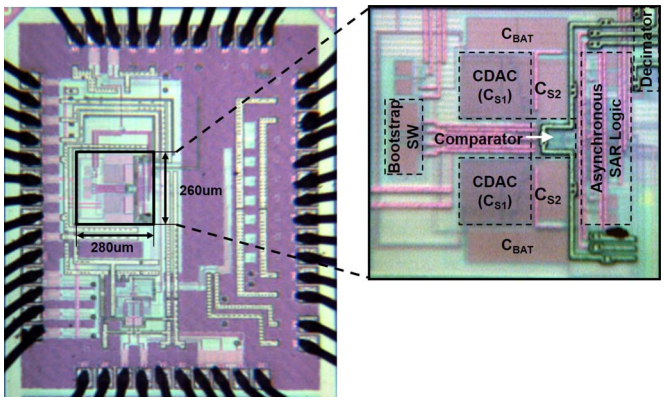


Fig. 18. Die micrograph.

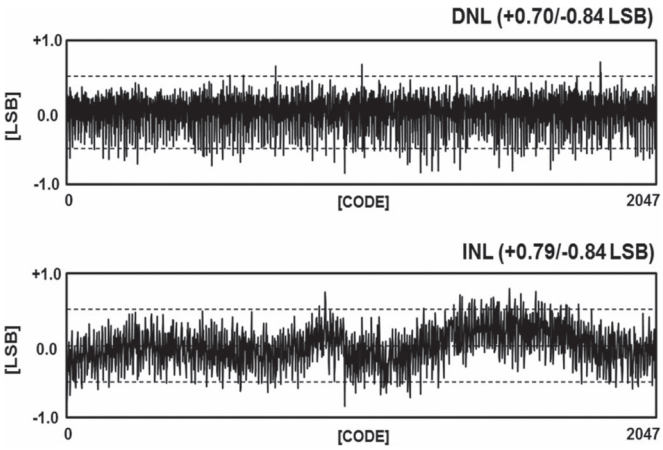


Fig. 19. Measured DNL (top) and INL (bottom) plot.

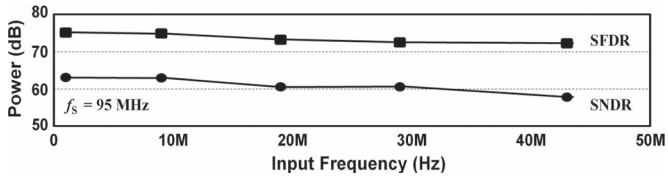


Fig. 20. Measured dynamic performance.

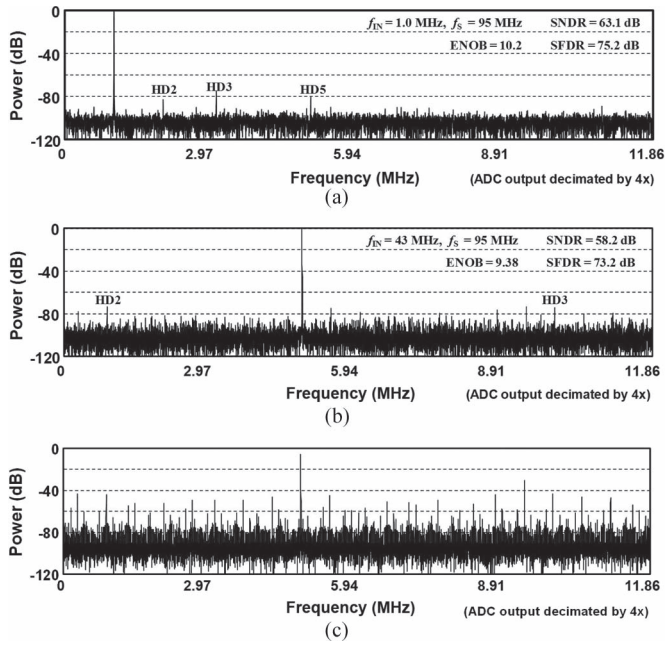


Fig. 21. Measured ADC output spectrum for sinusoidal input at (a) low frequency; (b) Nyquist frequency with and (c) without radix calibration.

area of 0.07 mm^2 (see Fig. 18). The ADC consumes 1.36-mW (excluding I/O pad power consumptions) through a 1.1 V supply, while the analog and digital sections dissipate 0.55 mW and 0.81 mW, individually. Within the analog power dissipation, the comparator and CDAC switching consumes 400 μW, and 150 μW, respectively. Note that, all the reference voltage buffers, including $V_{\rm CM}$ and $V_{\rm REF}$, are implemented off-chip with on-chip bypass capacitors occupied additional $\sim$0.03 mm^2 of die area. The reported power consumption excludes the power consumption of those off-chip voltage buffers, ADC output drivers and I/O pads. Although the radix calibration logic is performed via software, we translate the logic into RTL and conduct trial synthesis using digital standard cell library in 65 nm CMOS. The estimated active area and power dissipations are 300 μm^2 and 200 μW, respectively. To test the prototype, a signal source generator is first passed through a passive 6th order band-pass filter, followed by a balun that converts the single-ended signal into differential 1.6 V_{pp} signals. As shown in Fig. 19, the measured differential non-linearity (DNL) and integral non-linearity (INL) were within +0.70/$-$0.84 LSB and +0.79/$-$0.84 LSB, respectively. As discussed in Section III-C, the non-linear parasitic capacitance can contribute additional INL error, and the measured INL pattern is indeed similar to the SPICE simulated one as shown in Fig. 12. The measured dynamic performance of the ADC at a sampling rate of 95-MS/s is illustrated in Fig. 20. In order to reduce the I/O throughput, the digital output codes are decimated by four times on chip. In the ADC dynamic performance versus the input frequency plot, the SNDR achieves 63.1 dB for 1.0-MHz input frequency and remains above 58.2 dB up to the Nyquist input frequency. The corresponding FFT snapshots are shown in Fig. 21(a) and (b). Note that both FFT plots assume that the radix calibration has been applied, using the algorithm discussed in Section III-C. On the other hand, the FFT plot in Fig. 21(c) uses the nominal non-binary radix for signal reconstruct 30 dB difference in SFDR and SNDR compared to the one with radix calibration [Fig. 21(b)]. This performance difference is close to our expectation based on simulations that consider both capacitor mismatch and parasitics effects. Those effects can change the non-binary radix value, leading to performance degradations. Since the radix calibration scheme iteratively looks for the actual non-binary radix, it improves the fidelity of the reconstructed signal as observed in both simulation and measurement.

In terms of the achieved power efficiency, we utilize the commonly used figure of merit (FOM), defined as Power$/f_S \cdot 2^{\rm ENOB}$. In this prototype, FOM achieves a 12 fJ/conversion-step for a 1-MHz input, and a 21.5 fJ/conversion-step at the Nyquist input frequency with 95-MS/s due to increased noise floor while achieving similar SFDR performances. If the estimated power dissipation for the radix calibration logic

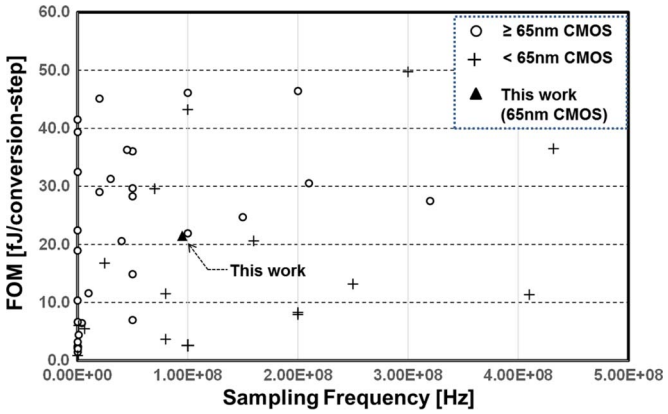


Fig. 22. Measured FOM comparison with ADCs presented at ISSCC (1997–2016) and VLSI (1997–2015) [19].

TABLE III
ADC PERFORMANCE COMPARISON (10 > ENOB AND 90 MS/s)

	This work	[20]	[21]	[22]
Technology	65nm CMOS	90nm CMOS	65nm CMOS	28nm CMOS
ADC Architecture	Passive-Gain SAR ADC	Pipelined ADC	Noise-Shape SAR ADC	SAR-assisted Slope ADC
Speed (MS/s)	95	100	90	100
Supply (V)	1.1	1.1	1.2	0.9
Input Swing (V_{pp})	1.6	2.0	N/A	1.6
SFDR (dB)	75.2	74	72	75.4
SNDR (dB)	63.1	63.2	62	64.43
Power (mW)	1.36	0.8	6.2	0.35
Area (mm^2)	0.073	0.32	0.03	0.0042
FOM (fJ/conv.-step)	21.5	52.7	35.8	2.63

were included in the total power consumption, FOM would be degraded by 15%. Fig. 22 compares the FOM with $>$ 50 MS/s and $>$ 50 dB SNDR ADCs presented at ISSCC (1997–2016) and VLSI (1997–2015) [19]. The measured performance summary and comparison with the state-of-the-art ADCs with similar specification are demonstrated in Table III. Comparing these results with the performance of state-of-the-art ADCs implemented in the same CMOS technology nodes, our proposed passive gain asynchronous SAR ADC achieves the lowest FOM. Given the technology-scaling benefits and mostly digital nature of SAR ADCs, we expect the power efficiency of the proposed ADC architecture to further improve with more advanced technology nodes. In fact, it is noteworthy that the FOM achieved by this prototype is better than some of the state-of-the-art SAR ADCs (see Fig. 22) in more advanced nodes ($<$ 65 nm), which indicates the potential of the proposed ADC architecture.

V. CONCLUSION

This paper presents an asynchronous SAR ADC architecture with an embedded passive gain technique that is fully integrated into the proposed sampling network. The architecture has been shown to significantly relax the noise and power requirement of the comparator while also improving the overall conversion speed. This is crucial in forging a path towards higher speeds, but lower power consumption in analog-to-digital conversion for the resolution of around 11 bit, which is mainly constrained by the non-linear parasitic capacitance in the capacitor network. The achievable resolution can be further improved for the more advanced technologies that provide better active switches with less parasitics. Furthermore, the proposed time-out mechanism facilitates the completion of the SAR conversion under the event of the comparator metastability. Finally, we expect the proposed ADC architecture to continue improving in terms of power efficiency and speed with more advanced technology nodes due to the mostly digital implementation [1].

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Jae-Won Nam (S'13) received the B.S. and M.S. degrees in information and communications engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2006 and 2008, respectively. Since February 2008, he has been with Electronics and Telecommunications Research Institute (ETRI), Daejeon, as a Researcher. Currently, he is working toward the Ph.D. degree in electrical engineering at the University of Southern California (USC), Los Angeles, CA, USA. To conduct the research, he obtained a Ph.D. Fellowship from a Viterbi-USC Graduate School of Engineering.

His research interests include designing low-power high-speed high-resolution analog-to-digital data converters, and high-speed I/O interface circuits. Mr. Nam was the corecipient of the Silver Award from the 10th Korea Intellectual Property Office (KIPO) circuit design contest in 2009.

Mike Shuo-Wei Chen (S'00–M'06) received the B.S. degree from National Taiwan University, Taipei, in 1998 and the M.S. and Ph.D. degrees from University of California, Berkeley, CA, USA, in 2002 and 2006, all in electrical engineering. He is currently an Assistant Professor in Electrical Engineering Department at University of Southern California, Los Angeles, CA, USA, and holds Colleen and Roberto Padovani Early Career Chair position.

From 2001 to 2006, he was a Graduate Research Assistant at Berkeley Wireless Research Center, working on mixed-signal circuits, ultra-wideband, digital baseband, and ASIC implementation. During that time, he proposed and demonstrated the asynchronous SAR ADC architecture, which has been adopted for low-power high-speed analog-to-digital conversion in industry. Since 2006, he has been a member of Analog IC Group at Atheros Communications (now Qualcomm-Atheros), working on mixed-signal and RF circuits for various wireless communication products. After joining University of Southern California, he leads an analog mixed-signal circuit group, focusing on high-speed low-power data converters, bio-inspired electronics, RF frequency synthesizers, and DSP-enabled analog circuits and systems.

Dr. Chen was the recipient of NSF Faculty Early Career Development (CAREER) Award and DARPA Young Faculty Award (YFA) in 2014, Analog Devices Outstanding Student Award for recognition in IC design in 2006, and UC Regents Fellowship at Berkeley in 2000. He also achieved an honorable mention in the Asian Pacic Mathematics Olympiad, 1994.