

Soft-Switched Interleaved Boost Converters for High Step-Up and High-Power Applications

Sungsik Park, Yohan Park, Sewan Choi, Woojin Choi, and Kyo-Beum Lee

Abstract—This paper proposes a generalized scheme of new soft-switching interleaved boost converters that is suitable for high step-up and high-power applications. The proposed converter is configured with proper numbers of series and parallel connected basic cells in order to fulfill the required output voltage and power levels, respectively. This leads to flexibility in device selection resulting in high component availability and easy thermal distribution. Design examples of determining the optimum circuit configuration for given output voltage and power level are presented. Experimental results from a 1.5-kW prototype are provided to validate the proposed concept.

Index Terms—Continuous conduction mode (CCM), high step-up, high voltage gain, multiphase, nonisolated, soft-switched.

I. INTRODUCTION

RECENTLY, high step-up dc–dc converters that do not require isolation have been used in many applications, such as dc back-up energy systems for uninterruptible power system, renewable energy systems, fuel cell systems, and hybrid electric vehicles. Generally, the high step-up dc–dc converter for these applications has the following requirements.

- 1) High step-up voltage gain. Sometimes the voltage gain could be more than 10.
- 2) High current handling capability.
- 3) High efficiency at a desired level of volume and weight.
- 4) Low-input current ripple.

In order to provide high output voltage, the classical boost converter should operate at extremely duty cycle, and then the rectifier diode must sustain a short pulse current with high amplitude. This results in severe reverse recovery as well as high EMI problems. Using an extreme duty cycle may also lead to poor dynamic responses to line and load variations. Moreover, in the high step-up dc–dc converter the input current is usually large,

and hence low-voltage-rated MOSFETs with small $R_{DS(ON)}$ are necessary in order to reduce the dominating conduction loss. However, the switch in the classical boost converter should sustain high output voltage as well, and therefore, the device selection is faced with a contradiction.

A lot of high step-up dc–dc converter topologies have been presented to overcome the aforementioned problem. Converters with coupled inductors [1]–[5] can provide high output voltage without extreme duty cycle and yet reduce the switch voltage stress. The reverse recovery problem associated with rectifier diode is also alleviated. However, in [1] the efficiency is degraded due to the losses associated with leakage energy of the coupled inductor. In [2] and [3] the leakage energy of the coupled inductor is effectively recycled. However, the converter presented in [2] has high resonating currents through both the magnetizing inductance and the power switch. In the integrated boost-flyback step-up converter [3] the turn ratio of the coupling inductor should be increased as the required output voltage increases, which makes the flyback subconverter handle higher output power leading to large power loss in the flyback converter diode. In fact, these topologies incorporating the flyback transformer [2], [3] is not suitable for high step-up and high-power applications since the capacity of the magnetic core should substantially be increased as the required output power is increased. A solution to these problems has been presented at the expense of increased number of components [4], [5]. Also, most of the high step-up converters with the coupling inductor has large input current ripple due to the operation of the coupling inductor.

High step-up dc–dc converters based on the switched-capacitor circuit [6]–[11] have been presented for low power applications. The switched-capacitor converter [6], [7] does not employ any inductor making it feasible to achieve high power density. However, the efficiency could be reduced to allow output voltage regulation. In [8] the switched capacitor circuit is integrated within a boost converter to achieve output voltage regulation without decreasing efficiency, but the numbers of components are high, and input current ripple is considerable. Single-switch topologies based on the switched-capacitor circuit [9], [10] and switched-capacitor/switched-inductor hybrid structure [11] exhibit continuous input current and reduced switch and diode voltage stresses. The major drawback of these topologies is that attainable voltage gains and power levels without degrading system performances are restricted. The effective way of extending these schemes to achieve higher voltage gain or power level has not been discussed.

Meantime, it has been demonstrated in many high current applications that the interleaved technique provides advantages

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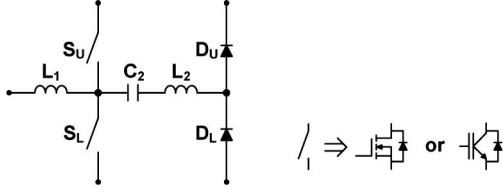


Fig. 1. Basic cell of the proposed interleaved high step-up converter.

of handling high current and reducing the passive component size [12], [13]. A cascade structure of the interleaved boost converter [14] can provide a fairly high output voltage without the extreme duty cycle, but the switch and diode voltage stresses at the second stage is equal to output voltage. High gain interleaved converters that connect the two converters in parallel at the input and series at the output [15], [16] achieve higher output voltage with reduced switch and diode voltage stresses, but attainable voltage gain is not very high. Hard switching operation also degrades the efficiency and limits the switching frequency.

Soft switching techniques should also be employed in order to achieve high efficiency at a desired level of volume and weight. They are more preferable if required power level gets higher. Most of the aforementioned high step-up dc–dc converters are hard switched and not suitable for high-efficiency and high-power applications. A soft-switching interleaved boost converter with coupling inductor [17] exhibits high voltage gain and zero volt switch (ZVS) and zero current switch (ZCS) operations of switches. However, this topology still has considerable input current ripple and high number of component. Improved high step-up converter topologies [18]–[20] have been presented to provide interleaving, soft switching, and extendibility.

Therefore, preferable features of the high step-up dc–dc converter for high-efficiency, high-power applications are soft-switching, interleaving, low-input current ripple, reduced number of components, low component ratings, extendibility, and low volume and weight.

In this paper, a new interleaved high step-up dc–dc converter for high-efficiency, high-power applications are presented. The proposed converter has the following advantages.

- 1) Reduced voltage stresses of switches and diodes.
- 2) ZVS turn-on of the switches and ZCS turn-off of the diodes.
- 3) Low-input current ripple due to the interleaved structure.
- 4) Reduced energy volumes of most passive components.
- 5) Extendibility to desired voltage gain and power level.

The operating principles along with a design example of the proposed converter are described. Experimental results from a 1.5-kW prototype are also provided to validate the proposed concept.

II. PROPOSED INTERLEAVED HIGH STEP-UP CONVERTER

A. Generalized Multiphase DC–DC Converter

Fig. 1 shows a basic cell used as a building block to build the proposed high step-up converter. The basic cell consists of an input filter inductor, a switch leg and diode leg, and an auxiliary

inductor, and capacitor. Fig. 2 shows the generalized circuit of the proposed converter with N and P , where N is the number of output series-connected basic cell and P is the number of output parallel-connected basic cell, respectively, meaning that there exist totally $N \cdot P$ basic cells. The diode leg of n th basic cell is connected to the output capacitor $C_{3,n}$, where $n = 1, 2, 3, \dots, N$ and $p = 1, 2, 3, \dots, P$, and output capacitors $C_{3,1}$ to $C_{3,N}$ are connected in series on top of output capacitor C_1 to form the output voltage. That is, “ N ” could be increased to get higher output voltage while “ P ” could be increased to get higher output power. It should be noted that the voltage rating of switches can be reduced by increasing N and the current rating of them can be reduced by increasing N or P . Also, the voltage and current ratings of diodes can be reduced by increasing N and P , respectively. Therefore, optimum devices in the sense of cost and availability can be selected by proper choice of N and P .

The interleaving technique can be applied to reduce the size of input filter inductors and output filter capacitors. Therefore, “ N ” and “ P ” can properly be chosen according to given output voltage and power level. This could give flexibility in device selection resulting in optimized design even under harsh design specifications.

B. Voltage Conversion Ratio

The key waveforms of the generalized high step-up dc–dc converter are shown in Fig. 3. The interleaved asymmetrical pulse width modulation switching is applied, that is, D and $1-D$ are the duty cycles of lower and upper switches of a leg, respectively, and each leg is interleaved with a phase difference of $2\pi/(N \cdot P)$.

To obtain the voltage gain of the proposed converter, it is assumed that the voltages across C_1 , $C_{2,np}$, and $C_{3,n}$ are constant during the switching period of T_S . The output voltage is given by

$$V_o = V_{C1} + V_{C3,1} + \dots + V_{C3,N} \quad (1)$$

or

$$V_o = \frac{N+1}{1-D_{\text{eff}}} V_i \quad (2)$$

where the effective duty D_{eff} is defined by

$$D_{\text{eff}} = D - \Delta D \quad (3)$$

where $\Delta D = D_2 + D_1$ is the duty loss. The output voltage can also be expressed as

$$V_o = \frac{N+1}{1-D} V_i - \Delta V \quad (4)$$

where ΔV is the voltage drop caused by the duty loss ΔD . From (2), (3), and (4) the voltage drop ΔV can be obtained by

$$\Delta V = \frac{\Delta D \cdot V_i \cdot (N+1)}{(1-D)(1-D+\Delta D)}. \quad (5)$$

According to volt-second balance principle on L_2 , the capacitor voltage $V_{C2,np}$ can be obtained by

$$V_{C2,np} = V_{C1} + V_{C3,n}(1-D-\Delta D) \quad (6)$$

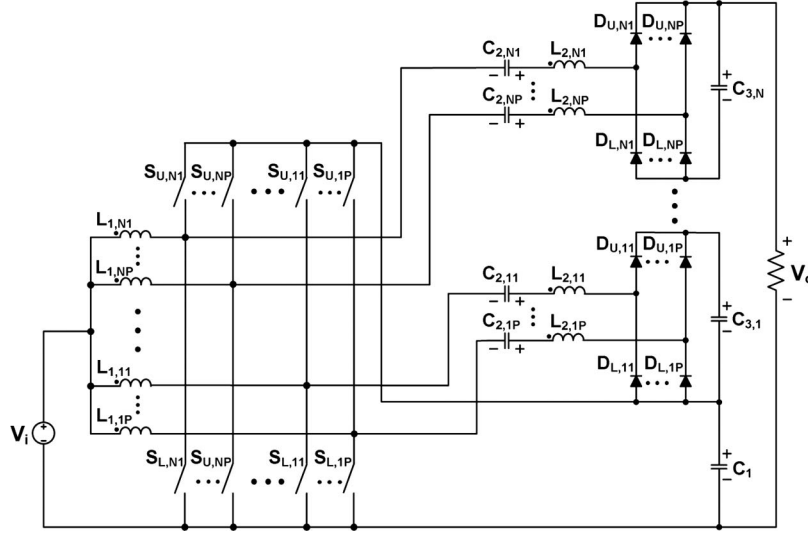


Fig. 2. Generalized circuit topology of the proposed interleaved high step-up dc-dc converter (N is the number of output series-connected basic cell, and P is the number of the output parallel-connected basic cell).

where V_{C1} and $V_{C3,n}$ can be expressed as

$$V_{C1} = \frac{1}{1-D} V_i \quad (7)$$

$$V_{C3,n} = \frac{1}{1-D} V_i - \frac{\Delta V}{N}. \quad (8)$$

In the mean time, since the output load current equals the average current of $D_{U,np}$ and $D_{L,np}$ the following equations can be derived:

$$I_{DU,av} = I_{DL,av} = \frac{V_o}{P \cdot R_o}. \quad (9)$$

Then, since the operating duty cycle D is much larger than the duty loss ΔD in most of the operating region, positive and negative peak values $I_{L2,+pk}$ and $I_{L2,-pk}$ of the inductor current I_{L2} can be approximated by

$$I_{L2,+pk} \approx \frac{2 \cdot V_o}{(1-D) \cdot P \cdot R_o} \quad (10)$$

$$I_{L2,-pk} \approx \frac{2 \cdot V_o}{D \cdot P \cdot R_o}. \quad (11)$$

These peak values decrease as P increases, but they do not depend on N . Also, by applying volt-second principle to inductor L_2 during $D_1 T$ and $D_2 T$, D_1 and D_2 can be obtained by

$$D_1 = \frac{I_{L2,+pk} \cdot L_2}{V_{C1} \cdot T_s} \quad (12)$$

$$D_2 = \frac{I_{L2,-pk} \cdot L_2}{V_{C1} \cdot T_s}. \quad (13)$$

From (2), (3), (10)–(13), the I–O voltage gain of the proposed converter can be obtained by

$$\frac{V_o}{V_i} = \frac{D\alpha - \alpha + \sqrt{\alpha(D^2\alpha - 2D\alpha + \alpha + 2\beta + 2\beta N)}}{\beta} \quad (14)$$

where $\alpha = DR_o P$ and $\beta = 4 f_s L_2$.

Using (14) the effective voltage gain of the proposed converter is plotted as shown in Fig. 4. Even though there is a slight drop off the ideal voltage gain which is caused by duty loss ΔD , the effective voltage gain of the proposed converter is almost $N + 1$ times compared to that of the conventional boost converter. This is a very desirable feature in high step-up applications since reduced duty ratio leads to reduced current stresses on the components, resulting in increased efficiency.

The duty loss ΔD is drawn as a function of the output power in Fig. 5. The duty loss increases linearly as the output power increases. Also, we can see that the larger the inductance value is the larger the duty loss is. The duty loss can be reduced by choosing smaller inductance L_2 , but this reduces ZVS range of lower switch S_L , as shown in (16). Therefore, inductance L_2 should be properly chosen considering a tradeoff of switching loss and voltage gain.

C. ZVS Characteristic for Main Switch

ZVS of the upper and lower switches of each leg depends on the difference of the filter inductor current i_{L1} and auxiliary inductor current i_{L2} as shown in Fig. 2. The ZVS current for lower (upper) switch, $I_{SL,ZVS}$ ($I_{SU,ZVS}$), is the positive (negative) peak of $i_{L1} - i_{L2}$ when the upper (lower) switch is turned off. To ensure the ZVS turn on of upper switch S_U , the following condition should be satisfied:

$$\frac{1}{2} L_2 I_{SU,ZVS}^2 > \frac{1}{2} (C_{os1} + C_{os2}) \left(\frac{V_i}{1-D} \right)^2 \quad (15)$$

where C_{os1} and C_{os2} are the output capacitances of lower switch S_L and upper switch S_U , respectively. In fact, the condition of (15) can easily be satisfied, and ZVS of upper switch S_U can be achieved over the whole load range. To ensure the ZVS turn on of lower switch S_L , the following condition should be

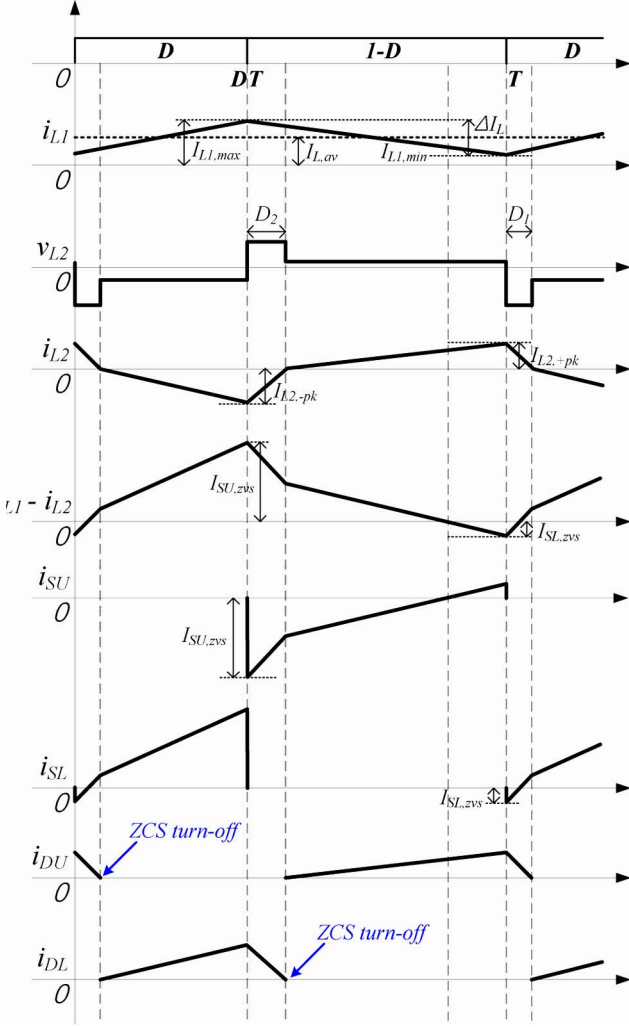


Fig. 3. Key waveforms associated with the n th cell of the generalized high step-up dc-dc converter.

satisfied:

$$\frac{1}{2}L_2I_{SL,ZVS}^2 > \frac{1}{2}(C_{os1} + C_{os2})\left(\frac{V_i}{1-D}\right)^2. \quad (16)$$

Equation (16) may not be satisfied under the conditions of small auxiliary inductance, large input filter inductance, and/or light load. Increasing auxiliary inductance to enlarge the ZVS region makes the duty loss ΔD large [21]. Alternatively, in order to enlarge the ZVS region, the input inductance can be decreased so that $I_{SL,ZVS}$ can be increased. However, decreasing the input filter inductance increases the current rating of the power devices, and therefore, the input filter inductance should be properly chosen considering a tradeoff between the ZVS region and the device current ratings. Therefore, ZVS for lower switch S_L can be achieved more easily with smaller value of L_1 and/or larger value of L_2 at the cost of the large current ripple. A tradeoff of switching loss and conduction loss should be considered. The quasi-square-wave ZVS turn-off can be achieved

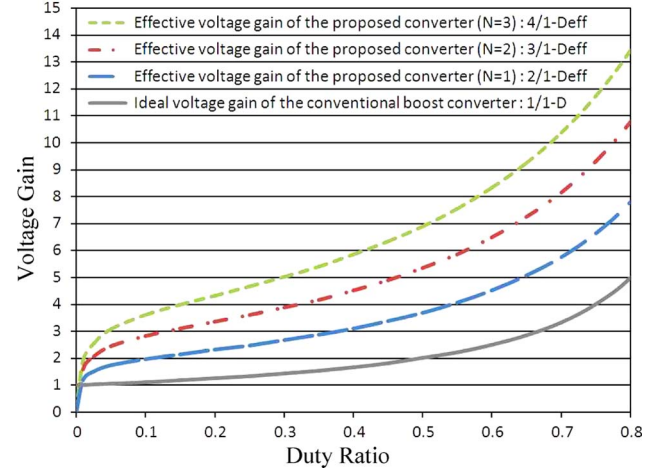


Fig. 4. Voltage gain as a function of the duty ratio ($P = 1$, $L_2 = 4 \mu\text{H}$, $f_s = 70 \text{ kHz}$, $P_o = 1.5 \text{ kW}$).

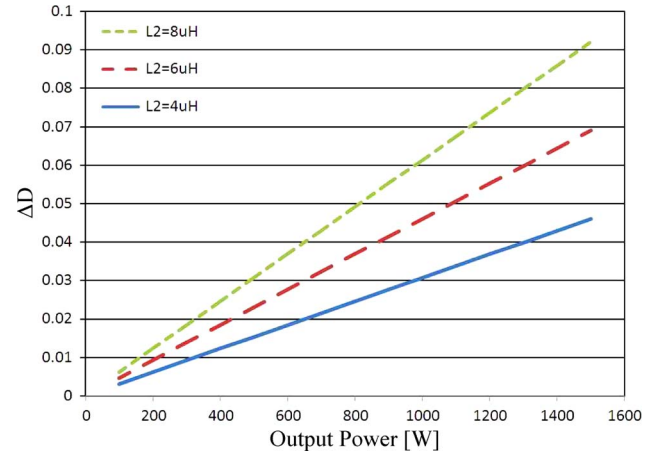


Fig. 5. Duty loss as a function of the output power ($N = 1$, $P = 1$, $f_s = 70 \text{ kHz}$, $D = 0.6$).

by adding a small capacitor across the switches even though this may somewhat degrade the ZVS turn-on performance.

III. DESIGN EXAMPLE

In this section, two design examples are presented to illustrate how to determine optimum values of N and P for given two specifications: 1) high step-up application and 2) higher power application.

A. High Step-Up Application

An example specification for the high step-up application is given as follows:

$$P_o = 1.5 \text{ kW}, \quad V_o = 380 \text{ V}, \quad V_i = 40 \text{ V}, \\ L_2 = 4 \mu\text{H}, \quad f_s = 70 \text{ kHz}, \quad \Delta I_s = 10\%, \quad \Delta V_o = 3\%.$$

First, the effective and actual duty cycles that affect the voltage ratings of switches, diodes, and capacitors are calculated for

TABLE I
COMPONENT VOLTAGE RATINGS ($P_o = 1.5$ kW, $V_i = 40$ V, $V_o = 380$ V)

		N=1	N=2	N=3
Duty	D (D_{eff})	0.82 (0.79)	0.71 (0.69)	0.62 (0.58)
Switches, C_1	V_{pk}	220V	150V	112V
Diodes, C_3	V_{pk}	162V	115V	90V
C_2	V_{pk}	213V	260V	285V

TABLE II
COMPONENT CURRENT RATINGS ($P_o = 1.5$ kW, $V_i = 40$ V, $V_o = 380$ V, $N = 2$)

		P=1	P=2	P=3
Switches	I_{rms}	21A	10.8A	8.3A
Diodes	I_{avr}	4.1A	2A	1.4A
C_2	I_{rms}	9.8A	4.4A	3.4A
C_1	I_{rms}	12A	5A	4A

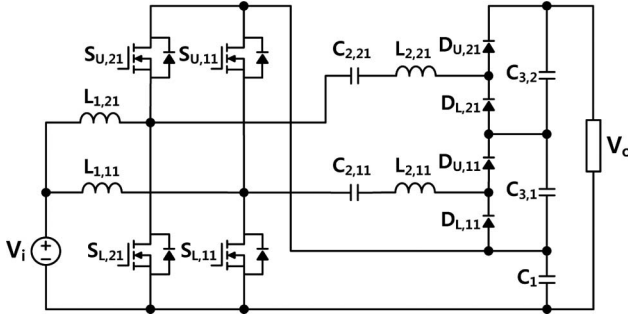


Fig. 6. Circuit diagram of the proposed converter with $N = 2$ and $P = 1$ ($P_o = 1.5$ kW, $V_i = 40$ V, $V_o = 380$ V).

several cases of N , and the resultant component voltage ratings are listed in Table I. Note that the voltage gain of 9.5 is achieved using the actual duty cycles of 0.82, 0.71, and 0.62 with $N = 1$, $N = 2$, and $N = 3$, respectively. It should be noted that choosing higher value of N reduces the required duty cycle, resulting in reduced voltage rating of the component. However, this in turn increases the numbers of components. Therefore, N is chosen to be as low as possible if voltage ratings of the components are within some limit so that proper components can be selected from the manufacture. In this example, N is chosen to be 2 so that MOSFETs with voltage rating of less than 200 V and Schottky diodes with voltage rating of 150 V can be used. Now, with $N = 2$ the current ratings of the components can be calculated for several cases of P , as shown in Table II. In this example, $P = 1$ is chosen since the current ratings are within proper limits. The circuit topology with $N = 2$ and $P = 1$ is shown in Fig. 6.

Fig. 7 shows key waveforms of the proposed converter with $N = 2$ and $P = 1$. The two switch legs are interleaved with 180° phase shift, and the upper and lower switches of each leg are operated with asymmetrical complementary switching to regulate the output voltage. The converter has eight operating

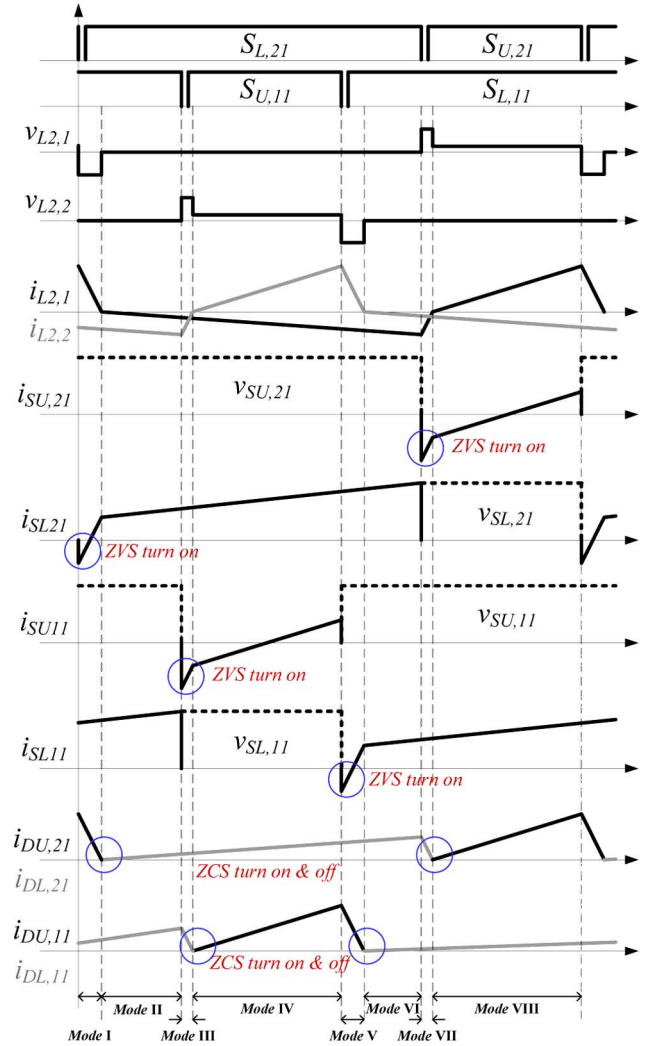


Fig. 7. Key waveforms of the proposed converter with $N = 2$ and $P = 1$.

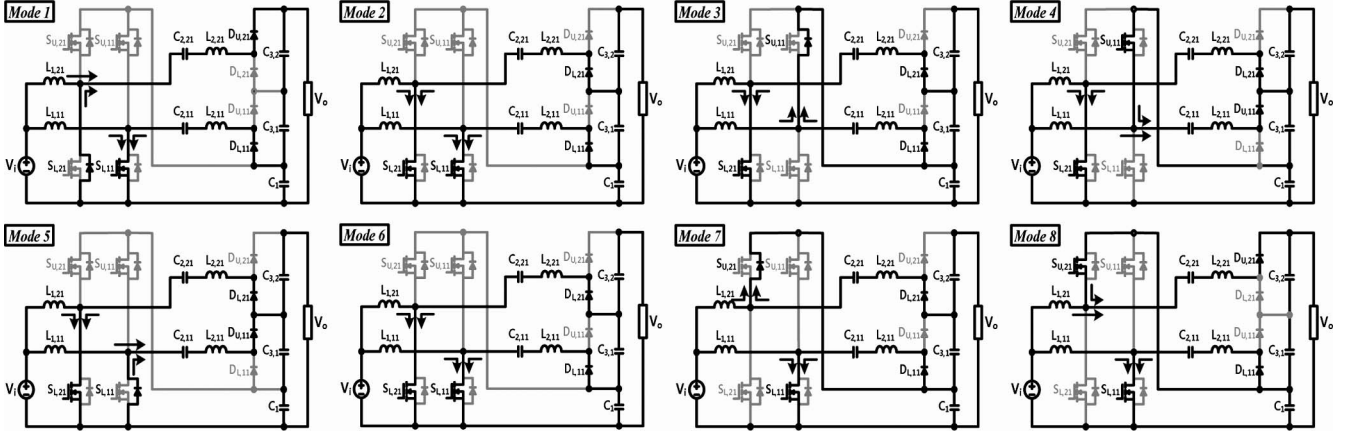
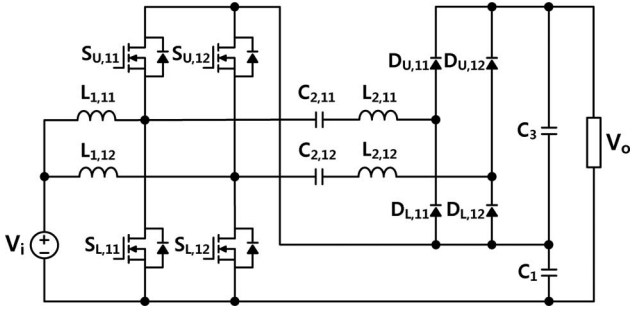
modes within each operating cycle. Fig. 8 shows the equivalent circuits of the eight operating modes.

B. Higher Power Application

An example specification for higher power application is given as follows:

$$P_o = 10 \text{ kW}, \quad V_o = 200 \text{ V}, \quad V_i = 40 \text{ V}, \\ L_2 = 4 \mu\text{H}, \quad f_s = 50 \text{ kHz}, \quad \Delta I_s = 10\%, \quad \Delta V_o = 3\%.$$

The effective and actual duty cycle are calculated for several cases of N , and the component voltage ratings are listed in Table III. Note that the voltage gain of 5 is achieved using the actual duty cycles of 0.65 and 0.48 with $N = 1$ and $N = 2$, respectively. In this example, N is chosen to be 1 since MOSFETs with voltage rating of less than 150 V and Schottky diodes with voltage rating of 120 V can be used, respectively. Now, with $N = 1$ the current ratings of the components can be calculated for several cases of P , as shown in Table II-B. In the example $P = 2$ is chosen, and the circuit topology with $N = 1$ and $P = 2$ is shown in Fig. 9.

Fig. 8. Operation modes of the proposed converter with $N = 2$ and $P = 1$.Fig. 9. Circuit diagram of the proposed converter with $N = 1$ and $P = 2$ ($P_o = 10$ kW, $V_i = 40$ V, $V_o = 200$ V).TABLE III
COMPONENT VOLTAGE RATINGS ($P_o = 10$ kW, $V_i = 40$ V, $V_o = 200$ V)

		N=1	N=2	N=3
Duty	D (D_{eff})	0.65 (0.6)	0.48 (0.4)	0.36 (0.2)
Switches, C_1	V_{pk}	115V	90V	65V
Diodes, C_3	V_{pk}	95V	80V	64V
C_2	V_{pk}	112V	140V	158V

From the aforementioned two design examples, it can be seen that flexibility in device selection that can be achieved by choosing proper N and P may result in a viable and low cost solution even under harsh design specifications.

C. Performance Comparison

In this section, the proposed converter is compared to the couple inductor converter [17] and the multiplier cell converters [20] that are high step-up interleaved soft-switching dc-dc converters recently proposed. The comparison has been performed in terms of utilization ratio of switching devices and energy volume of passive components, etc., and the results are listed in Table V. The switch utilization ratio of the proposed converter is comparatively small, which is a disadvantage of the proposed converter. Meanwhile, the diode utilization ratio of the proposed converter is significantly large compared to the conventional ones. Also, the voltage rating of the diode is small so

TABLE IV
COMPONENT CURRENT RATINGS ($P_o = 10$ kW, $V_i = 40$ V, $V_o = 200$ V, $N = 1$)

		P=1	P=2	P=3
Switches	I_{rms}	260A	140A	90A
Diodes	I_{avr}	50A	28A	18A
C_2	I_{rms}	112A	58A	40A
C_1	I_{rms}	150A	57A	37A

that Shottky diodes can be used. The multiplier cell converter could have considerable reverse recovery associated problem, which may result in limitation in switching frequency. The coupled inductor converter has considerable total energy volume of the inductor and, in general, it is difficult to apply to high power due to problems associated with leakage inductance of the coupled inductor. The proposed converter does not have serious problems associated with diode reverse recovery and magnetic coupling so that it is suitable to achieve high frequency and high power in high step-up applications.

IV. EXPERIMENTAL RESULTS

A prototype of the proposed converter with $N = 2$ and $P = 1$ (see Fig. 6) has been built with the specification used in Section III-A. Both lower and upper switches are implemented with IXYS IXTQ69N30P (300 V, 69 A, 49 mΩ) MOSFET. Fast recovery diodes of International Rectifier MUR820 (200 V, 8 A, 25 ns) are used for all rectifier diodes. Input filter inductor L_1 and auxiliary inductor L_2 are 50 μ H and 4 μ H, respectively. The designed values of auxiliary capacitors $C_{2,11}$ and $C_{2,12}$ are 10 μ F 260 V and 10 μ F 150 V, respectively. An off-the-shelf film capacitor of 20 μ F 600 V was used for all auxiliary and output capacitors.

The experimental waveforms of the proposed scheme are shown in Fig. 10. Fig. 10(a) shows the voltage and current waveforms of the auxiliary inductor $L_{2,21}$. Fig. 10(b) and (c) illustrates that both upper switch $S_{U,21}$ and lower switch $S_{L,21}$ are being turned on with ZVS. Fig. 10(d) and (e) shows that diode $D_{U,21}$ and $D_{L,21}$ are being turned off with ZCS. The measured and calculated efficiencies are shown in Fig. 11. The

TABLE V
COMPARISON BETWEEN CONVENTIONAL HIGH STEP-UP INTERLEAVED SOFT-SWITCHING CONVERTERS AND PROPOSED CONVERTER
($P_o = 1.5$ kW, $V_I = 40$ V, $V_o = 380$ V, $f_s = 70$ kHz, $\Delta I_s = 5\%$, $\Delta V_o = 1\%$)

		Coupled Inductor	Multiplier Cells	Proposed
Chosen topology		Fig. 2 of [17] $n=1, k=0.987$	Fig. 40 of [20] $M=2, P=2$	Fig. 6 $N=2, P=1$
Operating duty cycle		0.69	0.69	0.71
Switches	V_{pk}, I_{pk}	$2 \times 160V, 38.8A$ $2 \times 160V, 9.2A$	$2 \times 164V, 38.3A$	$2 \times 142V, 27.3A$ $2 \times 142V, 26.3A$
	q	4	2	4
	U	15.8	11.9	9.8
	Switching method	ZVZCS	ZCS	ZVZCS
Diodes	V_{pk}, I_{pk}	$2 \times 224V, 13.9A$ $2 \times 160V, 19.4A$ $2 \times 90V, 38.4A$ $2 \times 90V, 9.03A$	$2 \times 260V, 16.8A$ $3 \times 250V, 20.3A$ $2 \times 254V, 18.9A$ $3 \times 150V, 20.3A$	$2 \times 120V, 22.6A$ $2 \times 120V, 8.1A$
	q	8	10	4
	U^*	8.1	3.7	26.2
	Reverse recovery problem	negligible	D_{M1} and D_{M2} are considerable	negligible
Total energy volume of Inductors (ΣLI^2)		8.3	1.8	1
Total energy volume of Capacitors (ΣCV^2)		1	1.6	2.7

$$*U(\text{Utilization factor}) = \frac{P_o}{V_{pk} \times I_{pk} \times q}, \quad \text{where } q = \text{number of components}$$

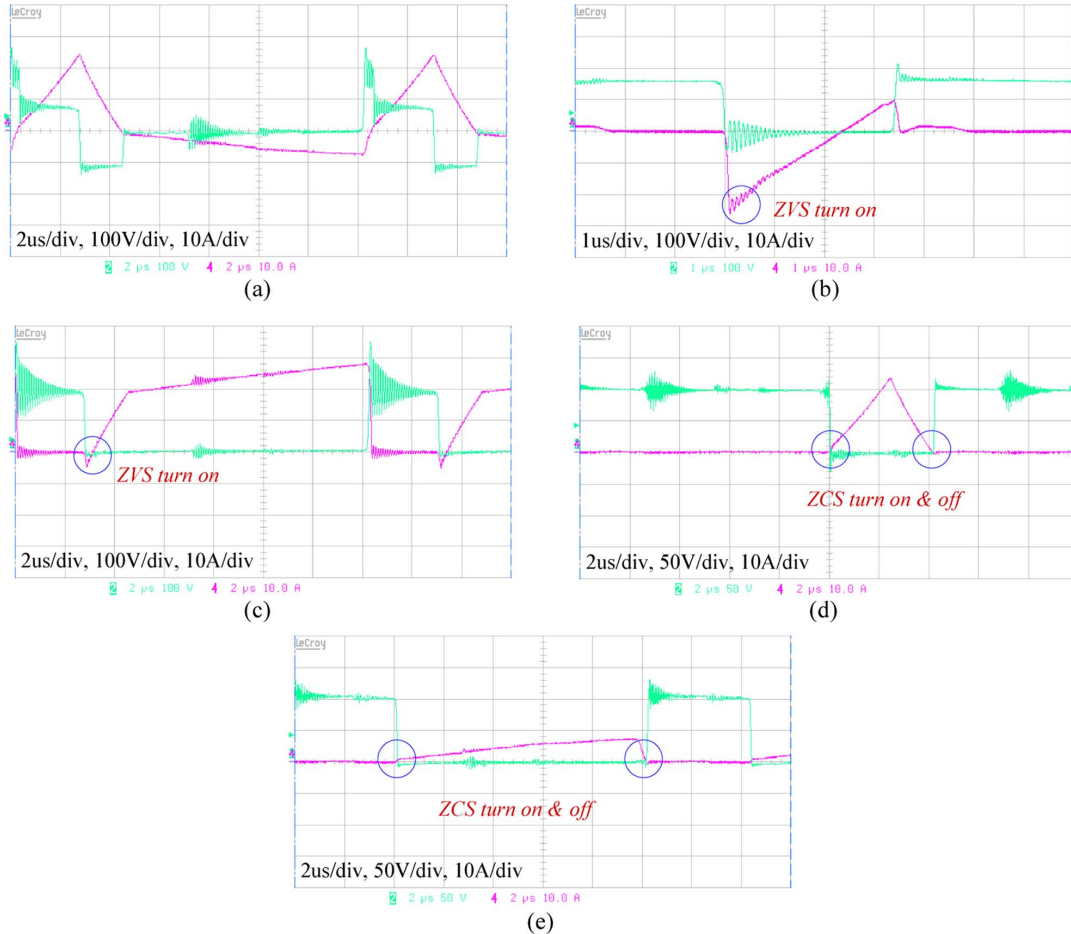


Fig. 10. Experimental waveforms of the proposed converter with $N = 2$ and $P = 1$. (a) Voltage and current waveforms of the auxiliary inductor $L_{2,21}$. (b) Voltage and current waveforms of the upper switch $S_{U,21}$. (c) Voltage and current waveforms of the lower switch $S_{L,21}$. (d) Voltage and current waveforms of the upper diode $D_{U,21}$. (e) Voltage and current waveforms of the lower diode $D_{L,21}$.

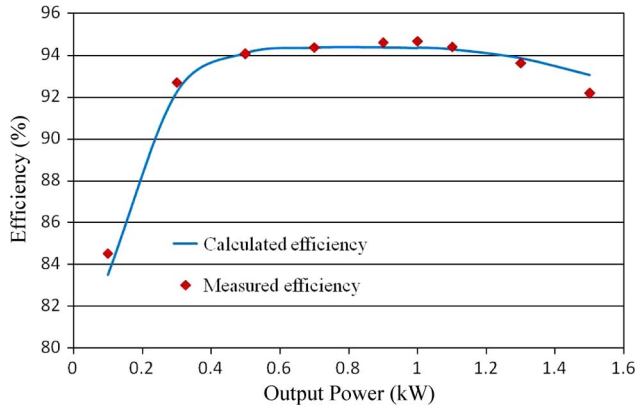


Fig. 11. Efficiency of the proposed converter.

TABLE VI
CALCULATED POWER LOSSES AT FULL LOAD CONDITION

Loss composition		Loss(W)
Upper switches	switching	6.2
	conduction	4.4
Lower switches	switching	23.7
	conduction	26.3
Diodes	conduction	27.1
Others		16
Total losses		103.7

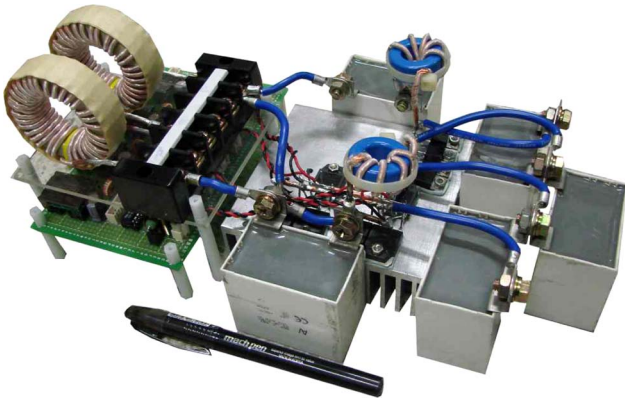


Fig. 12. Photograph of the 1.5-kW soft-switched CCM boost converter prototype.

measured efficiency of the proposed converter maintains over 92% in most of the load range. The peak efficiency of 94.7% was measured at 1-kW load. Fig. 12 shows the photograph of power circuit of the prototype. The calculated power losses under full load condition are listed in the Table VI. It indicates that the power loss associated with lower switches, which is

approximately 50% of the total loss, is the dominant source of the losses at full load condition.

V. CONCLUSION

In this paper, new soft-switched continuous-conduction-mode (CCM) boost converters suitable for high voltage and high-power application have been proposed. Given output voltage and power level, an optimized circuit can be configured by determining proper numbers of series and parallel connection of basic cells, which leads to flexibility in device selection resulting in high component availability and easy thermal distribution.

The proposed converter has the following features.

- 1) ZVS turn-on of the active switches in CCM.
- 2) Negligible diode reverse recovery due to ZCS turn-off of the diodes.
- 3) Greatly reduced components' voltage ratings.
- 4) Reduced energy volumes of passive components due to interleaving effect.

Two design examples are shown to illustrate how to determine the optimum circuit configuration. Experimental results from a 1.5-kW prototype have been provided, and the peak efficiency of 94.7% was measured at 1 kW.

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Author's photographs and biographies not available at the time of publication.