Power Density Optimization of 700 kHz GaN-Based Auxiliary Power Module for Electric Vehicles

Adhistira M. Naradhipa, Sangjin Kim, Daeki Yang, Sewan Choi, *Fellow, IEEE*, Inyong Yeo, and Younsik Lee

***Abstract*—This article proposes a high-power density 1.8 kW auxiliary power module (APM) for electric vehicles (EVs) based on gallium nitride devices. A design procedure for the high-frequency phase-shift full-bridge with current-doubler rectifier using printed circuit board (PCB)-based planar magnetics is proposed. Leakage inductance analysis of the high-frequency pulsewidth-modulation converter is given to achieve both regulation and zero-voltage-switching turn-ON. Then, the magnetics optimization procedure for the customized planar core is proposed with a magnetic figure-of-merit concept to meet the high-power density target. Technical considerations are detailed to meet the extreme temperature constraint imposed on the EVs components. Finally, the proposed APM is demonstrated with a switching frequency of 700 kHz and a power density of 8.1 kW/L (132.8 W/in^3).**

***Index Terms*—Auxiliary power module (APM), electric vehicles (EVs), high power density, optimization, phase-shift converter, planar magnetics.**

I. Introduction

In the past few years, the electric vehicles market shows a high demand for a longer driving range (more than 300 miles), which increases the space for high-voltage (HV) battery and decreases the vehicle footprint. As such, all the other electric vehicles (EVs) component's power density should be increased. In addition, the trend shows a proliferation of automation in EVs, which adds new auxiliary loads, such as cameras, radar, light detection and ranging, and central processing units. All of the EVs auxiliary loads are supplied by an auxiliary power module (APM) from the HV battery, as shown in Fig. 1 [1]–[7]. Therefore, the power level of the APM tends to increase up to 5 kW, which requires the APM to have a high-power density and high efficiency to fit into the limited EVs space.

In order to fulfill the space and power requirements, the US Department of Energy (DoE) sets a power density and efficiency target for APM to reach 4.5 kW/L and 98%, respectively, in 2025 [8]. However, it is not an easy task to realize the US DoE targets with the current Si-based APM's technology [9]–[10], as the APM has several challenges:

1) increase of output current requirement;
2) wide voltage range;
3) limited switching frequency;
4) high step-down ratio with single-turn secondary winding; and
5) high engine room temperature.

Therefore, the use of wide-bandgap devices, optimized design of magnetics, and selection of a suitable topology are crucial for a compact APM with a wide voltage range.

This article discusses the first phase of a GaN-based low-profile APM development project using PCB magnetics that addresses the abovementioned challenges and the possibility of achieving the design target, as given in Tables I and II. In the first phase, achieving the highest possible power density by greatly increased switching frequency while maintaining the acceptable operating temperature is the primary concern. Then, the efficiency will be improved in the second phase's prototype while complying with the power density target.

There are two state-of-the-art topologies for APM: resonant-based topology, and pulsewidth modulation (PWM) based topology. A two-stage non-isolated PWM-based converter followed by a DC transformer (DCX) resonant converter is a prevalent method to reduce the switching frequency range under a wide

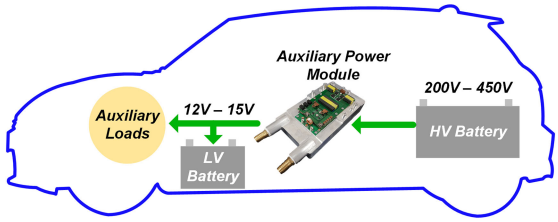

Fig. 1. Typical EVs powering systems for auxiliary loads.

TABLE I
Design Specification for EVs APM

Item	Values
Maximum power	1.8kW
Input voltage	200V – 310V
Output voltage	12.8V – 15.1V (13.0V$_{nom}$)
Maximum output power	129.5A
Target power density excluding heatsink	> 6kW/L

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Adhistira M. Naradhipa, Sangjin Kim, Daeki Yang, and Sewan Choi are with the Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul 01811, South Korea (e-mail: adhistira.madhyasta@gmail.com; winston88@seoultech.ac.kr; liam.yang@destinpower.com; schoi@seoultech.ac.kr).

Inyong Yeo and Younsik Lee are with the Department of Electric Power Conversion Engineering Design, Hyundai Motor Company, Hwaseong 18280, South Korea (e-mail: yiy1027@hyundai.com; 6302232@hyundai.com).

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TABLE II
DESIGN CONSTRAINTS FOR EVs APM

Item	Values
Maximum APM height excluding heatsink	17mm
Maximum temperature rise	50°C (with 65°C liquid coolant)
Number of PCB layers	4 layers
PCB copper thickness	3oz (0.1041mm)

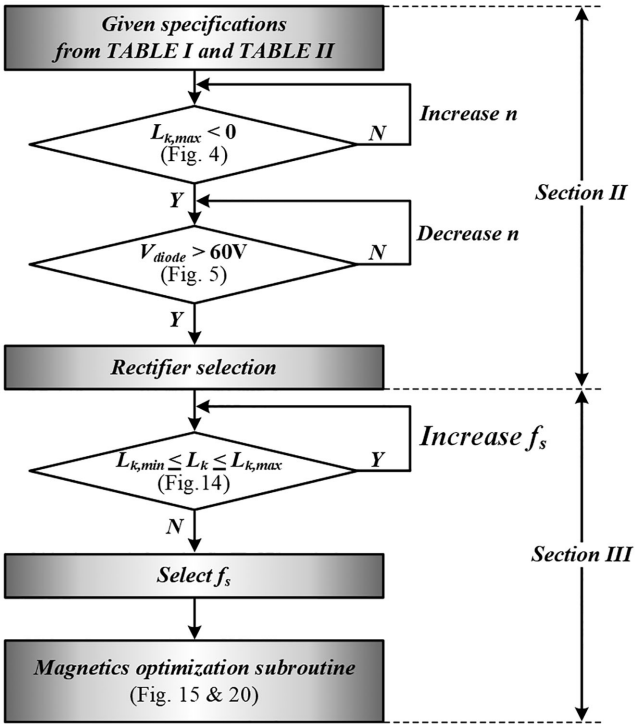


Fig. 2. Proposed design flowchart for high-frequency EVs APM.

voltage range. Combining three IPOP DCX LLC converters with a buck regulating stage for a 2 kW APM, [11] achieved a good efficiency and a power density of 1.9 kW/L with 1 MHz switching frequency. However, the two-stage approach increases the component counts and circuit complexity. A 1-kW GaN-based bidirectional SRC converter achieving a power density of 15.38 kW/L for APM is proposed in [12]. However, a sophisticated control with an open-loop look-up table was used to reduce the switching frequency range and achieve the high-power density.

One common PWM-based topology for EVs APM is the active-clamp forward (ACF) converter. In [13], a low-profile 4.4 kW/L, 490 W APM using ACF-based topology with 1.8 MHz effective switching frequency was developed. However, high component count increased the complexity of the APM. Moreover, the 650-V GaN devices cannot be applicable in the ACF converter when the HV battery voltage reaches 450 V. In the meanwhile, the phase-shift full-bridge (PSFB) has been widely adopted as a topology for EVs APM [14]–[19]. The 650 V GaN devices can be used in the PSFB converter. A power density

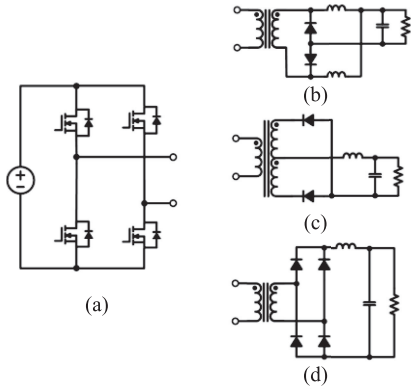


Fig. 3. Phase-shift full-bridge converter. (a) Full-bridge primary circuit. (b) CD rectifier. (c) CT rectifier. (d) FB rectifier.

of 12.5 kW/L was achieved in GaN-based PSFB [19], using a switching frequency of 500 kHz. However, this article did not discuss important issue in high-frequency PSFB converter design that need to be addressed to achieve the desired power density such as duty loss, selection of rectifier circuit, and magnetic optimization.

A zero voltage switching (ZVS) operation, especially at turn-ON, is necessary to use GaN devices at high switching frequency [19], [20]. However, in the high switching frequency PSFB converter, the requirement of high leakage inductance that is required to achieve a ZVS turn-ON under a wide load range contradicts the requirement of small enough leakage inductance to guarantee whole range voltage regulation. Therefore, design of leakage inductance along with comparison and selection of the common PSFB rectifier circuit for APM application at high switching frequency is given in this article, especially about duty loss and PCB winding-based magnetics, which was not clearly discuss in the previous works [16], [19], [21].

This article discusses a high-power density high switching frequency design procedure, as given in Fig. 2, for the PSFB-based EVs APM. The analytical rectifier topology selection based on the upper boundary of the leakage inductance and PCB winding magnetic components size is discussed in Section II. The switching frequency selection based on the leakage inductance and magnetics optimization using the proposed figure-of-merit is discussed in Section III. Details of the prototype, including the proposed PCB structure in extreme car's engine room temperature, and the experimental results are given in Section IV.

II. SELECTION OF THE PSFB RECTIFIER CIRCUIT

There are three common options of the rectifier circuit for the PSFB converter: center-tap (CT); current-doubler (CD); and full-bridge (FB), as shown in Fig. 3. In this section, the choice of the rectifier circuit is based on the qualitative and quantitative comparisons between the three rectifiers, considering the project design constraints given in Table II in addition to the specification in Table I.

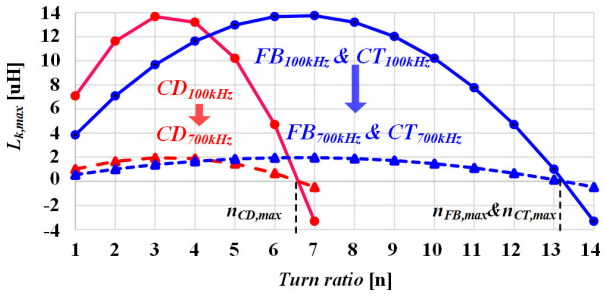


Fig. 4. Allowable maximum leakage inductance versus turn-ratio with switching frequency variation.

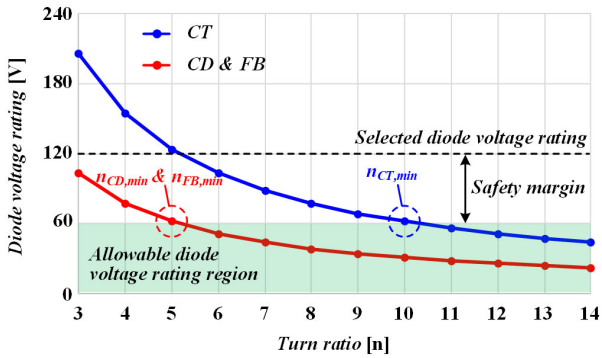


Fig. 5. Secondary diode voltage rating versus turn-ratio.

A. Analysis and Comparison Between Rectifier Circuits on Leakage Inductance in High Frequency PSFB Converter

It is well-known that the PSFB converter suffers from the duty loss D_{loss} that reduces the usable duty range for voltage regulation due to the voltage drop across the leakage inductor [22], which is becoming significantly problematic at the high-frequency operation.

Based on [22]–[24], the effective duty cycle in a PSFB converter is $D_{\text{eff}} = D - D_{\text{loss}}$, with D is the command duty from the controller. A PSFB converter with a CD rectifier requires half of the turn-ratio compared to CT and FB to achieve the same voltage gain with the same duty cycle [21]. Moreover, regardless of the rectifier circuit, a phase shift of 180° results in the maximum voltage gain and maximum command duty of $D_{\max} = 0.5$ using a 360° basis. To guarantee whole voltage range operation, D_{loss} should be limited to $D_{\text{loss,max}}$, as in (1).

The formula for D_{loss} as the function of L_k is given in [22]–[24]. The allowable maximum leakage inductance value can be calculated using (2) by following the step in [22] and assuming negligible output inductor current ripple. It is shown from Fig. 4, using (1) and (2), that the allowable maximum leakage inductance $L_{k,\max}$ that is required to achieve the voltage regulation drastically drops as the switching frequency is increased from 100 to 700 kHz, and for the specification in Table I, the maximum turn-ratios $n_{\max}$ are 6.7 for CD and 13.2 for both CT and FB at 700 kHz

$$D_{\text{loss,max}} = \begin{cases} 0.5 - \frac{n \cdot V_{o,\max}}{2 \cdot V_{\text{in,min}}}; & \text{CT and FB} \\ 0.5 - \frac{n \cdot V_{o,\max}}{V_{\text{in,min}}}; & \text{CD} \end{cases} \tag{1}$$

$$L_{k,\max} = \begin{cases} \frac{n \cdot V_{\text{in,max}} \cdot D_{\text{loss,max}}}{2 \cdot I_o \cdot f_s}; \text{ CT and FB} \\ \frac{n \cdot V_{\text{in,max}} \cdot D_{\text{loss,max}}}{I_o \cdot f_s}; \text{ CD.} \end{cases} \tag{2}$$

Fig. 5 shows that the voltage rating of secondary diodes decreases as n increases. In this article, Si-based diodes with voltage rating V_{diode} of 120 V are selected as the low voltage side devices. A safety margin of 60 V is used considering the diode voltage spike. Therefore, the minimum turn-ratios $n_{\min}$ are five for CD and FB, and ten for CT. From Figs. 4 and 5 the usable range of n for CD is $5 \leq n_{\text{CD}} \leq 6.7$, while they are $10 \leq n_{\text{CT}} \leq 13.2$ for CT and $5 \leq n_{\text{FB}} \leq 13.2$ for FB. To minimize the leakage inductance value, the selected turn-ratios are 10 for CT and 5 for both CD and FB. Therefore, CD and FB are preferred because the value of L_k is proportional to the square of number of turns [25], [26].

B. Analysis of Footprint in High-Current PCB-Winding-Based Magnetics Between Rectifier Circuits for PSFB Converter

A low-profile APM is beneficial for space allocation inside the EVs engine room. With the given limited transformer height of 17 mm, PCB winding magnetics are chosen in this article. A high switching frequency in high current applications limits the PCB copper thickness due to the skin effect, which makes the transformer winding footprint dominant over the core footprint due to increased winding width. Therefore, the transformer winding design becomes crucial for a high-power density APM.

Because of the high secondary winding current, a one-turn secondary is used, as shown in Fig. 6. Using (3), the secondary winding footprint, excluding the outer leg cores, can be calculated. From Fig. 7, the CT requires two independently operating secondary windings, which should be arranged in two different layers. On the other hand, the CD and FB only requires one operating secondary winding, which can be arranged in parallel layers to reduce the winding rms current in each layer by half, as shown in Figs. 8 and 9. Thus, the CD secondary winding footprint is much smaller, with only 1104.9 mm^2 than the CT with 3176 mm^2, excluding the outer leg cores. However, FB secondary footprint is 2096.7 mm^2 which is higher than CD because the secondary current of FB is twice of CD.

$$x_s \cdot y_s = 4 \cdot \left(W_s^2 + d_c^2\right) + (2 \cdot a + 2 \cdot b)\left(W_s + d_c\right) + (a \cdot b + 8 \cdot d_c \cdot W_s). \tag{3}$$

Unlike the secondary winding, the primary winding width is much smaller. However, the number of primary turns n_p in the PCB winding transformer under a limited number of layers has a considerable effect on the footprint. Equation (4) and Fig. 10 are used to calculate the primary winding footprint, and the effect of n_p on the footprint is shown in Fig. 11. From Figs. 7–9, the maximum primary turn is 5 for CT and 3 for CD and FB, which results in a similar footprint around 1500 mm^2 for CT and CD. However, the primary winding footprint for FB is 2950 mm^2 due to higher primary current. From the secondary winding and primary winding footprints evaluation, the CT transformer footprint is determined by the secondary winding, whereas

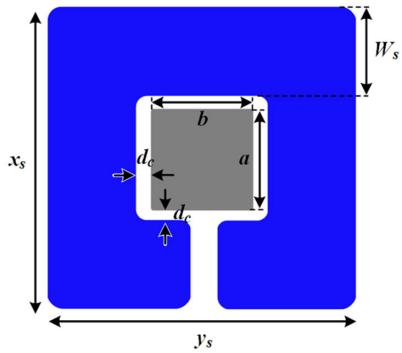


Fig. 6. Dimension of PCB-based one-turn secondary winding.

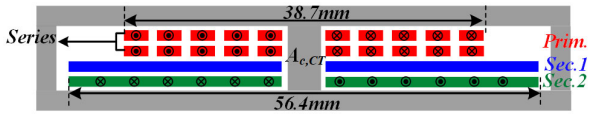


Fig. 7. Front-view of transformer for CT rectifier.

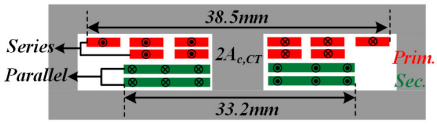


Fig. 8. Front-view of transformer for CD rectifier.

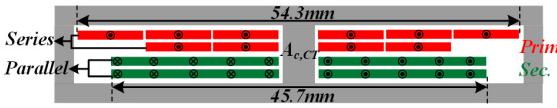


Fig. 9. Front-view of transformer for FB rectifier.

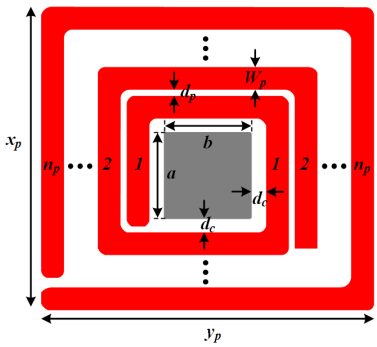


Fig. 10. Dimension of PCB-based primary winding.

the primary winding determines the CD and FB transformer footprints

$$x_p \cdot y_p = 4 \cdot \left(n_p^2 \cdot W_s^2 + d_c^2\right) + d_p^2 \cdot (n_p - 1)^2 + a \cdot b + d_p\,(n_p - 1) \cdot (4 \cdot n_p \cdot W_p + a + b + 4 \cdot d_c) + 8 \cdot n_p \cdot W_p \cdot d_c. \quad (4)$$

Another magnetic component that should be considered is the output inductor. When designed under the same output ripple current, the total CD output inductor footprint is 2×399 mm^2 which is more than twice of CT and FB output inductor that has a footprint of 319 mm^2. A one-turn inductor is implemented for both topologies, using a four-layer PCB winding connected in parallel in order to reduce the footprint, as shown in Fig. 12. Although the CD's inductors are larger than CT's and FB's inductor, the output inductor size is small compared to the transformer size. Therefore, the CD rectifier is chosen in this paper since the total CD's magnetic components footprint is 30.8% smaller than CT's and 29.9% smaller than FB's, as shown in Table III. Although the data in Table III is for a specific value, the trend of larger magnetic footprints CT and FB magnetic components footprint larger than CD is general for EVs APM application.

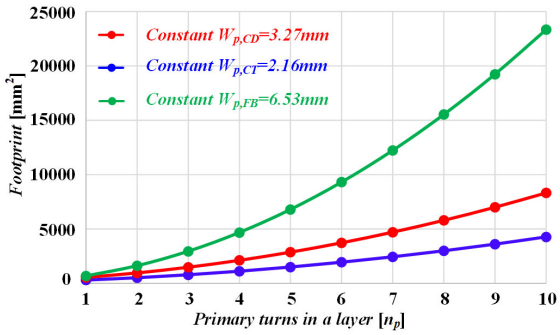


Fig. 11. Primary winding footprint versus number of primary turns in a PCB layer.

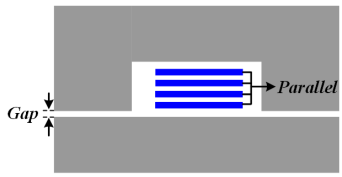


Fig. 12. Front-view of output inductor with one-turn winding.

TABLE III
MAGNETIC COMPARISON BETWEEN SECONDARY RECTIFIER TOPOLOGY

Item	CT	CD	FB
Current density J*		40A/mm^2	
Transformer max. $I_{P,rms}$	9A	13.6A	27.2A
Transformer max. $I_{S,rms}$	90A/layer	34A/layer	68A/layer
Switching frequency*		700kHz	
Turn-ratio	10:1:1	5:1	5:1
Transformer B_{max}*		80mT	
Inductor B_{pk}*		301mT	
Transformer footprint	3915.9mm^2	2133.9mm^2	3869.4mm^2
Inductor footprint	319mm^2	399mm^2·2EA	319mm^2
Total magnetic footprint	4234.9mm^2	2931.9mm^2	4188.4mm^2

*Selected value for the purpose of comparison.

III. FLUX DENSITY AND CURRENT DENSITY-BASED PLANAR MAGNETICS OPTIMIZATION FOR EVs APM

From the previous section, a PSFB-CD with $n = 5$ is chosen for the EVs APM. Magnetic components in PSFB-CD are the

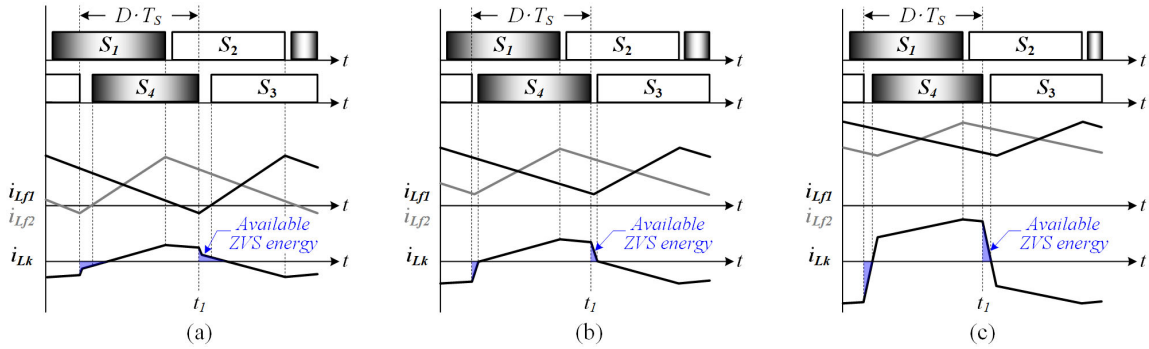


Fig. 13. PSFB-CD operation modes based on output inductor current. (a) DCM. (b) BCM. (c) CCM.

bottleneck to achieve the power density target of 6 kW/L. Therefore, magnetic optimization is required. The first step of the optimization is selecting the appropriate switching frequency.

A. Switching Frequency Selection Based on Leakage Inductance Design Range

The planar transformer core volume is around 5000 mm^3 at switching frequency of 500 kHz for power server application [27]. In EVs APM, not only it has higher power compared with server power application, but also the input voltage is higher and has a wider range, making the transformer volume larger at switching frequency of 500 kHz. Thus, a minimum switching frequency of 500 kHz is chosen.

In isolated PWM-based converters, such as PSFB-CD, increasing the switching frequency will decrease the allowable maximum leakage inductance value due to the duty loss. On the other hand, the required leakage inductance value for achieving ZVS turn-ON increases with the switching frequency. The PSFB-CD has three operating modes, which are continuous conduction mode (CCM), boundary conduction mode (BCM), and discontinuous conduction mode (DCM), depends on the output inductor current, as shown in Fig. 13. In CCM, usually, the leakage inductor energy is high enough to achieve ZVS turn-ON, and in DCM, the output inductor current goes to negative and helps for ZVS turn-ON commutation [19]. However, in BCM, the leakage energy is small, and output inductors do not take part in ZVS turn-ON process. Thus, the minimum leakage inductance $L_{k,\min}$ should be designed at BCM to achieve whole range ZVS turn-ON as expressed as follows [22]–[24]:

$$L_{k,\min} \geq \frac{(2C_{oss} + C_{Tr})\, V_{\text{in}}^2}{i_{Lk,\text{BCM}}^2(t_1)}. \tag{5}$$

Using GaN switch GS66516B from GaN System with C_{oss} of 177pF, and parasitic transformer capacitance C_{Tr} is assumed to be 220 pF [28], [29]. Fig. 14 shows the leakage inductance versus switching frequency curve. The blue line in Fig. 14 is the minimum leakage inductance to achieve ZVS turn-ON from 20% load, which increases with the switching frequency. Moreover, according to (5), the blue line will increase with higher C_{Tr} because more energy is required to achieved ZVS turn-ON. The red line in Fig. 14, plotted using (2), show the maximum leakage inductance to guarantee whole voltage operations, decreasing

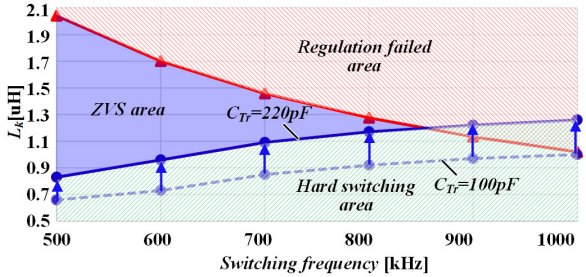


Fig. 14. Leakage inductance versus switching frequency to achieve voltage regulation and ZVS turn-ON.

as the switching frequency increases. Thus, to achieve both objectives of ZVS turn-ON and voltage regulation, the range of leakage inductance value that can be chosen gets narrower as the switching frequency increases. As shown in Fig. 14, between 850 kHz and 1 MHz, there is no solution for leakage inductance value to achieve both objectives simultaneously. The highest switching frequency that can be selected to achieve both objectives is around 800 kHz. However, considering the manufacturing error, the leakage inductance value that can be selected is too narrow at the switching frequency of 800 kHz. Therefore, a switching frequency of 700 kHz is selected to give enough room for the leakage inductance design value.

B. Flux Density and Current Density-Based Optimization of Customized-Core Matrix Transformer

The transformer, which is the bottleneck in achieving a high-power density converter, is optimized in this section. ML91 customized core from Hitachi Metal is chosen as it has the smallest core loss density in the considered switching frequency range [30]–[34]. Several optimization methods of the PCB winding magnetics with a customized core have been introduced for power server application [29], [31], [35], where the final design point is selected from the loss-footprint pareto-front. In this article, a magnetic figure-of-merit (FOM$_{\text{mag}}$), as in (6), is introduced to visualize the magnetic performance differences among the loss-footprint design points in the pareto-front. Fig. 15 shows the proposed matrix transformer optimization flowchart where maximum flux density and current density are the design

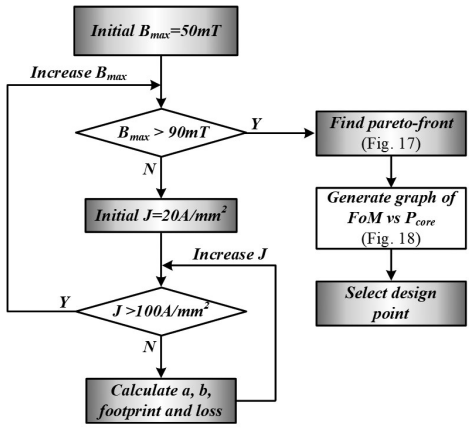


Fig. 15. Proposed transformer design optimization subroutine (from Fig. 2) based on flux density and current density.

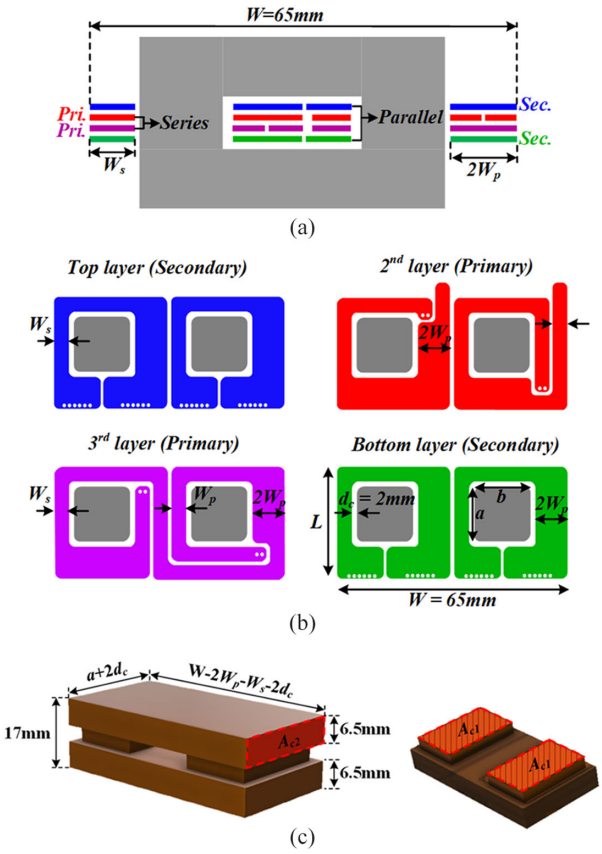


Fig. 16. Proposed planar transformer concept with customized core. (a) Front-view. (b) Top-view.(c) 3-D-view.

variables.

$$\mathrm{FoM_{mag}}(W \cdot m^2) = P_{\mathrm{mag}}(W) \cdot \mathrm{Footprint}(m^2) \quad (6)$$

A matrix transformer concept is used to reduce the leakage inductance and the current rating of the secondary winding [30]–[34]. Fig. 16 shows the proposed transformer core shape and winding arrangement. The top and bottom plates are extended by d_c at each side in order to meet the height limit of 17 mm

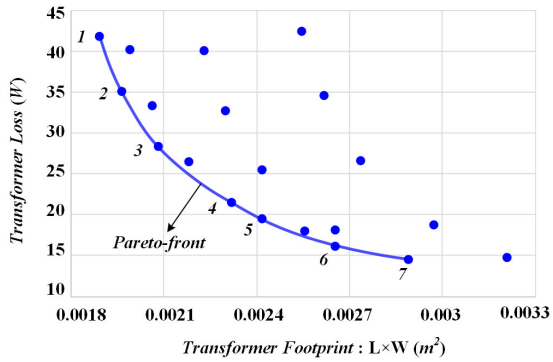


Fig. 17. Loss-footprint design points of the proposed planar transformer.

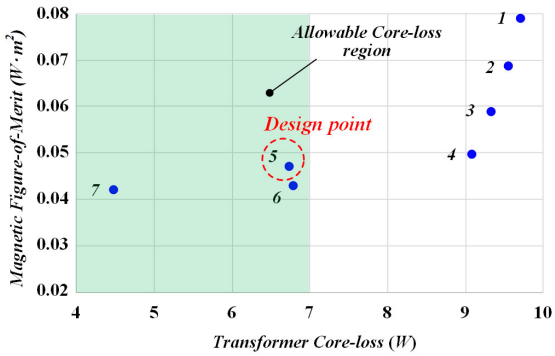


Fig. 18. Proposed figure-of-merit versus core-loss design points for the transformer.

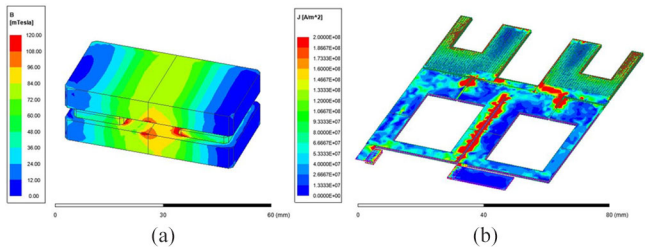


Fig. 19. FEA simulation results of the planar transformer. (a) Flux distribution. (b) Current distribution.

without the need to decrease the core cross-section area. Thus, the core-cross section areas between the leg and top-bottom plates are different. The extended plates do not cover the winding to maximize the heat dissipation for the winding and to minimize the heat induced by the winding to the core. For better heat dissipation, the high current windings are placed on the top and bottom layers and parallel connected.

The maximum flux density $B_{\max}$ is used to calculate core cross-section area A_{c2} of the transformer top and bottom plates, and then length a in Fig. 16 is determined using (7). The current density J is used to calculate primary winding W_p and secondary winding width W_s, and then length b in Fig. 16 is determined using (8). The transformer leg cross-section area A_{c1} in Fig. 16 is the multiplication of a and b. By knowing a, b, W_p, and W_s, the transformer footprint and losses can be calculated [31]–[34],

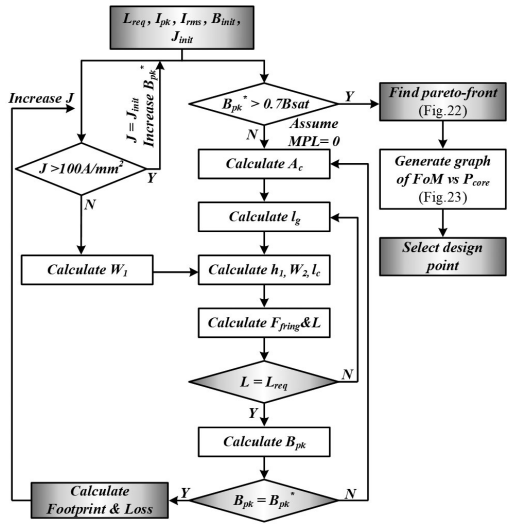


Fig. 20. Proposed inductor design optimization subroutine (from Fig. 2) based on flux density and current density.

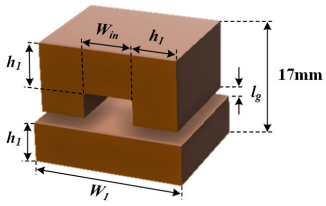


Fig. 21. 3-D-view of the proposed planar inductor.

[36]. Fig. 17 shows several transformer loss-footprint design points where the line shows the pareto-front, and the FoM_{mag} is calculated for seven design points on the pareto-front, which is plotted with the core loss, as shown in Fig. 18

$$a = \frac{\text{volt} - \text{sec}}{2 \cdot n \cdot B_{\max} \cdot 6.5 \text{ mm}} \tag{7}$$

$$b = 0.5 \cdot (W - 4 \cdot W_p - 2 \cdot W_s - 4 \cdot d_c) \tag{8}$$

Design point 5, which corresponds to $B_{\max} = 80$ mT and $J = 40$ A/mm^2, is chosen considering the footprint and the maximum core loss to achieve a thermally stable core. Fig. 19 shows the proposed transformer 3-D finite element analysis (FEA) simulation of the magnetic flux and current distribution. The simulated $B_{\max}$ is around 80mT, which coincides with the selected design point. However, the simulated J is more than 40 A/mm^2 because of the high-frequency effect. Nevertheless, the transformer loss in Fig. 17 includes the ac resistance R_{ac}, which results in total transformer loss of 19.6 W for the design in point 5.

C. Optimization of One-Turn Customized Core Inductor

The two filter inductors in the PSFB-CD are the major component contributing to the total converter footprint. Same with the transformer, ML91 customized core is selected for the inductor core. In this section, an optimization flowchart, which includes the core dimension and air gap calculation to achieve the given

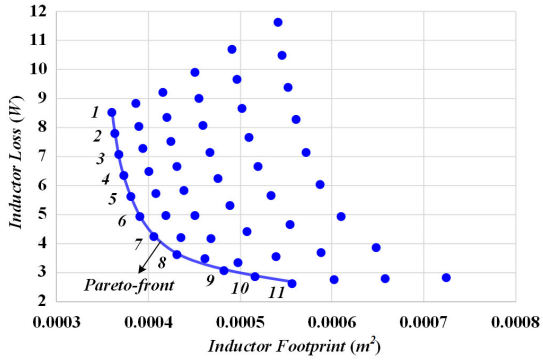


Fig. 22. Loss-footprint design points of the proposed planar inductor.

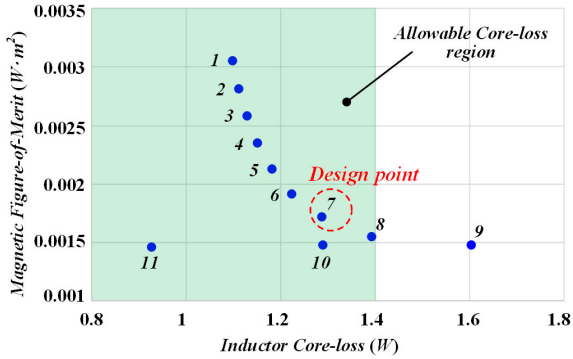


Fig. 23. Proposed figure-of-merit versus core-loss design points for the inductor.

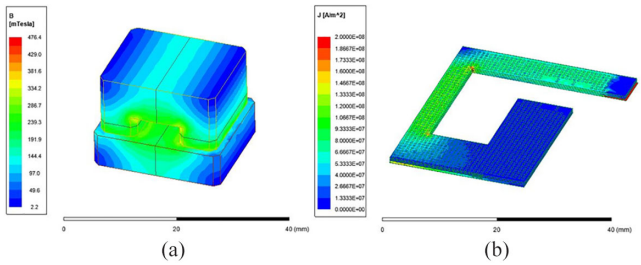


Fig. 24. FEA simulation results of the planar inductor. (a) Flux distribution. (b) Current distribution.

height constraint of 17 mm, is proposed. Fig. 20 shows the proposed optimization flowchart for the one-turn customized core inductor where the peak flux density B_{pk} and the current density J are the optimization variables. The UI core with four windings connected in parallel is used for the proposed inductor, as shown in Figs. 12 and 21. Similar to the transformer optimization, the loss-footprint pareto-front will be generated, and then FoM_{mag} is obtained. The final inductor design is selected by considering the footprint, FoM_{mag} and core loss.

In order to obtain the footprint of the inductor, W_1 and W_2 in Fig. 21 are needed. The value of W_1 is dependent upon the value of h_1 and W_{in}, whereas the value of W_2 is dependent upon h_1 and core-cross section area. Equations in (9) are used to get both W_1 and W_2, and the footprint is obtained by multiplying W_1 with W_2. The other variables in Fig. 20 are calculated using the well-known inductor formulas [37]. The loss-footprint design

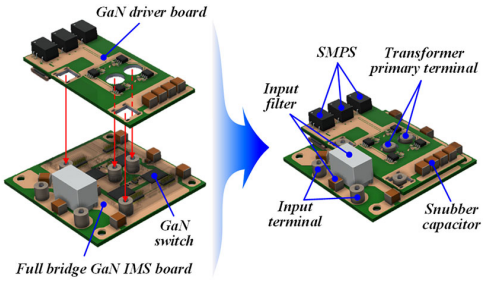


Fig. 25. Stacked concept of gate driver and IMS board for primary switches.

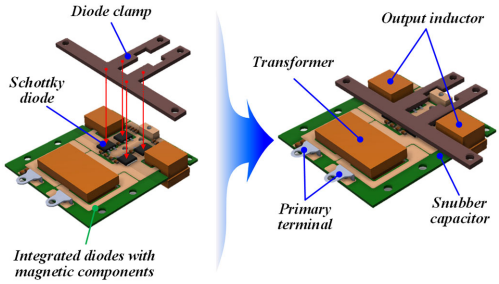


Fig. 26. The proposed diode cooling metal clamp in four-layers PCB board integrated with magnetics.

points are shown in Fig. 22, where the eleven design points in the pareto-front are selected to be plotted in Fig. 23 using the $\mathrm{FoM_{mag}}$ in (6). Design point 7 in Fig. 23 is chosen considering the footprint and the maximum core loss to achieve a thermally stable core. Fig. 24 shows the proposed inductor 3-D FEA simulation of the magnetic flux and current distribution. Fig. 24(a) shows the simulated flux distribution is smaller than $0.7B_{\mathrm{sat}}$ of 301mT. The winding current density within the inductor core is higher than outside of the core, as shown in Fig. 24(b), because there is a fringing effect from the air gap

$$\begin{cases} h_1 = \frac{17\mathrm{mm} - 0.5 \cdot l_{\mathrm{gap}}}{2} \\ W_1 = \frac{I_{\mathrm{rms}}}{J \cdot h} + 4\mathrm{mm} + 2 \cdot h_1 \\ W_2 = \frac{A_c}{h_1}. \end{cases} \tag{9}$$

IV. Experimental Prototype and Measurement Result

A. Experimental Prototype Concept for High Power Density APM

A short gating signal path is important to reduce the gating noise due to the intensified PCB parasitic at the high switching frequency. Therefore, to achieve a short gating path, the stacked PCB concept using an insulated metal substrate (IMS) board is used, as shown in Fig. 25, which also reduces the primary footprint board. For the secondary diode, using a separate IMS board is not recommended as it will increase the termination loss. However, the secondary diode will lose the advantages of good IMS thermal conductivity. Therefore, the integrated four layers PCB board of secondary diodes and magnetic PCB is shown in Fig. 26, in which a metal clamp connected to the heatsink is introduced to enhance the heat dissipation of the high current diodes. The prototype of the proposed high-power density EVs

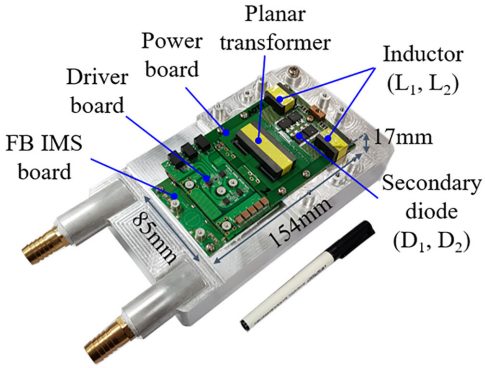


Fig. 27. Proposed 700 kHz, 8.1 kW/L, 1.8 kW EVs APM prototype.

TABLE IV
High Power Density EVs APM Prototype Specification

Item		Values
Power density w/o heatsink		8.1kW/L (85mm×152mm×17mm)
PCB components	Full-Bridge Primary circuit	IMS Board
	Magnetic components and Secondary circuit	Four-layers PCB
	Gate Driver circuit	Six-layers PCB
Switching frequency		700kHz
Transformer	Dimension	65mm×33.5mm×17mm
	# of turns	5:1
	Core	Customized UI ML91 Hitachi core
	B_{max}	80mT
	L_m / L_k	50uH / 0.9uH
Inductor	Dimension	7.9mm×31.8mm×17mm
	Core	Customized UI ML91 Hitachi core
	Inductance	470nH
	B_{pk}	298mT
Primary switches		GaN Systems GS66516B (650V/47A/100°C)
Secondary diodes		VISHAY V60DM120C-M3 (120V/60A/175°C)

APM including the water coolant heatsink, as shown in Fig. 27, achieved a power density of 8.1 kW/L, as detailed in Table IV, excluding the heatsink.

As shown in Table V, the proposed converter achieves power density higher than [11] and [39]. Although the power density in [38] reaches 10 kW/L, the converter is tall with a height of 40 mm and tested only up to 400 W. Despite the excellent power density and efficiency achievement in [12] compared with the proposed APM, a sophisticated variable frequency plus open-loop look-up table control should be used to cover the wide voltage range in EVs APM. Due to the secondary Si-Diode, the proposed APM's measured efficiency is not as high as the previous works. Nevertheless, as shown in Fig. 33, the proposed APM's peak efficiency is estimated to be 94.8% when SR is used. Some important issues for each work are shown in italic in Table V.

TABLE V
COMPARISON WITH THE RECENT GaN-BASED EVs APM

	DELTA [12]*	NUAA [11]	Nagoya Tech. [38]	TOYOTA [39]*	Proposed
Topology	Bidirectional SRC	Two-Stage: Buck + IPOP HB-LLC	Two-Stage: DCM Boost + HB-LLC	FB-FB Multiport Converter	PSFB-CD
Power rating	1kW	2.5kW	1.8kW (*tested only up to 400W*)	1kW	1.8kW
Input voltage	240V-450V	220V-450V	140V-260V	*180V-210V*	200V-310V
Switching frequency	300kHz – 1MHz	1MHz	300kHz	175kHz	700kHz
Switching devices	GaN-FET (HV) & GaN-FET(LV)	GaN-FET (HV) & GaN-FET(LV)	GaN-FET (HV) & GaN-FET (LV)	Si-MOSFET (HV) & GaN-FET (LV)	GaN-FET (HV) & Si-Diode (LV)
Converter height	10mm	39mm	*40mm*	*38.1mm*	17mm
Power density	15.38kW/L	*1.9kW/L*	10kW/L	3.3kW/L	8.1kW/L
Control	*Variable frequency + Open-loop look-up table*	Buck-stage duty	Boost-stage duty + LLC-stage variable frequency	PWM + Phase-shift	Phase-shift
Peak efficiency	96.1% with SR	95.1% with SR	92% with SR	93.9%(12V); 95.35%(48V) with SR	*91.87% (with Si-Diode)*

*Company made prototype.

TABLE VI
IMS BOARD THERMAL RESISTIVITY

Item	Values
Junction-Case $R_{th,J\text{-}C}$	0.27°C/W
Case-IMS $R_{th,C\text{-}IMS}$	0.0065°C/W
IMS-TIM $R_{th,IMS\text{-}TIM}$	0.6°C/W
TIM-Housing $R_{th,TIM\text{-}H}$	0.14°C/W
Housing-Coolant $R_{th,H\text{-}CL}$	0.2°C/W

TABLE VII
PCB BOARD THERMAL RESISTIVITY

Item	Values
Junction-Case $R_{th,J\text{-}C}$	0.95°C/W
Case-IMS $R_{th,C\text{-}PCB}$	0.0065°C/W
IMS-TIM $R_{th,PCB\text{-}TIM}$	0.6°C/W
Estimated Junction-Housing through the proposed cooling metal-plate $R_{th,J\text{-}H}$	3.35°C/W
Housing-Coolant $R_{th,H\text{-}CL}$	0.2°C/W

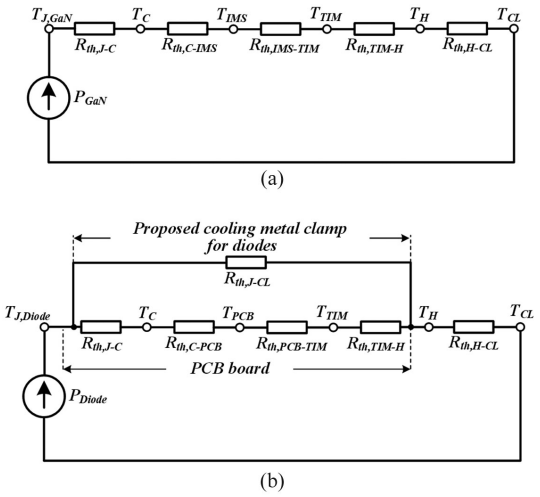


Fig. 28. Thermal equivalent circuit. (a) Primary IMS board. (b) Secondary diodes PCB board with the proposed metal clamp.

B. Thermal Analysis of the Proposed 8.1 kW/L EVs APM

The equivalent thermal circuit for both the primary IMS and secondary PCB boards is shown in Fig. 28. The thermal resistivity for both the primary IMS board and secondary diode PCB board with metal clamp is given in Tables VI and VII, respectively. In order to estimate the junction temperature of both GaN FETs and secondary diodes, (10) is used

$$T_j = (P_{\text{loss}} \cdot R_{\text{th,eq}}) + T_{\text{CL}}. \tag{10}$$

The experiment is done at a room temperature of 30 °C, with the coolant temperature T_{CL} of 20 °C. At input voltage of 310 V and maximum output current of 130A, junction temperature of a GaN FET $T_{J,\text{GaN}}$ is 36.73 °C. The difference between junction and coolant temperature ΔT for GaN FET is 16.73 °C. The calculated diode temperature without the proposed cooling metal clamp is 106.5 °C. However, by implementing the proposed cooling metal clamp, the diode temperature was around 65 °C, as shown in the experimental results, which results in ΔT of 45 °C for secondary diodes. Therefore, $T_{J,\text{GaN}}$ and $T_{J,\text{diode}}$ at engine room with coolant temperature of 65 °C are 81.73 °C and 110 °C, respectively, which are still below the allowable maximum junction temperature of both devices as given in Table IV.

C. Experimental Results of the 700 kHz, 1.8 kW Prototype

The measured leakage inductance of the experimental prototype is 0.9 uH, which is inside the leakage inductance range in Fig. 14. Figs. 29 and 30 show the full-load experimental waveforms of the primary and secondary side for $V_{\text{in}} = 310$ V and $V_{\text{in}} = 200$ V, respectively. When V_{in} is equal to 200V, all switches can achieve ZVS turn-ON. However, at V_{in} is 310V, only the V_{S3} and V_{S4} achieve ZVS turn-ON, whereas V_{S1} and V_{S2} only partially discharged before turn-on due to higher C_{Tr} than the expected value.

In order to check the steady-state thermal performance of the proposed converter, the converter is operated for 11 min, and the thermal data of each device is measured using YOKOGAWA DL850, as shown in Fig. 31. The D1 to D4 in Fig. 31 show the secondary diode temperature, and each diode has a different temperature, although the inductor current is balanced, as shown in Figs. 29 and 30. The temperature difference occurs due to some unsymmetrical in the PCB layout and measurement error. The average temperature of four secondary diodes is 65.8 °C,

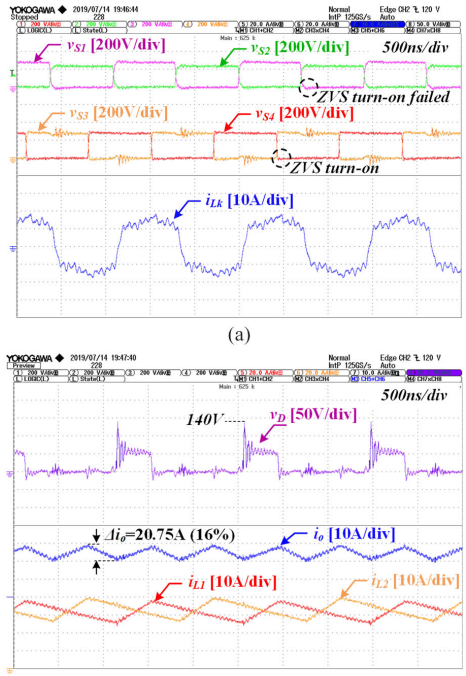


Fig. 29. Experimental waveforms at full-load with $V_{\text{in}} = 310$ V, $V_o = 13.9$ V. (a) HV side. (b) Low voltage (LV) side.

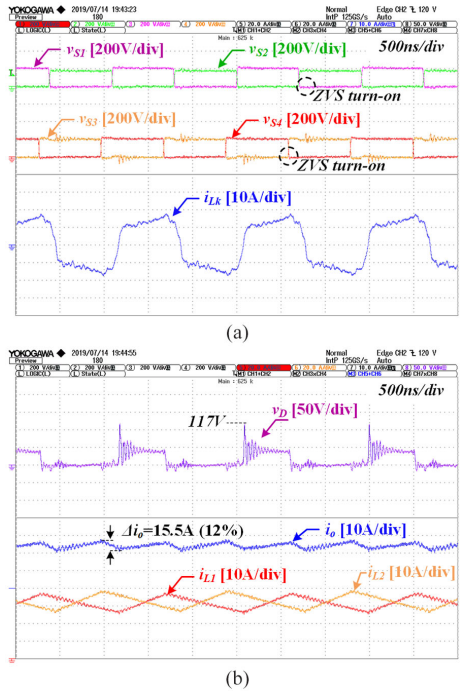


Fig. 30. Experimental waveforms at full-load with $V_{\text{in}} = 200$ V, $V_o = 13.9$ V. (a) HV side. (b) LV side.

which is close to the analysis. Likewise, *S*1 to *S*4 in Fig. 31 gives the thermal measurement of the GaN FETs, in which the average temperature of four GaN FETs is 33.9 °C, which also shows a good estimation of the theoretical analysis. The magnetics thermal picture is given in Fig. 32, which the temperature-rise of both winding and core of the transformer and inductor is still within the maximum temperature rise limit of 50 °C.

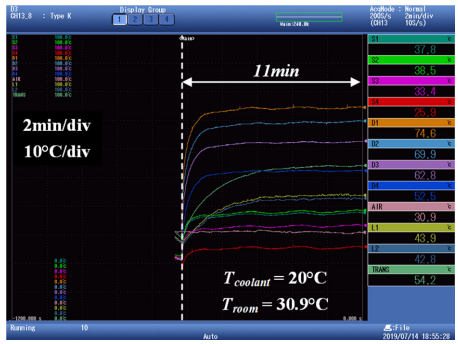
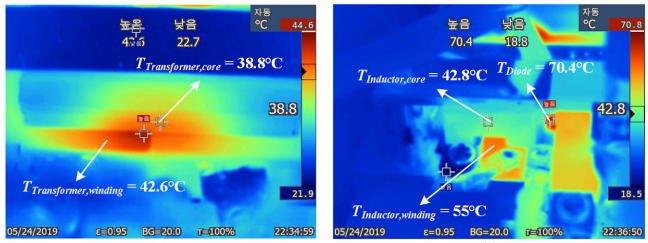


Fig. 31. Thermal test of the proposed 700 kHz EVs APM at full-load.



(a) (b)

Fig. 32. Thermal photograph at full-load. (a) Transformer. (b) Output inductor.

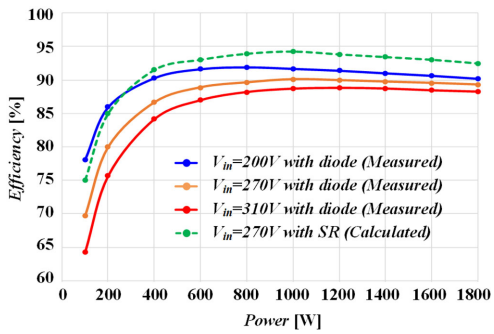


Fig. 33. Measured efficiency curves of the EVs APM at $V_o = 13.9$ V with different V_{in} using Yokogawa WT3000.

Voltage oscillation caused by a resonance between leakage inductance and the parasitic capacitance of the diode is minimized by adding a simple RC snubber for each diode. The snubber component's value was experimentally tuned. The selected values of $R_{sn} = 2.2\,\text{k}\Omega$ and $C_{sn} = 10$ nF for each diode. Both R_{sn} and C_{sn} use 1/4 W 2012 package, and the steady-state temperature is similar to the diode in Fig. 31. Although the diode voltage spike at $V_{\text{in}} = 310$ V is higher than 120 V, the avalanched energy is lower than the allowed maximum avalanched energy by VISHAY V60DM120C-M3. The snubber circuit selection and detailed design will be discussed in the future work for high-frequency EVs APM.

Figs. 33 and 34 show the efficiency curve and loss breakdown at full-load, respectively. The peak efficiency of the prototype is 91.87% at $V_{\text{in}} = 200$V. Replacing the secondary diodes to synchronous rectification (SR) in the future work will increase efficiency by around 5%, as shown in Fig. 33, because the largest portion of the loss is from the secondary diode conduction loss. Although using SR requires more space for gate driver

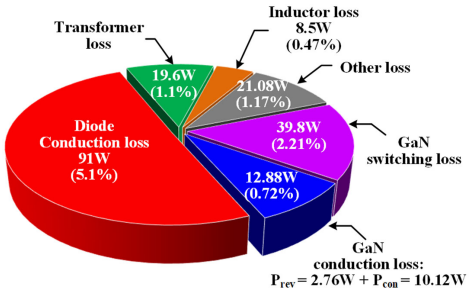


Fig. 34. Loss breakdown at $Po = 1.8$ kW, $V_{\text{in}} = 270$V, and $Vo = 13.9$V.

circuitry, the GaN FETs footprint for the low-voltage side is very small, which will have a small effect on the present prototype's footprint.

In terms of light load efficiency, most of the loss is from switching loss of the GaN FETs. Although GaN FETs have very small output capacitance, the PCB winding transformer capacitance causes the reduction of the ZVS range. Because this present prototype power density is 8.1 kW/L, which exceeds the target power density of 6 kW/L, the tradeoff between efficiency and power density can be done by adjusting the switching frequency. Thus, allowing higher leakage inductance, which results in wider ZVS turn-ON range. Moreover, a transformer winding method to decrease the transformer winding capacitance will be applied in future work.

V. Conclusion and Discussion

In this article, an EVs APM with a high-power density of 8.1 kW/L (132.7W/in^3) is developed by applying a switching frequency of 700 kHz. For a wide voltage range and high-current application, the PSFB-CD is selected as the most suitable topology. An optimization procedure based on pareto-front and FOM_{mag} is introduced and applied for PCB-winding planar magnetics. The FEA simulation results are provided to verify the validity of the proposed magnetics design concept. The experimental results show that the proposed high-power density EVs APM is able to operate over a wide input voltage (200–310 V) and wide output voltage (12.8–15.1 V) range with 1.8 kW of rated load. The experimental prototype achieves 91.87% of efficiency, without SR, at the power of 1 kW ($V_{\text{in}} = 200$ V and $V_o = 13.9$V).

The achieved power density of 8.1 kW/L exceeds the power density target of 6 kW/L. In order to further increase the efficiency while satisfying the power density target of 6 kW/L, several suggestions are made for future work.

1) Reduction of parasitic transformer capacitance by proper winding arrangement.
2) Reduction of magnetizing inductance: trade-offs between conduction and switching losses.
3) Applying SR to decrease conduction loss, which dominates in EVs APM.
4) Tradeoff between efficiency and power density, which can be done by adjusting the switching frequency, allows higher leakage inductance, thereby wider ZVS turn-ON range.
5) Integration of the planar transformer and output inductors.

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Adhistira M. Naradhipa was born in Indonesia in 1993. He received the B.Eng. degree in electrical engineering from University Indonesia, Depok, Indonesia, in 2015, and the M.Sc. degree in electrical and information engineering from the Seoul National University of Science and Technology, Seoul, Korea, in 2019.

He is currently an Associate Researcher in electric power and energy studies at the Department of Electrical Engineering, Universitas Indonesia. His current research interests include dc-dc converters and ac-dc converters for renewable energy and electric vehicles.

Sangjin Kim was born in Korea in 1988. He received the B.S. and M.S. degrees in control and instrumentation engineering in 2012 and 2017, respectively, from the Seoul National University of Science and Technology, Seoul, Korea, where he is currently working toward the Ph.D. degree in electrical and information engineering.

His research interests include high power dc-dc converters and bidirectional dc-dc converters.

Daeki Yang was born in Korea, in 1980. He received the B.S. and M.S. degrees in control and instrumentation engineering in 2009 and 2014, respectively, from the Seoul National University of Science and Technology, Seoul, Korea, where he is currently working toward the Ph.D. degree in electrical and information engineering.

His research interests include bidirectional dc-dc converters and three-phase grid-connected inverters for uninterruptible power supplies and energy storage systems.

Sewan Choi (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 1995.

From 1985 to 1990, he was a Research Engineer with Daewoo Heavy Industries. From 1996 to 1997, he was a Principal Research Engineer with Samsung Electro-Mechanics Co., Korea. In 1997, he joined the Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul, Korea, where he is currently a Professor. His research interests include power conversion technologies for renewable energy systems and dc–dc converters and battery chargers for electric vehicles.

Dr. Choi is President of the Korean Institute of Power Electronics in 2021. He was TPC Chair of ICPE2019-IEEE ECCE Asia held in Busan, Korea. He is currently the Chairman of IEEE PELS Seoul section. He has been serving as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2006.

Inyong Yeo was born in Korea in 1985. He received the B.S. degree in electronic engineering from the the Hanyang University in Seoul, Korea, 2011, and the M.S. degree in nuclear and quantum engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2013.

Since 2013, he has been working as an Electric Power Conversion Engineer for Hyundai Motor Company.

Younsik Lee was born in Korea in 1977. He received the B.S. degree in electrical and electronics from Chung-ang University, Seoul, Korea, in 2005.

He had worked for LG Electronics Company until 2013. Since 2013, he has been working as an Electric Power Conversion Engineer for Hyundai Motor Company.