New Interleaved Current-Fed Resonant Converter With Significantly Reduced High Current Side Output Filter for EV and HEV Applications

Dongok Moon, Junsung Park, *Student Member, IEEE*, and Sewan Choi, *Senior Member, IEEE*

***Abstract*—This paper proposes a new interleaved current-fed resonant converter with significantly reduced high current side output filter. The proposed interleaved converter has theoretically zero output filter capacitance, low-input current ripple, ZCS turn-on and turn-off for all switches and diodes, and zero *di/dt* at turn-off of diodes when operated at load independent points. A two-stage power conversion technique is applied to the interleaved converter for high efficiency under wide voltage range operation. A 2-kW prototype of the proposed low-voltage dc/dc converter for EV and HEV applications is built and tested to verify the validity of the proposed operation.**

***Index Terms*—Current-fed resonant converter, electric vehicle (EV), interleaved, low-voltage dc/dc converter (LDC), soft switched.**

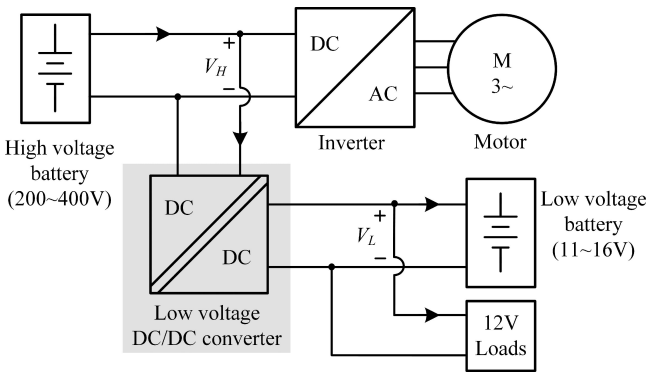

Fig. 1. Block diagram of an EV power train.

I. Introduction

RECENTLY, eco-friendly cars such as an electric vehicles (EVs), hybrid electric vehicles (HEVs) and plug in hybrid electric vehicles (PHEVs) are attracting increasing attention as a solution of environmental pollution, global warming, and exhaustion of fossil fuels. Configurations of several types of HEV and PHEV power train systems are described in [1], and block diagram of an EV power train is shown in Fig. 1. The low- voltage dc/dc converter (LDC) provides power to 12-V loads such as the head lamps, wiper blade motor, electronic power steering, radio system, etc., and charges a 12-V auxiliary battery from a high-voltage battery (200–400 V) [2]. This application requires an efficient (usually, higher than 90%), compact, and light-weight dc/dc converter. Also, due to safety and high step down conversion ratio galvanic isolation is generally required.

The phase shift full-bridge (PSFB) converter [3]–[8] is widely used as the dc/dc converter because of its small RMS current and inherent zero voltage switching (ZVS) characteristic. Disadvantages of the PSFB converter are that turn-off current of switches is large and turn-off losses associated with the diode reverse recovery are considerable. Also, the PSFB converter requires snubber circuits in the rectifier side to reduce the voltage spikes generated at turn-off.

In order to reduce the turn-off losses of switches and diodes resonant converters with ZVS or zero current switching (ZCS) capabilities, such as SRC and LLC could be considered as candidates for the LDC [9]–[13]. The switching frequency of the resonant converter can further be increased due to reduced turn-off losses, which results in reduced size of passive components. In general, the resonant converter requires output capacitor for suppression of output ripple voltage, while the PSFB converter requires output inductor for suppression of output ripple current. The volume of the output filter inductor or capacitor is considerable in the low-voltage high-current application. In order to reduce the volume of the output filter, interleaved techniques can be applied to the resonant and PSFB converters [14]–[16].

However, the effect of volume reduction by means of interleaving of the conventional resonant and PSFB converters is limited, especially in the low-voltage high-current application such as LDC. Also, these converters are hard to achieve high efficiency in whole range of wide input and output voltage application such as LDC. Therefore, two-stage power conversion techniques are used in this wide voltage range application [17]–[19].

This paper proposes a new interleaved current fed resonant converter with significantly reduced high current side output filter, which is suitable for EV and HEV applications. The proposed interleaved resonant converter has the following features: 1) theoretically zero output capacitance, resulting in significantly reduced output capacitor; 2) low input current ripple;

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D. Moon and S. Choi are with the Department of Electrical & Information Engineering, Seoul National University of Science and Technology, Seoul 139-743, Korea (e-mail: dong_ok@seoultech.ac.kr; schoi@seoultech.ac.kr).

J. Park is with the Department of New Energy Engineering, Seoul National University of Science and Technology, Seoul 139-743, Korea (e-mail: pjs09507@seoultech.ac.kr).

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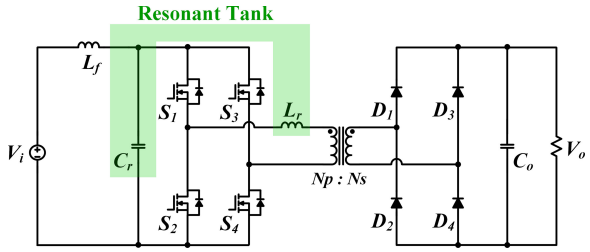

Fig. 2. Proposed current-fed resonant converter.

3) ZCS turn-on and off for all switches and diodes without regard to voltage and load variation; 4) zero *di/dt* at turn-off of diodes, resulting in negligible turn-off losses associated with the diode reverse recovery. A method of two-stage power conversion technique is employed to achieve high efficiency in whole range of wide input and output operating voltage. A 2-kW prototype of the proposed two-stage interleaved converter has been built and tested to verify the validity of the proposed operation.

II. Proposed Current-Fed Resonant Converter

Fig. 2 shows the circuit diagram of the proposed current-fed resonant converter. The proposed converter consists of an input filter inductor, four switches, a resonant tank, a transformer, a diode rectifier, and an output filter capacitor. The output voltage of the proposed converter is regulated by fixed duty and variable switching frequency.

A. Operating Principles

The operating modes and key waveforms of the proposed converter at switching frequency of $f_s = 0.5f_r$ are shown in Figs. 3 and 4, respectively.

Mode I [$t_0 \sim t_1$]: This mode begins with $L_r - C_r$ resonance when switches S_1 and S_4 are turned ON at t_0. The equivalent circuit of this mode is shown in Fig. 5. The resonant voltage and current are determined, respectively, as follows:

$$i_{Lr}(t) = I_i(1 - \cos\omega_r t) \tag{1}$$

$$v_{Cr}(t) = ZI_i \sin\omega_r t + \frac{N_s}{N_p}V_o \tag{2}$$

where Z is the characteristic impedance, and ω_r is the angular resonant frequency. They can be expressed, respectively, as follows:

$$Z = \sqrt{\frac{L_r}{C_r}} \tag{3}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}. \tag{4}$$

Input current I_i is determined as follows:

$$I_i = \frac{N_s V_o}{N_p R_L} \tag{5}$$

where R_L is the load resistance. This mode ends when switches S_1 and S_4 are turned OFF at t_1.

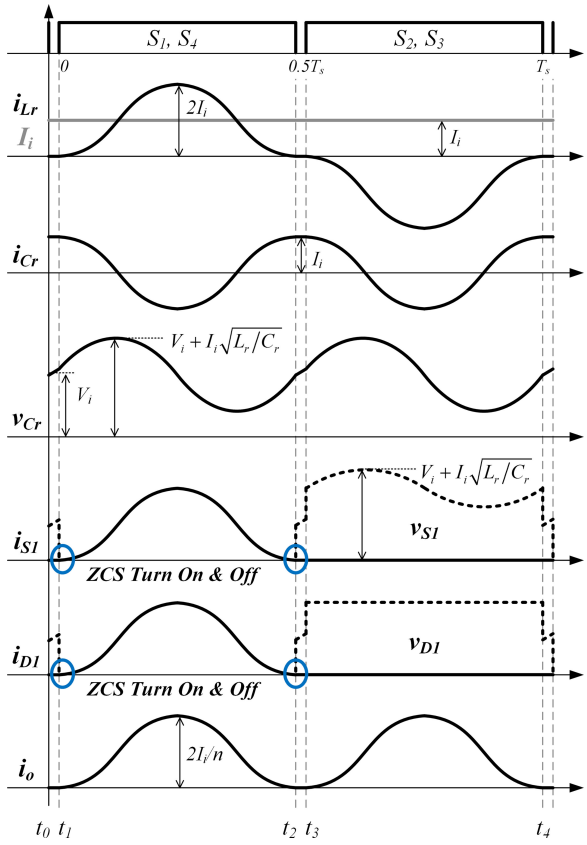

Fig. 3. Key waveforms of the proposed converter at $f_s = 0.5f_r$.

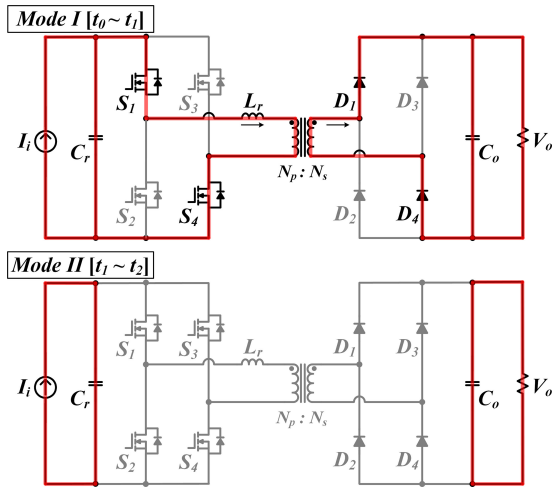

Fig. 4. Operating states of the proposed converter at $f_s = 0.5f_r$.

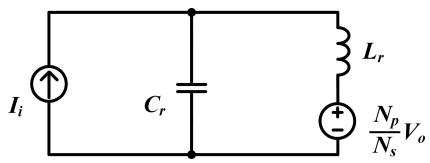

Fig. 5. Equivalent resonant circuits of mode I ($t_0 \sim t_1$).

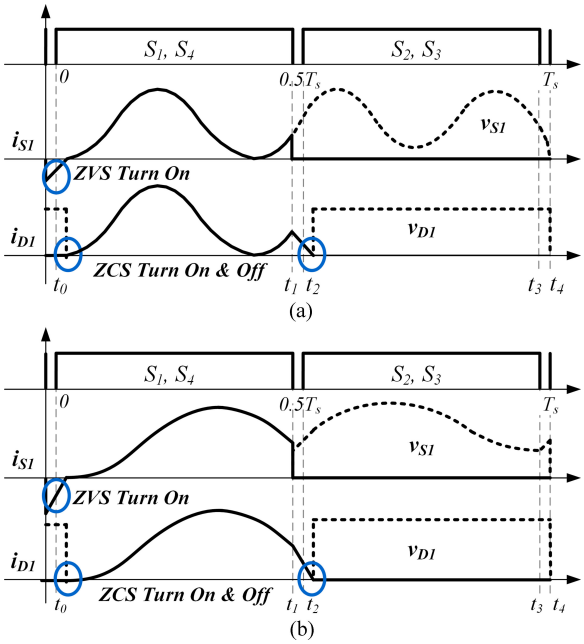

Fig. 6. Voltage and current waveforms of switches and diodes of the proposed converter. (a) Below resonance ($f_s < 0.5f_r$). (b) Above resonance ($f_s > 0.5f_r$).

Mode II [$t_1 \sim t_2$]: During this mode, the power is not transferred to the load and the output filter capacitor supplies

The other half of a cycle is repeated in the same fashion. Note that all switches and diodes are turned ON and OFF under ZCS condition. The voltage and current waveforms of switches and diodes of the proposed converter at switching frequencies of $f_s < 0.5f_r$ (below resonance) and $f_s > 0.5f_r$ (above resonance) are shown in Fig. 6 (a) and (b), respectively. Note that the proposed converter achieves ZVS turn-on at both below resonance and above resonance operations unlike the conventional resonant converter such as SRC [20].

B. Voltage Gain Expression

Assuming that *Mode II*, which corresponds to dead time, is neglected, the average voltage across the resonant capacitor that is equal to the input voltage can be expressed as

$$V_i = V_{Cr.\mathrm{av}} = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} \left(Z I_i \sin \omega_r t + \frac{N_p}{N_s} V_o \right) dt \ . \quad (6)$$

From (6), the voltage gain of the proposed converter is determined by

$$M = \frac{V_o}{V_i} = \frac{(\pi N_p \omega_r)(1 - \cos \frac{\omega_s}{\omega_r}\pi) N_s}{(\pi N_p \omega_r)(1 - \cos \frac{\omega_s}{\omega_r}\pi) N_p + Q\omega_s} \quad (7)$$

where Q is the quality factor, which determines the slope of the voltage gain curve and can be determined as follows:

$$Q = \frac{\omega_r L_r}{R_L}. \quad (8)$$

The higher the Q, the higher is the slope of the gain curve. The voltage gain curves of the proposed converter are as shown in Fig. 7. Note that the load independent points of the proposed converter are multiple in the below resonance region and are determined as follows:

$$f_r = 2\,k\,f_s \quad (9)$$

where k is the natural number. It should also be noted that the voltage gain of the proposed converter converges to 1, while that of the SRC converges to 0 as the switching frequency decreases in the below resonance region. In the above resonance region, the slopes of the voltage gain curves according to Q of the proposed converter have similar values with those of the SRC.

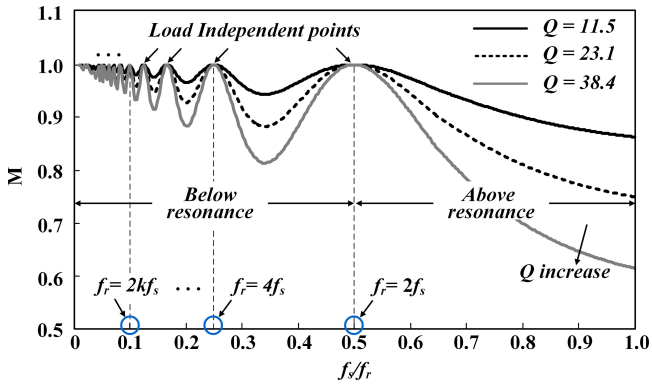

Fig. 7. Voltage gain curve of the proposed converter.

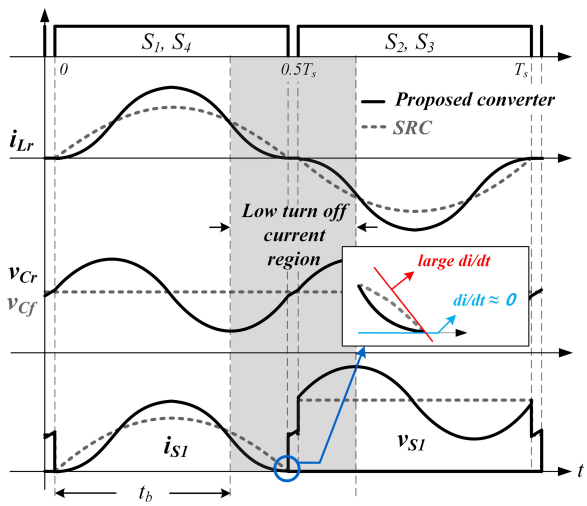

Fig. 8. Comparison of key waveforms of the proposed converter and SRC at load independent point.

C. Comparison of the Proposed Converter and SRC

Fig. 8 shows comparison of key waveforms of the proposed converter and the SRC. Note that the resonant frequency of the proposed converter is two times that of the SRC. During $0 < t < 0.5\ T_s$, the resonant current of the SRC is expressed as

$$i_{Lr\_\mathrm{SRC}}(t) = 1.57 \sin \frac{\omega_r}{2}\, t. \quad (10)$$

TABLE I
COMPARISON OF CHARACTERISTICS OF THE PROPOSED CONVERTER AND SRC AT LOAD INDEPENDENT POINT

		SRC	Proposed converter
Input current ripple		Large	Small
Switches	$V_{\rm pk}$ $I_{\rm rms}$ Switching characteristics	V_i $0.785I_{\rm i}$ ZCS turn-on and off	$V_i + ZI_i$ $0.866I_{\rm i}$ ZCS turn-on and off
Reverse recovery of diodes		Small	Negligible
Ripple current of C_r		$1.1I_{\rm i}$	$0.707I_{\rm i}$

The time t_b at which the resonant currents of the two converters are identical can be obtained using (1) and (10) by

$$t_b = \frac{2.24}{\omega_r}. \tag{11}$$

This means that the turn-off current of the proposed converter is lower than that of the SRC, when the switching frequency of the proposed converter is used as follows:

$$\frac{f_r}{1.402} \le f_s \le 1.402 f_r. \tag{12}$$

The diode *di/dt* at turn-off of the proposed converter is theoretically 0, while that of the SRC is large, as shown in Fig. 8. Therefore, turn-off losses associated with diode reverse recovery of the proposed converter are negligible, while those of SRC cannot be neglected as the switching frequency increases.

The comparison of characteristics of the proposed converter and SRC at a load independent point is summarized in Table I. The proposed converter is the current-fed converter and, therefore, has much smaller input current ripple compared to the SRC which is the voltage-fed converter. The voltage and current ratings of switches of the proposed converter are higher than those of the SRC. The peak value of switch voltage of the proposed converter is affected by characteristic impedance *Z* and can be limited by choosing proper value of *Z*. It should be noted that the ripple current of the resonant capacitor of the proposed converter is 40% smaller than that of the SRC, which significantly reduces cost and volume of the resonant capacitor.

D. Proposed Interleaved Technique

The circuit diagram and key waveforms of the conventional two-phase interleaved series resonant converter (SRC) are shown in Fig. 9. The two SRC are operated at switching frequency, which is the same as the resonant frequency and are phase shifted by $\pi/2$. The output currents of each phase are the secondary winding current rectified by the diode bridge and can be expressed, respectively, as follows:

$$i_{o,1} = \frac{I_o}{2} + \sum_{m=1}^{\infty} \frac{I_o}{(1+2m)(1-2m)} \cos(2m\omega t) \tag{13}$$

$$i_{o,2} = \frac{I_o}{2} + \sum_{m=1}^{\infty} \frac{I_o}{(1+2m)(1-2m)} \cos\left(2m\left(\omega t - \frac{\pi}{2}\right)\right). \tag{14}$$

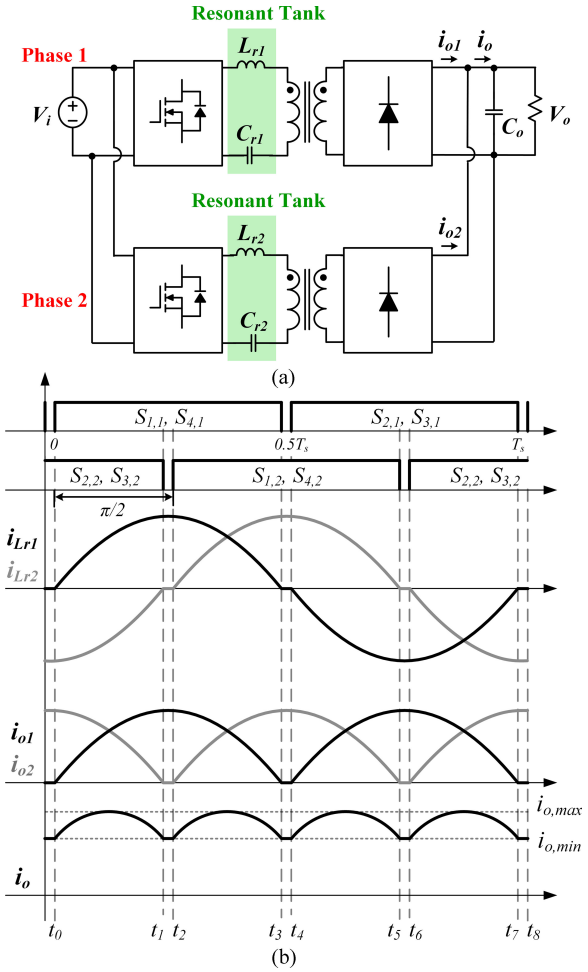

Fig. 9. Conventional two-phase interleaved series resonant converter. (a) Circuit diagram. (b) Key waveforms at $f_s = f_r$.

The output current of the conventional interleaved SRC is obtained by

$$\begin{aligned} i_o &= i_{o,1} + i_{o,2} \\ &= I_o + \sum_{m=1}^{\infty} \frac{2I_o}{(1+4m)(1-4m)} \cos(4m\omega t). \end{aligned} \tag{15}$$

It is seen from (15) that there exist multiples of fourth-order harmonic component in the output current. In general, the output current of the conventional *N*-phase interleaved SRC has ripple contents of multiples of second-order harmonic component as shown in the following equation:

$$\begin{aligned} i_o &= i_{o,1} + i_{o,2} + i_{o,3} + \cdots + i_{o,N} \\ &= I_o + \sum_{k=1}^{N} \sum_{m=1}^{\infty} \frac{2I_o}{k(1+2m)(1-2m)} \\ &\quad \times \cos\left(2m\omega t - \frac{2(m-1)\pi}{N}\right). \end{aligned} \tag{16}$$

Using (16), the ripple current of output capacitor of the conventional *N*-phase interleaved SRC is determined by (17) as

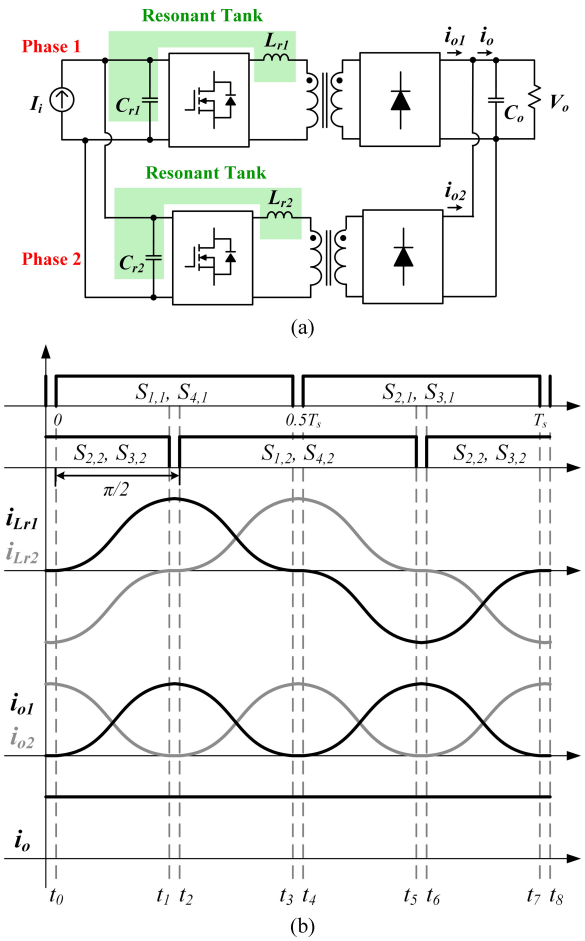

Fig. 10. Proposed two-phase interleaved current-fed resonant converter. (a) Circuit diagram. (b) Key waveforms at $f_s = 0.5f_r$.

shown at the bottom of the page, where $i_{o,\min}$ and $i_{o,\max}$ can be expressed, respectively, as follows:

$$i_{o,\min} = \frac{P_o \pi}{2 V_o N} \sum_{m=1}^{N} \sin\left(\frac{m\pi}{N}\right) \tag{18}$$

$$i_{o,\max} = \frac{P_o \pi}{2 V_o N} \sum_{m=1}^{N} \sin\left(\frac{(2m-1)\pi}{2N}\right). \tag{19}$$

Fig. 10(a) shows the circuit diagram of two-phase interleaved version of the proposed converter. The key waveforms of the proposed two-phase interleaved converter are shown in Fig. 10(b). Each converter is interleaved with phase shift of $\pi/2$. Note that the resonant frequency is selected to be twice of the switching frequency. The output currents of each phase are the secondary winding current rectified by the diode bridge and can be obtained

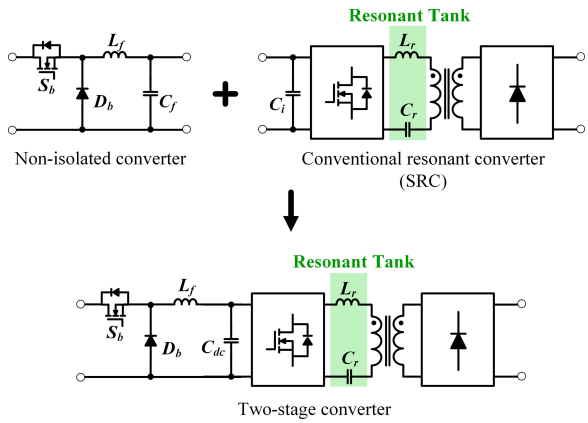

Fig. 11. Concept of the conventional two-stage converter.

by

$$i_{o1} = \frac{1}{2} I_o (1 - \cos(\omega_r t)) \tag{20}$$

$$i_{o2} = \frac{1}{2} I_o (1 + \cos(\omega_r t)). \tag{21}$$

The output current of the proposed interleaved converter is obtained by

$$\begin{aligned} i_o &= i_{o1} + i_{o2} \\ &= \frac{1}{2} I_o (1 - \cos(\omega_r t)) + \frac{1}{2} I_o (1 + \cos(\omega_r t)) = I_o. \end{aligned} \tag{22}$$

It should be noted that ac ripple components of the output current are completely eliminated and the output current is ripple free, meaning that required output capacitance C_o is theoretically zero. The proposed interleaving technique is very effective especially in the low voltage and high-current applications, where the output filter significantly affects the efficiency and size of the whole system. The concept of interleaving of the proposed current-fed resonant converter can be extended to *N*-phase system. The output current of the *N*-phase interleaved current-fed resonant converter can be obtained by

$$\begin{aligned} i_o &= i_{o1} + i_{o2} + \cdots + i_{oN} \\ &= \sum_{m=1}^{N} \frac{I_o}{N} \left(1 - \cos\left(\omega_r t - \frac{2(m-1)\pi}{N}\right)\right) = I_o. \end{aligned} \tag{23}$$

The two-stage power conversion technique is applied to the proposed interleaved current-fed resonant converter to maximize the advantage of the proposed concept in wide voltage range application. Figs. 11 and 12 show the concept of the

$$I_{\mathrm{Co,rms}} = \sqrt{\frac{1}{\pi} \int_0^{\pi} \left\{ (I_{o.\min} - I_o) + (I_{o.\max} - I_{o.\min}) \sin(N w_r t) \right\}^2 d(N w_r t)} \tag{17}$$

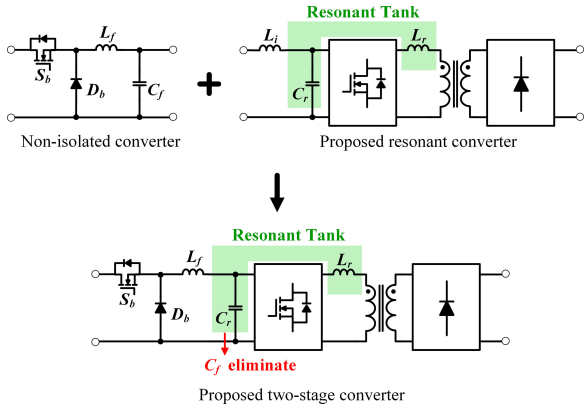

Fig. 12. Concept of the proposed two-stage converter.

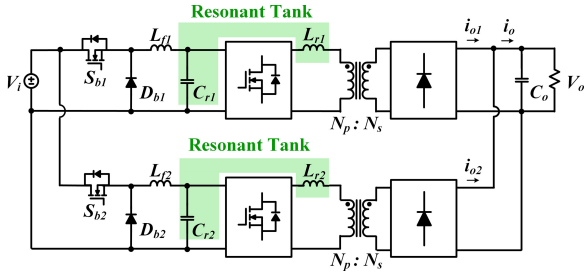

Fig. 13. Proposed PIPO interleaved converter.

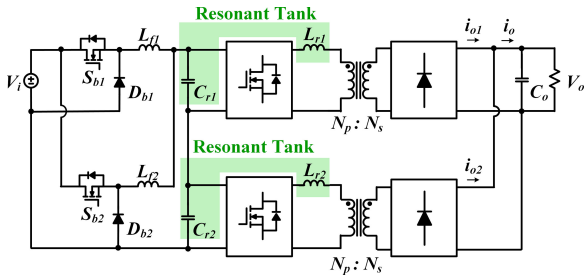

Fig. 14. Proposed SIPO interleaved converter.

conventional and proposed two-stage converters using a buck converter as a nonisolated converter, respectively. It is seen from Fig. 11 that filter capacitor C_f of the nonisolated converter and input capacitor C_i of the conventional resonant converter are combined into single capacitor $C_{\rm dc}$ in the two-stage converter that is comparatively large since the voltage ripple of the capacitor should be small. In the meanwhile, it is seen from Fig. 12 that filter capacitor C_f of the nonisolated converter is eliminated, and filter inductor L_f of the nonisolated converter and input inductor L_i of the proposed resonant converter are combined into single inductor L_f in the two-stage converter. Note that resonant capacitor C_r in the proposed two-stage converter does not need to be large since it is used only as a resonant capacitor. Figs. 13 and 14 show the proposed interleaved two-stage converters with parallel input and parallel output (PIPO) structure and series input and parallel output (SIPO) structure, respectively.The PIPO interleaved converter is better suited to relatively low-input voltage application, while SIPO interleaved converter is better suited to relatively high-input voltage application. The PIPO converter is more vulnerable to current unbalance caused by resonant component tolerances, parasitic component of each converter. Instead, the current unbalance can be alleviated by controlling each of the nonisolated stage of the PIPO converter. On the other hand, the SIPO converter is immune to current unbalance caused by resonant component tolerances due to inherent charging balance of two resonant capacitors [21], [22].

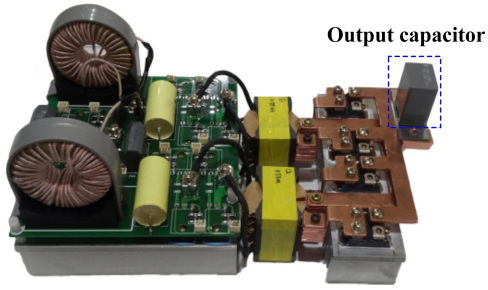

Fig. 15. Photograph of a 2-kW prototype of the proposed converter.

III. Experimental Results

A 2-kW prototype of the proposed interleaved converter has been built and tested to verify the operating principle, and the experimental results are provided. The system specification used in the experiment is as follows: $P_o = 2$ kW, $V_i = 200$–400 V, $V_o = 12$ V, $N_p : N_s = 7 : 1$, $f_{\rm s\_buck} = 20$ kHz, $f_r = 133$ kHz, $D_d T_s = 100$ ns, $L_{f1,2} = 560$ μH, $L_r = 3\mu$H, $C_r = 0.47$ μF, and $C_o = 110$ μF.

Switches in nonisolated are implemented with IXKH47N60C (600 V, 47 A, and 65 mΩ) MOSFET, and switches in isolated stages are implemented with IRFP4668 (200 V, 130 A, and 9.7 mΩ) MOSFET, and diodes in the isolated stage are implemented with IXFN520N075T2 (75 V, 200 A, and 1.9 mΩ) MOSFET for synchronous rectification. Filter inductors of each phase are implemented with powered cores CH571125 from Changsung. Transformers of each phase are implemented with ferrite cores PQ50/50 from TDK. Required output capacitance and ripple current of the output capacitor of the proposed converter were obtained to be 78 μF and 4 A, respectively, by simulation considering dead time of the switches and tolerance of the resonant components. Considering proper margin, film capacitor FFB54D0117KJC with capacitance of 110 μF and ripple current of 10 A was chosen from AVX. Calculated output capacitance and ripple current of the output capacitor of the interleaved SRC are 250 μF and 25.2 A, respectively. Considering margin, two film capacitors FFB34D0137K with capacitance of 130 μF and ripple current of 22 A, each can be chosen from AVX for comparison. This means that the output capacitor volume of the proposed converter is only 1/5 compared to that of the interleaved SRC. The photograph of the prototype of the proposed converter is shown in Fig. 15. It is seen from Fig. 15 that

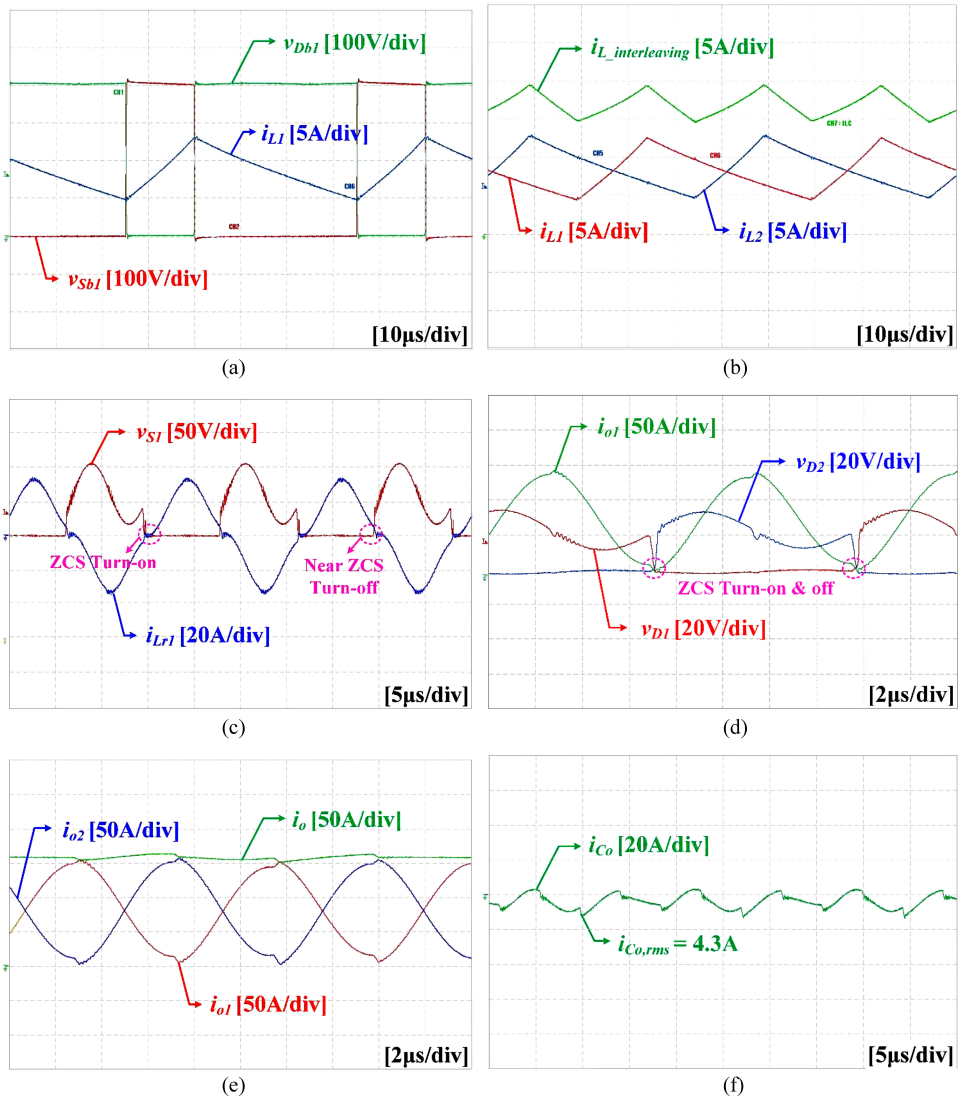

Fig. 16. Experimental waveforms at full load. (a) Switch voltage v_{Sb1} and diode voltage v_{Db1} and inductor current i_{L1}. (b) Inductor current i_{L1}, i_{L2}, and interleaving current $i_{\mathrm{L\_interleaving}}$. (c) Switch voltage v_{S1} and resonant current i_{Lr1}. (d) Diodes voltage $v_{\mathrm{D1,2}}$ and rectified current i_{o1}. (e) Rectified current i_{o1}, i_{o2}, and interleaved output current i_o. (f) Ripple current of output capacitor.

volume of the output capacitor is very small. Fig. 16 shows key experimental waveforms of the proposed converter at full load. Fig. 16(a) shows waveforms of the switch and diode voltages and the filter inductor current of the nonisolate stage. Fig. 16(b) shows waveforms of each inductor current and interleaved inductor current of the nonisolated stage. Fig. 16(c) and (d) shows waveforms of the switch voltage and resonant current and the diode voltage and output current of a phase, respectively, of the isolated stage. It is seen that all switches and diodes are turned ON and OFF under ZCS condition. Fig. 16(e) shows waveforms of the output currents of each phase and the interleaved output current. Fig. 16(f) shows the ripple current of the output capacitor, which is only 4.3A in rms value. The ripple current of the output capacitor of the proposed converter should not exists in theory, but in practice small amount of ripple current exists due to dead time of the switches and tolerance of the resonant components. Fig. 17 shows the measured efficiency

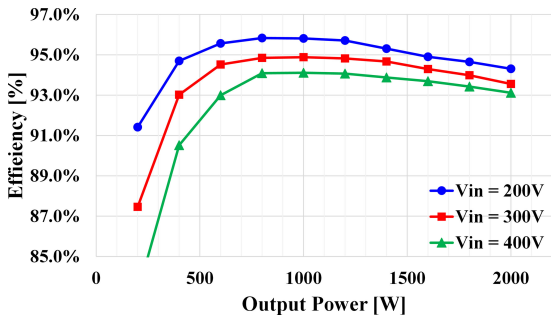

Fig. 17. Measured efficiency of the proposed two-stage interleaved converter.

using YOKOGAWA WT3000. The maximum efficiency is 95.9% at 0.9kW and full load efficiency is 94.3%, respectively, when input voltage is 200 V.

IV. Conclusion

This paper proposes a new two-stage interleaved current-fed resonant converter. The current-fed resonant converter achieves ZCS turn-on and turn-off for all switches and diodes, and has zero *di/dt* at turn-off of diodes when operated at load independent points. Interleaved operation of the current-fed resonant converter has theoretically zero output filter capacitance, resulting in significantly reduced volume of the output capacitor. A two-stage power conversion technique is applied to the interleaved converter for high efficiency under wide voltage range operation. A 2-kW prototype of the proposed converter has been built and tested to verify the validity of the proposed operation. The maximum efficiency is 95.9% at 0.9 kW and full load efficiency is 94.3%, respectively, when input voltage is 200 V. The proposed converter could be a possible option for the LDC of EV and HEV.

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Dongok Moon received the B.S. degree from the Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul, Korea, in 2013, where he is currently working toward the M.S. degree.

His research interests include dc–dc converter and battery charger for electric vehicles.

Junsung Park (S'13) received the B.S. and M.S. degrees from the Seoul National University of Science and Technology (Seoul Tech), Seoul, Korea, in 2009 and 2011, respectively. He is currently working toward the Ph.D. degree at the Power Electronics and Fuel Cell Power Conditioning Laboratory, Seoul Tech.

His research interests include high power dc–dc converter for electric vehicles and renewable energy systems.

Sewan Choi (S'92–M'96–SM'04) received the B.S. degree in electronic engineering from Inha University, Incheon, Korea, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from Texas A&M University, College Station, TX, USA, in 1992 and 1995, respectively.

From 1985 to 1990, he was with Daewoo Heavy Industries as a Research Engineer. From 1996 to 1997, he was a Principal Research Engineer at Samsung Electro-Mechanics Co., Korea. In 1997, he joined the Department of Electrical and Information Engineering, Seoul National University of Science and Technology (Seoul Tech), Seoul, Korea, where he is currently a Professor. His research interests include power conversion technologies for renewable energy systems and dc–dc converters and battery chargers for electric vehicles.

Dr. Choi is an Associate Editor of the IEEE Transactions on Power Electronics and the IEEE Transactions on Industry Applications.