A 12-Bit 1.6, 3.2, and 6.4 GS/s 4-b/Cycle Time-Interleaved SAR ADC With Dual Reference Shifting and Interpolation

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Abstract—This paper demonstrates a multi-bit/cycle successive-approximation register (SAR) analog-to-digital converter (ADC) architecture for low-power and high-speed operation. The proposed dual reference shifting and interpolation technique reduces the power and area overhead of the multi-bit/cycle SAR architecture, allowing for a higher number of bit quantization for each conversion cycle and thus, a higher conversion rate. To prove the concept, a 12-bit 32-way time-interleaved 4-b/cycle SAR ADC prototype is fabricated in 65-nm CMOS technology. The ADC prototype can be configured with multiple sampling rates (1.6, 3.2, and 6.4 GS/s). It measures a peak effective number of bits (ENOB) of 10.9 bits at 6.4 GS/s and 9.4 ENOB at the maximum input frequency of 1 GHz. The prototype achieves a Schreier figure-of-merit (FOM$_{Schreier}$) of 154.9 dB at 6.4-GS/s sampling rate.

Index Terms—CMOS, multi-bit/cycle, Successive-approximation register analog-to-digital converter (SAR ADC), switched-capacitor circuit, time-interleaved (TI) ADC.

I. INTRODUCTION

THE emerging trend of high-throughput and flexible communication systems demands a high-speed analog-to-digital converter (ADC) to quantize a wide spectrum with the highest possible dynamic range [1]–[3] but at a reasonable cost. The achievable ADC resolution typically degrades with increasing signal bandwidth mainly due to clock jitter constraint and the ADC implementation itself. The objective of this paper is to minimize the cost of a high-speed high-resolution ADC implementation such that it is mostly limited by the clock jitter performance. For very high sampling speed operation, a time-interleaved (TI) topology is commonly adopted to scale up the sampling rate of a single ADC in a given technology and architecture [4]–[14]. However, parallelizing a number of ADC channels increases the burden of the input and the clock network, in addition to the necessity

to overcome the mismatch and sampling phase imbalance in between ADCs that further incurs implementation overhead. Therefore, it is important to maximize the sampling speed of a single ADC such that fewer and energy-efficient ADC channels are required. In this paper, we explore such ADC architecture without pipelining for better energy efficiency.

We aim to achieve >10 ENOB with >GHz signal bandwidth and at the same time, minimize the power consumption as much as possible in 65-nm standard CMOS technology. To achieve this goal, we propose an area- and power-efficient 4-bit/cycle successive-approximation register (SAR) architecture, targeting 12-bit resolution and >200 MS/s. We also apply various circuit and layout level techniques to maximize the bandwidth of the interleaved sampling network. A fine clock skew tuning mechanism is deployed to correct for the sampling phase imbalance between the 32 interleaved ADC channels. In the proof-of-concept prototype, the ADC achieves an effective number of bits (ENOB) of 10.9 and 9.4 for an input frequency of 24 MHz and 1 GHz, respectively, at 6.4 GS/s with a total power consumption of 225 mW, excluding external reference voltage drivers, I/O buffers, and inter-channel foreground calibration circuits (one-time operation). By enabling the number of ADC channels, the overall sampling rate can support different modes: 1.6, 3.2, and 6.4 GS/s.

This paper is organized as follows. Section II introduces the operation principle of the proposed dual reference shifting and interpolation (DRSI) technique and its advantages over the conventional multi-bit SAR architecture. Section III analyzes various non-idealities unique in the proposed dual-path ADC architecture, including offset and gain errors between the paths. Section IV describes the implementation details of the ADC. The measurement results are presented in Section V, followed by the conclusion in Section VI.

II. PRINCIPLE OF OPERATION

A. Existing Multi-Bit/Cycle SAR Topologies

One common approach to increase the speed of an SAR ADC is to quantize the analog residue voltage on more discrete levels in each SAR conversion cycle, which is also known as the multi-bit per cycle SAR algorithm [15]–[18]. It reduces the required number of SAR conversion cycles to complete the bit trials by a factor of M, assuming an M-bit per cycle SAR ADC is used. The mathematical operation of a particular
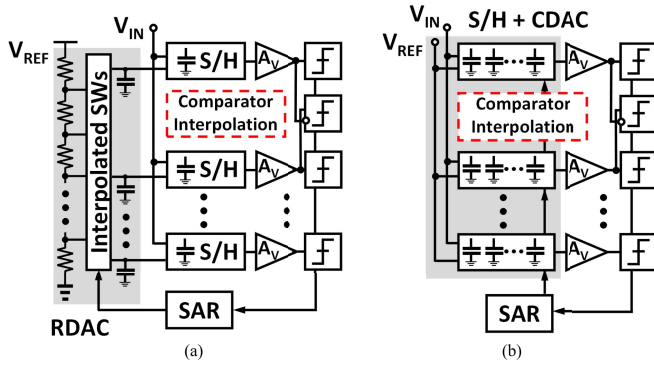
Fig. 1. Conventional multiple S/H based M-bit/cycle SAR ADC with (a) RDAC and (b) CDAC.
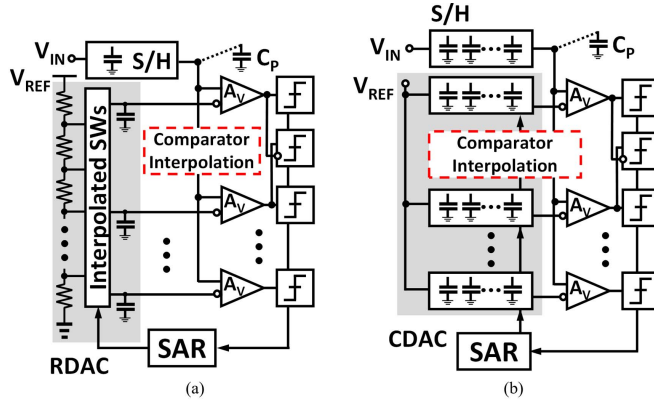
Fig. 2. Single S/H-based M-bit/cycle SAR ADC with (a) RDAC and (b) CDAC.

TABLE I
COMPARISON OF THE REQUIRED CAPACITANCES FOR M-BIT/CYCLE SAR ADC TOPOLOGIES

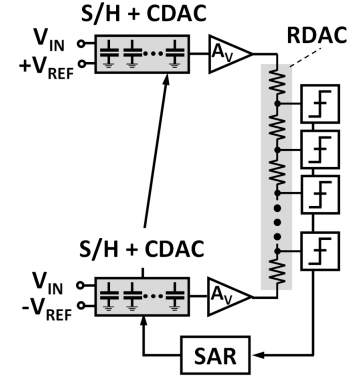| Topology Required capacitance	Conventional Multiple S/H		Single S/H		This work Fig. 3
	RDAC Fig.1 (a)	CDAC Fig.1 (b)	RDAC Fig.2 (a)	CDAC Fig.2 (b)	
Capacitance for signal path	$\alpha \cdot 2^{M-1}$	*2^{M-1}	α	2	*2
Capacitance for reference path	$\left(\dfrac{\alpha}{\alpha-1}\right) \cdot 2^{M-1}$		$\left(\dfrac{\alpha}{\alpha-1}\right) \cdot 2^{M-1}$	2^M	
Total capacitance	$\left(\dfrac{\alpha^2}{\alpha-1}\right) \cdot 2^{M-1}$	2^{M-1}	$\dfrac{\alpha \cdot (\alpha-1+2^{M-1})}{\alpha-1}$	$2+2^M$	2

Fig. 3. Proposed DRSI M-bit/cycle SAR ADC.

cycle with a full-scale range of $\pm V_{\text{REF}}$ can be expressed as

$$D_{\text{Conv}} = \sum_{k=1}^{2^M-1} \text{sign}[V_{\text{RES}} - V_{\text{TH},k}] \qquad (1)$$

$$= \sum_{k=1}^{2^M-1} \text{sign}[V_{\text{RES}} + (2\lambda_k - 1) \cdot V_{\text{REF}}] \qquad (2)$$

where D_{Conv} is a digital thermometer code for the residue voltage (V_{RES}), and λ_k is the interpolation coefficient for the kth reference voltage ($\lambda_k = k/2^M$, $k \in \{1, 2, \cdots, (2^M - 1)\}$). Figs. 1 and 2 show general approaches for implementing (2), which are typically composed of sample-and-hold (S/H), reference digital-to-analog converters (DACs), and comparators. For comparison purposes, we divide the approaches into two categories: the first category uses 2^{M-1} S/H (Fig. 1), while the second category uses single S/H (Fig. 2). In each category, the reference DACs can be implemented in either a resistive or capacitive array, assuming the comparator interpolation technique is used. Next, we examine the minimum required capacitance values in the signal and reference paths, i.e., S/H and DAC, as they indicate the potential area and power consumption, as well as the ADC input driver's constraint.

Table I summarizes the results of the required capacitances of each M-bit/cycle SAR topology given a target kT/C noise and speed specification. As an example, for resistive reference DAC (RDAC) topologies, we consider the required capacitance

in S/H and the RDAC for sufficient thermal noise filtering while minimizing the associated area and power consumption. To satisfy the noise requirement, $kT/C_S + kT/C_R$ should be less than $kT/C_{\min}$, where C_S and C_R are the capacitances in the S/H and RDAC circuits, and $kT/C_{\min}$ is the target sampled noise level. It suggests that

$$C_R > \frac{\alpha}{\alpha-1} \cdot C_{\min}, \text{ if } C_S = \alpha \cdot C_{\min} \qquad (3)$$

where α is the capacitor weighting factor ($\alpha > 1$) of C_S against $C_{\min}$.

Moreover, to meet the RDAC settling requirement [0.5 least significant bit (LSB) settling error], the worst case scenario should be considered and bounded within the SAR conversion cycle time ($T_{1cyc.SAR}$), yielding the following design constraint:

$$R_{\text{REF}} \le \frac{4 \cdot T_{1cyc.SAR}}{C_R \cdot (N+1) \cdot \ln 2} R_{\text{REF}} \le \frac{4 \cdot T_{1cyc.\,SAR}}{C_R \cdot (N+1) \cdot \ln 2} \qquad (4)$$

where N are the target ADC resolution, and the switch resistance is assumed to be negligible compared with the total resistance of the RDAC ladder (R_{REF}). As for the capacitive reference DAC (CDAC) topologies, their sizing is mainly determined by the kT/C noise constraint. In most cases, C_S and C_R need to be sized greater than $C_{\min}$ to satisfy the final SNR requirement, as summarized in Table I. In a nutshell, we can observe that either the C_S or C_R capacitance scales exponentially with the factor M in any of the existing topologies, which prevents them from higher speed operation as the implementation cost would become excessively high.
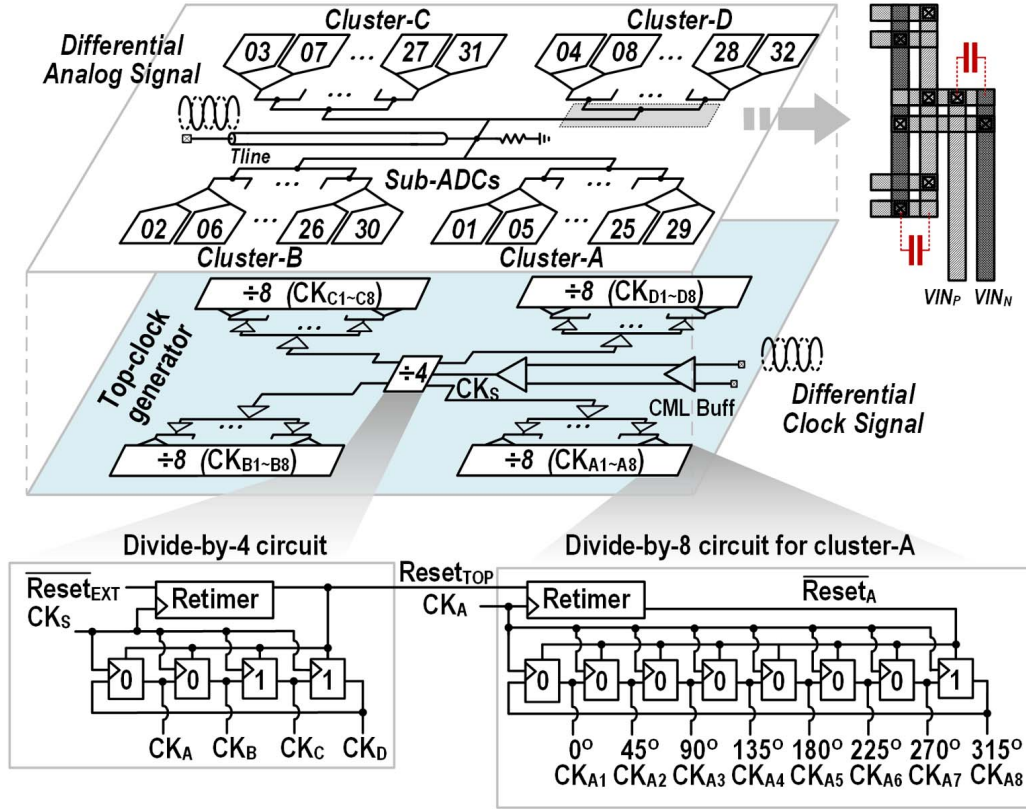
Fig. 4. Proposed 32-way TI-ADC architecture.

B. Proposed Dual Reference Shifting and Interpolation

To reduce the implementation cost of M-bit/cycle SAR architecture, we propose to rearrange (1) and (2) by introducing two variables, $V_{\text{UP}} = V_{\text{RES}} + V_{\text{REF}}$ and $V_{\text{DN}} = V_{\text{RES}} - V_{\text{REF}}$, and then linearly interpolating between the two into $(2^M - 1)$ decision levels, as shown as follows:

$$D_{\text{DRSI}} = \sum_{k=1}^{2^M-1} \text{sign}[V_{\text{Comp},k}] \tag{5}$$

$$= \sum_{k=1}^{2^M-1} \text{sign}[\lambda_k \cdot V_{\text{UP}} + (1 - \lambda_k) \cdot V_{\text{DN}}] \tag{6}$$

$$= \sum_{k=1}^{2^M-1} \text{sign}[V_{\text{RES}} + (2\lambda_k - 1) \cdot V_{\text{REF}}] \tag{7}$$

where D_{DRSI} is a digital thermometer code for given V_{RES} in the proposed DRSI architecture. There are several implementation advantages in using the form of (6), as conceptually illustrated in Fig. 3. First, it utilizes only two S/Hs to sample the analog input and add or subtract V_{REF} via charge redistribution, regardless of the M value. As the sampling noise (kT/C) from the two S/H networks is also interpolated, the sampling capacitance does not need to be increased as in some prior M-bit/cycle SAR architectures; i.e., C_S can be kept as small as C_{min}. This architecture allows better scalability toward higher bit quantization in each SAR cycle. Second, the S/H in conventional single S/H M-bit/cycle topologies

(Fig. 2) is loaded with $(2^M - 1)$ comparators, where pre-amplifiers cannot be shared. In the proposed DRSI scheme, two pre-amplifiers can be shared and inserted after S/H to amplify V_{UP} and V_{DN}, respectively, for reducing the noise, kickbacks, and loadings from the comparators. The gain and offset requirements of these pre-amplifiers are analyzed in Section III. Third, because the input is effectively subtracted from the corresponding reference voltage after interpolation, the comparator needs to detect only the zero-crossing point of the interpolated voltages. It allows the comparator to work in the highest gain region. Finally, although an interpolation resistor network is still needed in the proposed DRSI at the pre-amplifier outputs, it does not consume static current unlike the conventional RDAC.

In short, the proposed DRSI architecture eliminates the exponential dependence on factor M while relaxing the ADC input driver requirement, as summarized in Table I. This architecture provides a more efficient implementation for a high-speed and high-resolution SAR ADC.

III. NON-IDEALITY ANALYSES OF DRSI

As DRSI is composed of dual paths for shifting up and down the reference voltage, we analyze the impact of mismatch between the paths and derive the tolerance.

A. Gain Error

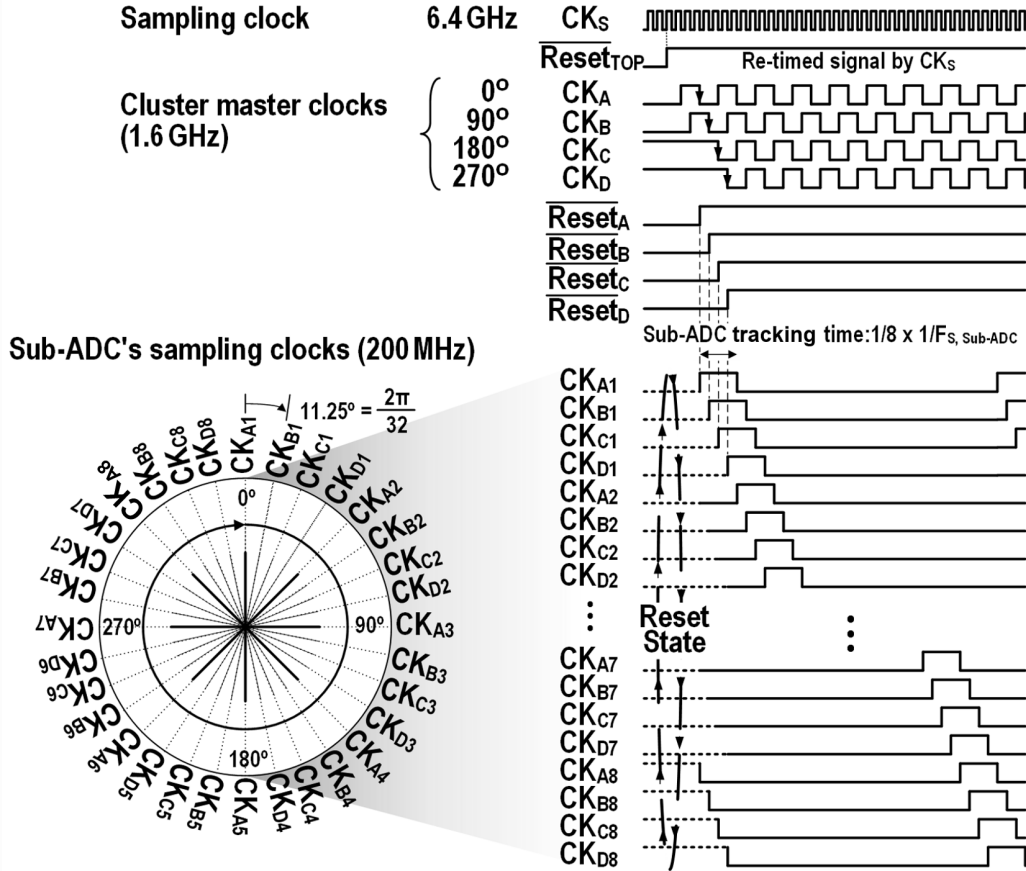We first analyze the gain errors, which mainly result from the two separate S/H and pre-amplifiers. Assuming

Fig. 5. Timing diagram of multi-phase clocks used in TI-ADC.

the gain from each path is G_{UP} and G_{DN} while the ideal gain should be G_i, we define a differential mode gain error, ΔG, where $G_{\mathrm{UP}} = G_i + \Delta G/2$ and $G_{\mathrm{DN}} = G_i - \Delta G/2$. Here, the common-mode gain error is not considered because it effectively changes the value of G_i. Given that, the interpolated value for each decision level ($V_{\mathrm{Comp},k}$) can be expressed as

$$V_{\mathrm{Comp},k} = G_{\mathrm{UP}} \cdot \lambda_k V_{\mathrm{UP}} + G_{\mathrm{DN}} \cdot (1 - \lambda_k) \cdot V_{\mathrm{DN}}. \quad (8)$$

A local ($V_{\mathrm{err}G,k}$) offset voltage caused by ΔG can be found by rearranging (8)

$$V_{\mathrm{Comp},k} = G_i \cdot \{V_{\mathrm{RES}} + (2\lambda_k - 1) \cdot V_{\mathrm{REF}} + V_{\mathrm{err}G,k}\} \quad (9)$$

$$V_{\mathrm{err}G,k} = \frac{\Delta G}{2G_i}\{V_{\mathrm{REF}} + (2\lambda_k - 1) \cdot V_{\mathrm{RES}}\} \quad (10)$$

$$\max[V_{\mathrm{err}G,k}] = V_{\mathrm{err}G,k}|_{V_{\mathrm{RES}}=V_{\mathrm{REF}}, \lambda_k=1-1/2^M}$$
$$\text{or} \quad V_{\mathrm{err}G,k}|_{V_{\mathrm{RES}}=-V_{\mathrm{REF}}, \lambda_k=1/2^M}. \quad (11)$$

We can observe that $V_{\mathrm{err}G,k}$ is input and decision-level dependent, and the largest error occurs at the very top and bottom of decision levels for the maximal input, as indicated in (11). Given the built-in conversion redundancy in this paper, we limit the worst case gain error within a half LSB for each SAR conversion cycle (i.e., max $V_{\mathrm{err}G,k} < 0.5$ LSB). By applying (10) and (11), we can then derive the following expression:

$$\frac{\Delta G}{G_i} \leq \left(\frac{1}{2^M - 1}\right). \quad (12)$$

In this prototype, we design the gain error ($\Delta G/G_i$) to be less than 5%, which is ensured via careful matching and gain calibrations. Note that the pre-amplifier's integral non-linearity (INL) has a similar effect in introducing the error term similar to (9). Therefore, we adopt complementary input pairs to avoid a non-linear gain variation during the signal excursion, which will be elaborated in Section IV-C2.

B. Offset Error

We now analyze the offset mismatch of the dual paths. Similar to the gain error analysis, the output referred offset error at the interpolator output can be expressed as follows:

$$V_{\mathrm{Comp},k} = G_i \cdot \begin{cases} \lambda_k \cdot \left(V_{\mathrm{UP}} + \dfrac{V_{\mathrm{OS,cm}} + V_{\mathrm{OS,diff}}}{2}\right) \\ +(1 - \lambda_k) \cdot \left(V_{\mathrm{DN}} + \dfrac{V_{\mathrm{OS,cm}} - V_{\mathrm{OS,diff}}}{2}\right) \end{cases} \quad (13)$$

where $V_{\mathrm{OS,cm}}(= V_{\mathrm{OS,UP}} + V_{\mathrm{OS,DN}})$ and $V_{\mathrm{OS,diff}}(= V_{\mathrm{OS,UP}} - V_{\mathrm{OS,DN}})$ are defined as common and differential mode offset errors, respectively. Rearranging (13) shows the relationship between the offsets and the reference level discrepancy

$$V_{\mathrm{Comp},k} = G_i \cdot \{V_{\mathrm{RES}} + (2\lambda_k - 1) \cdot V_{\mathrm{REF}} + V_{\mathrm{errOS},k}\} \quad (14)$$

$$V_{\mathrm{errOS},k} = \frac{V_{\mathrm{OS,cm}}}{2} + (2\lambda_k - 1) \cdot \frac{V_{\mathrm{OS,diff}}}{2}. \quad (15)$$

In contrast to the gain errors, (14) and (15) show both common and differential mode offset errors contribute to a
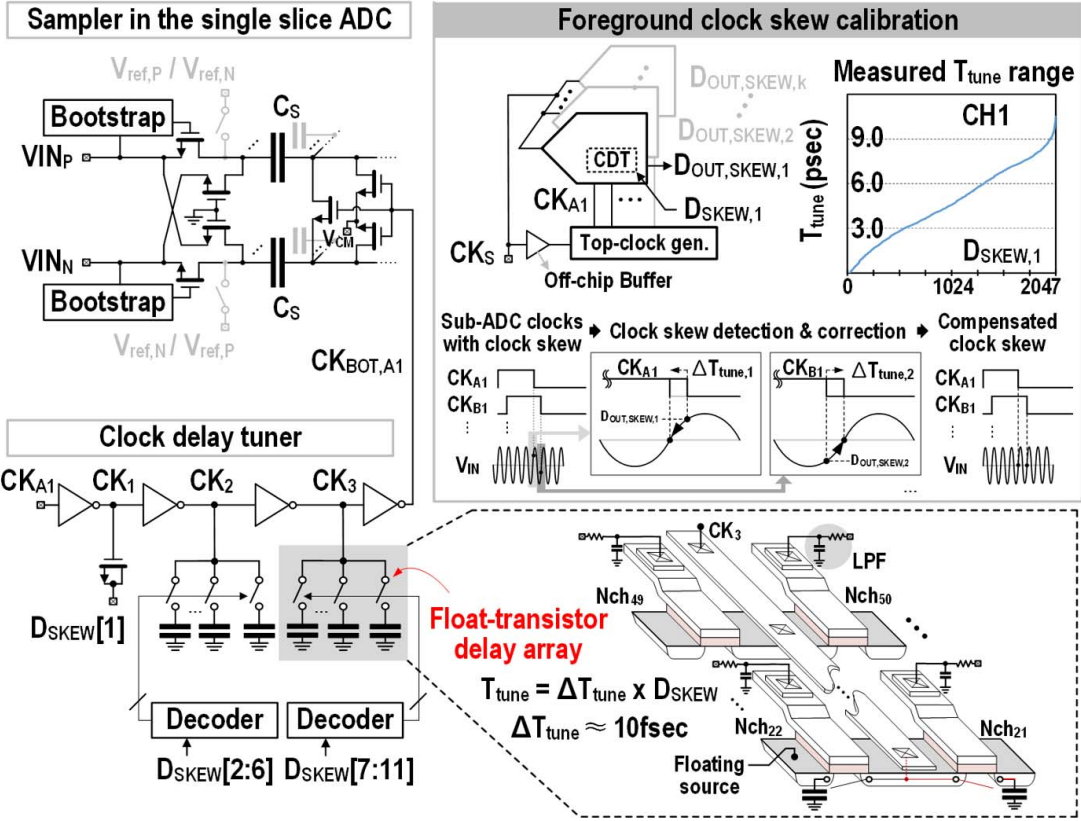
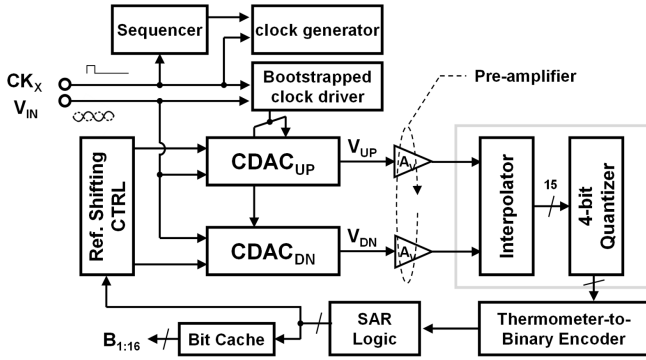Fig. 6. TI-ADC sampling network and clock skew calibration.

Fig. 7. Block diagram of the proposed SAR ADC with DRSI implementation.

decision error. Therefore, in order to suppress the conversion error less than 0.25 LSB at the target N-bit ADC resolution, the offsets should satisfy the following inequality:

$$V_{\text{errOS},k} \leq \frac{V_{\text{REF}}}{2^{N+1}}. \tag{16}$$

According to (16), the offset tolerance is more stringent than that of the gain error, because the offset margin for an N-bit ADC is ultimately defined by the last conversion stage. In this paper, we design an offset calibration circuit at each pre-amplifier to compensate the worst case input referred offset errors $((V_{\text{OS,cm}}/2) \pm (V_{\text{OS,diff}}/2))$, i.e., $V_{\text{OS,UP}}$ or $V_{\text{OS,DN}}$, less than 200 μV.

IV. CIRCUIT IMPLEMENTATION

A. 32-Way Time-Interleaved ADC Architecture

To increase the sample rate, this prototype time interleaves up to 32 SAR ADC channels. Since the resolution of the SAR ADC aims at >10 ENOB, the sampling capacitance is relatively large compared to an ADC with moderate resolution (6–8 bit), which can severely degrade the input tracking bandwidth in a TI topology. To mitigate this loading effect, we divide the interleaved ADCs into four clusters and stagger the sampling sequence among the clusters, as shown in Fig. 4. Only one ADC channel from each cluster tracks with the input voltage for the time duration of 625 ps; as a result, the ADC input is loaded with a total of four sampling capacitors at any given time. In order to achieve a linear input sampling network, we adopt a purely passive network via designing a differential transmission line with on-chip 50-Ω termination to mitigate the capacitive loading effect of the long-distance routing. Additionally, since a load impedance of each ADC channel in both sampling and hold mode is much higher than on-chip termination resistor, the kick-back charge is mostly dissipated through the termination resistor. Furthermore, as adjacent sampling events are located in different clusters (which are physically far apart as shown in Fig. 4 and die photograph), the kick-back charge should pass through the termination resistor first. Thus, it further helps to isolate the kick-back effect between ADC channels.
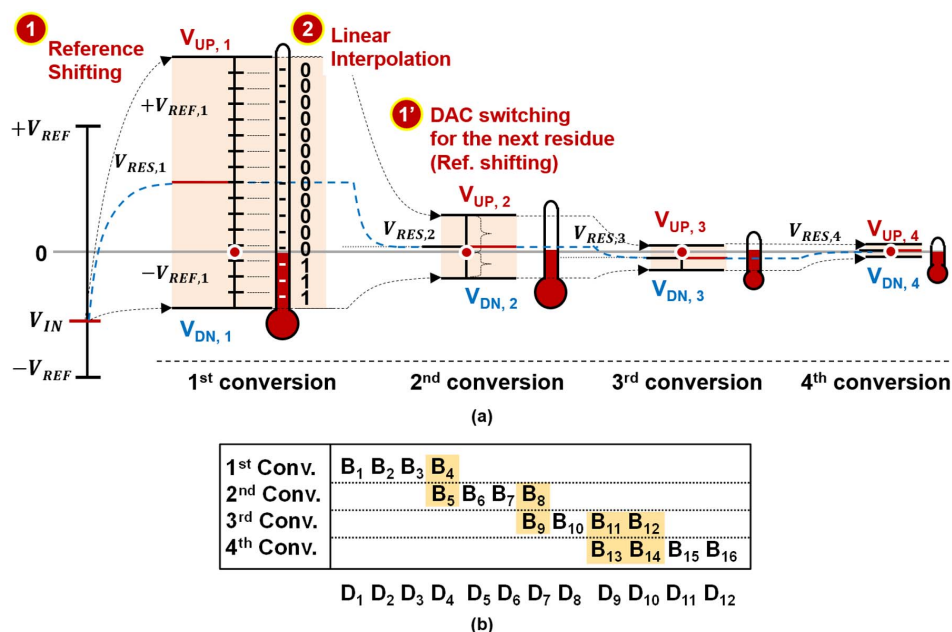
Fig. 8.   (a) Timing diagram of the proposed SAR conversion cycles. (b) Implemented conversion redundancy.
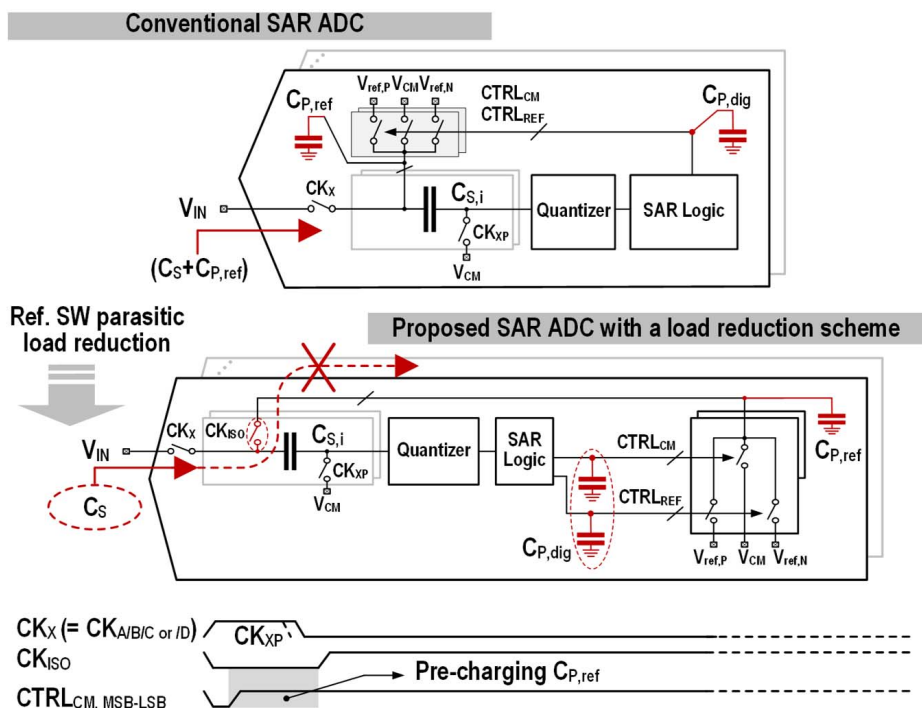

Fig. 9.   Load reduction scheme in the S/H.

Regarding the layout strategy to accommodate the large ADC array, the routings of the differential input signal are placed in a way that the mutually coupled parasitic capacitance is reduced (illustrated in Fig. 4), leading to wider routing bandwidth. In order to minimize the sampling clock skew between ADC channels, the input and clock signals should ideally be routed side by side; however, the mutual coupling can cause sampling phase disturbance and clock feedthroughs to ADC inputs, causing signal-to-noise ratio (SNDR) degradations. Therefore, we insert additional metal traces to shield between input and clock signals, and tie it with a cleaner ground domain to suppress the cross talks.

B. Global Clock Generation and Distribution

1) Multi-Phase Clock Generator: A 6.4-GHz external clock source is brought to the center of the chip via differential signaling and current-mode logic (CML) for better power supply noise rejection. Also, we use on-chip ac coupling capacitor with differential clock signal to mitigate the common-mode
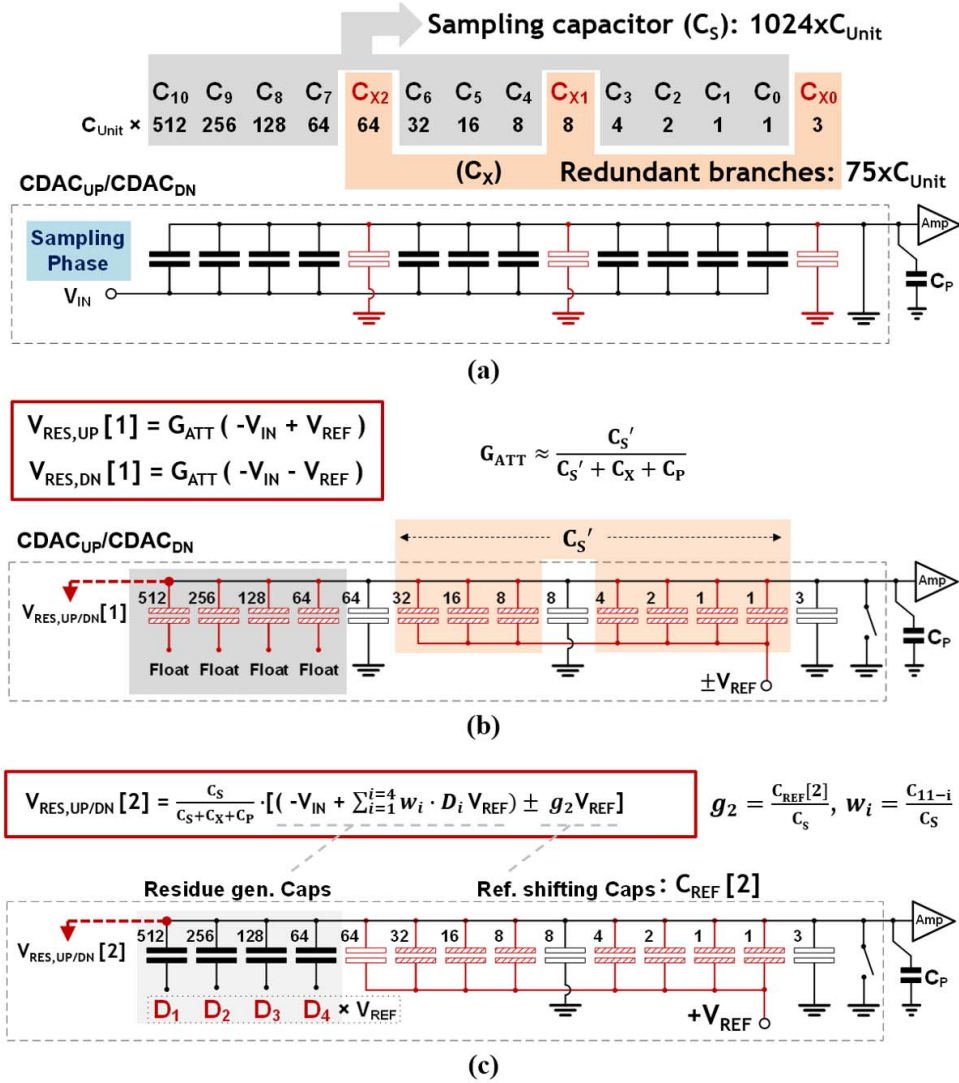
Fig. 10. Proposed CDAC operation in (a) sampling phase and (b) first and (c) second SAR conversion cycle.

interference between off-chip and on-chip ground. Furthermore, we occupy about 0.3-mm^2 active area for deploying decoupling capacitors with an isolation from other power domains. To perform frequency division, the differential clock is first converted into single end and then divided by four with low-noise true-single-phase-clock (TSPC) flip-flops. The four divided clock phases are routed to each ADC cluster using a tree structure to minimize the deterministic clock skew. The second clock divider generates eight phases by placing each TSPC near the corresponding ADC channel and forms a ring-based divider to reduce the overall clock routing and facilitate a well-balanced layout. With proper clock buffering (6-stage inverter), we ensure sharp clock transition edges throughout the clock path. Note that the external asynchronous reset signal (Reset$_{TOP}$) is first re-timed with the 6.4-GHz clock (Reset$_{A/B/C/D}$ in Fig. 5) and later re-timed with the local clock in each cluster, in order to ensure synchronous operation of the distributed clock dividers, as illustrated in Fig. 5.

2) Sampling Clock Skew Calibration: Despite the efforts to balance the sampling clock phase in clock generation and distribution, manufacturing variability may still introduce clock skews, requiring extra compensation. Fig. 6 illustrates the schematic of the proposed clock delay tuner (CDT) circuit and calibration routine. We insert three delay stages in the sampling clock path of the bottom plate switches, and each stage is composed of inverters, digitally controlled capacitive loads, decoders, and *R–C* filters to reduce the noise disturbance to the switches. For coarse delay tuning, we simply turn a minimum-sized MOS varactor ON and OFF. However, for fine delay adjustment (on the order of 10 fs), we propose to turn floating transistors ON and OFF without attaching a physical capacitor. As the parasitic capacitance at the drain or source terminal of the floating transistors between OFF and the triode mode is roughly $W \cdot L \cdot C_{OX}$, changing the dimensions of the transistor can provide a sufficiently small capacitance difference, and thus leads to a fine delay variation. Note that there exists a junction capacitance at the drain or source terminals and that can degrade the delay tuning capability. To minimize this unwanted junction capacitance, we share the active area of the floating transistors in the layout.
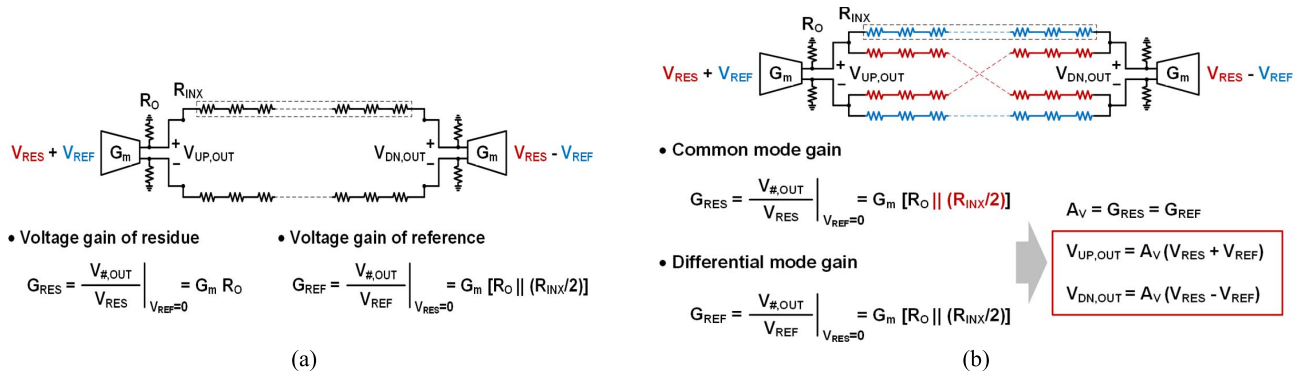
Fig. 11. Voltage gains of residue and reference path (a) without and (b) with the proposed cross-coupled resistor ladder network.
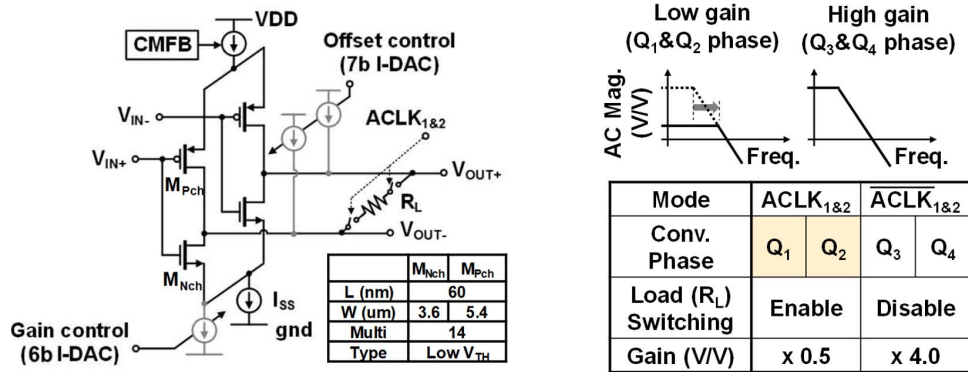

Fig. 12. Proposed implementation of the G_m-cell with dual-mode operation scheme.

Detection of actual clock skew is performed in the foreground where the sampling clock is reused as the ADC input. Because each ADC channel operates at a sub-harmonic frequency of the sampling clock, the sampled voltage should be a dc value. As the slew rate of a sinusoid is highest around the zero-crossing point, we first adjust the input align the relative phase between the ADC input and the sampling clock accordingly. This is achieved by monitoring the first ADC channel's output while adjusting the phase of input sinusoid via external delay tuner. As a result, a small change in the sampling clock phase results in a larger dc voltage offset. We then leverage this property and cycle through the clock skew tuning bits until the sampled dc voltages (averaging over a few thousand samples to reduce noise impact) of all ADC channels are closely matched, suggesting that the sampling clock phases are more balanced. The measured clock tuning range is about 10 ps with a resolution of about 10 fs (the delay tuning profile plotted in Fig. 6), and the corresponding harmonic tone at the ADC output is improved by about 30 dB after the calibration routine, which is elaborated in Section V.

C. SAR Implementation

As shown in Fig. 7, the SAR ADC consists of two capacitor DACs ($CDAC_{UP}$ and $CDAC_{DN}$) to perform DRSI operations via signal sampling and reference shifting, while two shared pre-amplifiers are used to enlarge the CDAC outputs instead of individual pre-amplifiers in front of all the comparators. The outputs of the pre-amplifiers are further interpolated, quantized, and decoded for SAR logics. Note that a bootstrapped sampling switch is used for better linearity, and a clock generator creates all the required clock phases. In order to enhance a conversion speed further, the reference shifting controller would be eliminated by applying direct thermometer code from quantizer with non-binary weighted capacitor array [19]. However, it would not be efficient for higher resolution per conversion cycle SAR-based TI-ADC as enlarge CDAC interconnection reduces overall ADC input bandwidth.

To incorporate conversion redundancy, the ADC conducts four conversion cycles. Each conversion step first carries out reference shifting with residue generation followed by interpolation that quantizes the region into 16 equal voltage intervals, as illustrated in Fig. 8(a). Fig. 8(b) shows how the SAR ADC recombines the digital bits to accommodate previous stage conversion errors. Here, we can see that the size of the redundancy region is simply determined by the full-scale range of each conversion; i.e., 1-bit redundancy corresponds to a twice larger full-scale range. The range scaling is implemented via CDAC weighting, and more detailed configurations are described in Section IV-C1. Due to the lack of residue amplification as in a pipelined ADC, a 4-bit/cycle SAR ADC needs to reduce the reference range by eight times at every conversion to accommodate 1-bit redundancy among consecutive SAR conversions.

In the following sub-sections, the details of several key building blocks are described.
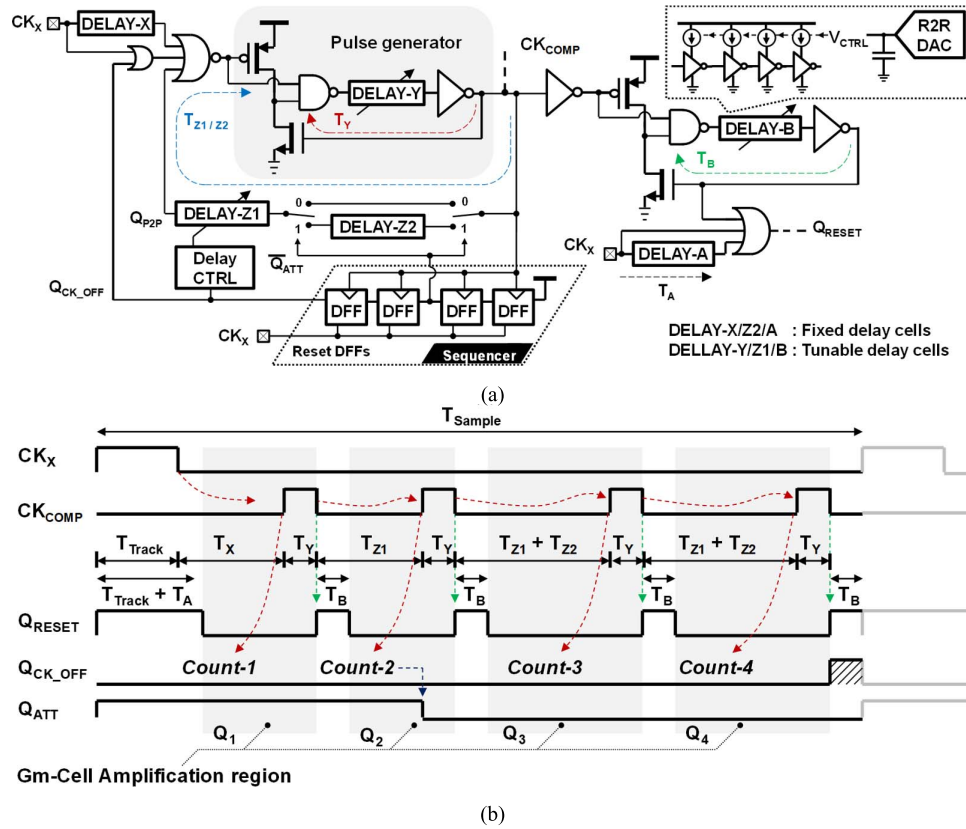
Fig. 13.   (a) Implementation of the single ADC clock generator. (b) Timing diagram of the single ADC.

1) Sampling CDAC Network: To maximize the signal bandwidth in a large-scale TI topology, it is crucial to reduce the capacitive loading from each SAR ADC. Therefore, we propose a reduced parasitic loading scheme in the S/H circuit while optimizing the SAR conversion speed, as shown in Fig. 9. Conventionally, the reference switches are physically placed close to the CDAC. In our design, because the CDAC network is relatively large due to the higher ENOB target, longer routings are created for the digital control bits and thus, larger parasitics ($C_{P,\text{dig}}$), which slow down the SAR conversion. Instead, we place those reference switches close to the SAR digital logic and insert a relatively small isolation switch close to the top plate of the sampling capacitors. During the S/H tracking phase, this isolation switch is OFF, preventing the parasitics ($C_{P,\text{ref}}$) from loading the ADC input; meanwhile, $C_{P,\text{ref}}$ is pre-charged to the common-mode voltage (V_{CM}) to reduce the enlarged settling time of the first SAR conversion cycle due to the switches connected in series. Note that the $C_{P,\text{ref}}$ value is about four times larger (mainly coming from routing parasitic) than the parasitic at the top and bottom plates of C_S. Although, the effect of pre-charging is reduced by a charge sharing, it is still helpful to pre-charge $C_{P,\text{ref}}$ with V_{CM}.

Fig. 10(a) shows more details of the CDAC network implementation. Each single-ended capacitor bank of CDAC$_{\text{UP}}$ and CDAC$_{\text{DN}}$ consists of 1024-unit cells to sample the input signal (V_{IN}) and 75-unit cells used to provide redundancy. In total, 4 capacitor banks ($\approx$1.42pF excluding parasitic capacitance) are used, occupying an active area of 0.03mm^2. The redundant cells are connected to V_{CM} during the sampling phase. In the first conversion phase right after the input sampling, the top

plates of the 1024-unit capacitor arrays are connected with positive reference voltage for CDAC$_{\text{UP}}$ and negative reference voltage for CDAC$_{\text{DN}}$. Thus, the sampled signal is level shifted upward and downward by the reference voltage, as required by (6). However, depending on the value of the sampled signal, the output voltages may go beyond the supply voltage rails in the first SAR conversion cycle and create unwanted operation conditions. Furthermore, a large signal swing typically introduces more distortion. Therefore, we intentionally attenuate the signal (230-mV$_{\text{PP}}$ differential signal swing after about seven times attenuation) by floating the first four MSB branches in the first cycle, as shown in Fig. 10(b). Note that some charge loss through the parasitics of the MSB branches are compensated via enlarged MSB capacitor sizing and built-in redundancy.

In the second conversion, the first four MSB branches are switched based on the first decision results, and the remaining LSB capacitors are switched to either positive or negative reference voltages to shift the residue voltage up or down by the intended full-scale range of the second SAR conversion cycle [Fig. 10(c)]. In other words, the reference shifting and residue voltage generation take place simultaneously via charge redistribution. We perform the remaining third and fourth conversion cycles using the same operation principles.

2) Pre-Amplifier and Resistive Interpolator: To perform 4-bit quantization, we share pre-amplifiers before the resistive interpolator and latches not only to save power but also to avoid the CDAC charge leakage path (shown in Fig. 3). Additionally, the provided gain can relax the noise requirement of the interpolators and the latches. According to the SPICE
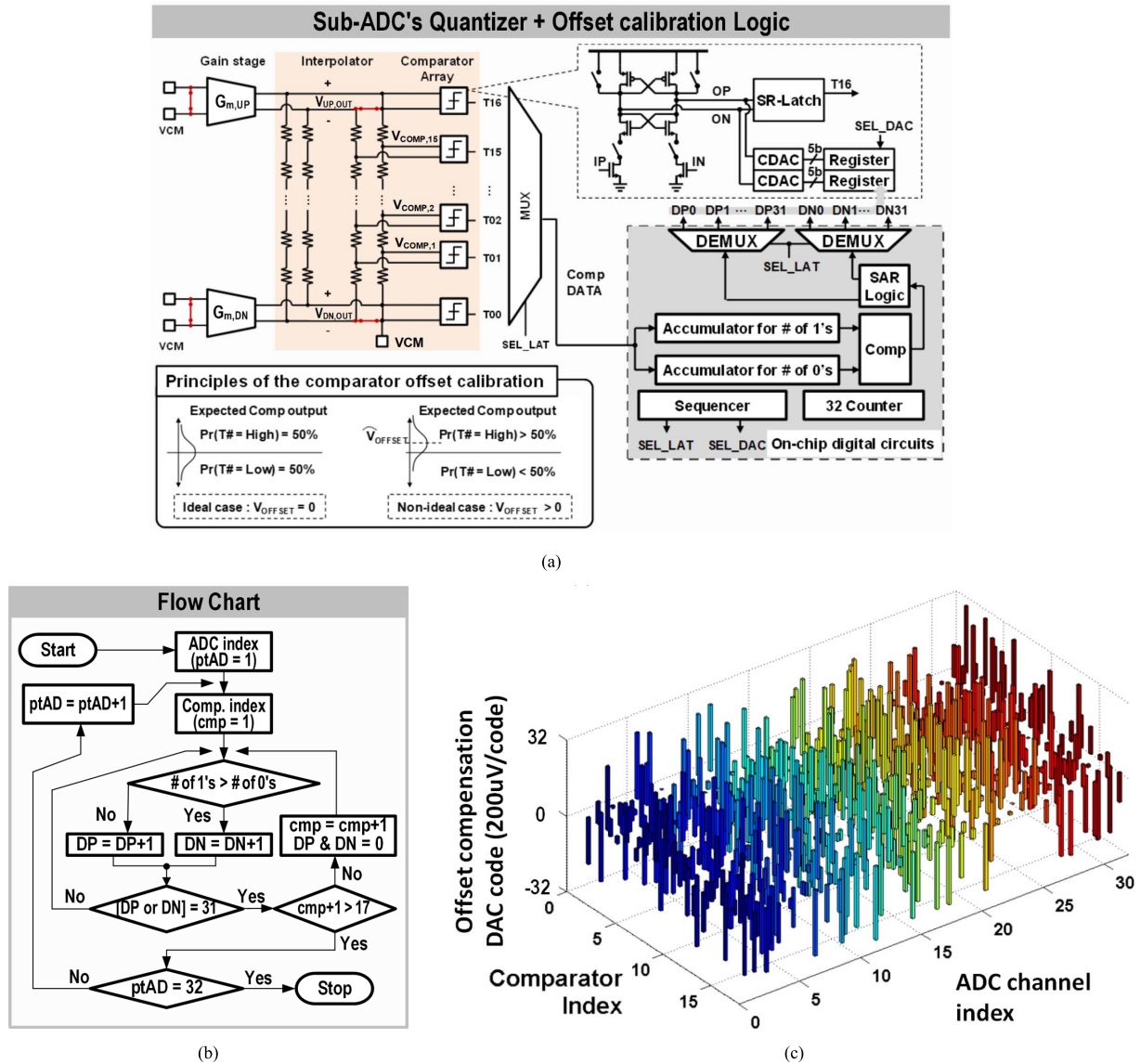
Fig. 14. (a) On-chip offset calibration process for the single ADC comparators. (b) Flowchart. (c) One example of the measured comparator offset compensation codes.

simulation, we achieved $<100~\mu V_{\text{rms}}$ noise for each pre-amplifier. However, the actual pre-amplifier noise contribution can be reduced by the interpolation network which suppresses the correlated noise between two pre-amplifiers. The power dissipation of the two G_m-cells is about 1 mW while under 1.1-V analog supply voltage. For the interpolator design, a simple resistor ladder between the two pre-amplifier outputs and utilization of the internal nodes for interpolation cause imbalanced voltage gain issues. This challenge can be better understood by examining the common mode and the differential mode gain of the transconductance (G_m) cell (pre-amplifier) loaded with the interpolator network, because the residue voltage V_{RES} and the reference voltage V_{REF} are the common mode and the differential input voltage, respectively.

For common-mode operation, as the output voltages of each G_m-cell moves in the same direction, no current flows through the resistor ladder. Therefore, the resistor ladders
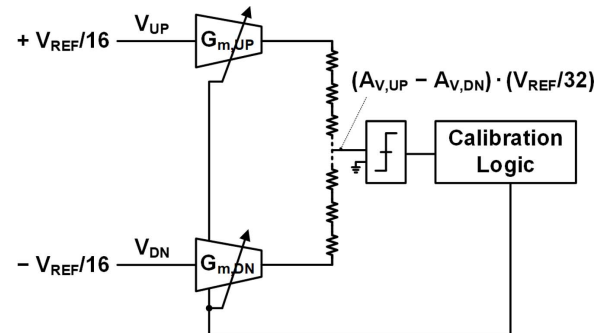

Fig. 15. On-chip pre-amplifier gain calibration process for the single ADC.

are effectively open for the residue signal gain, as shown in Fig. 11(a). However, the resistor ladder loads the differential signal at the amplifier output, as the ac signal flows through the resistor ladder. As a result, the voltage gains between the
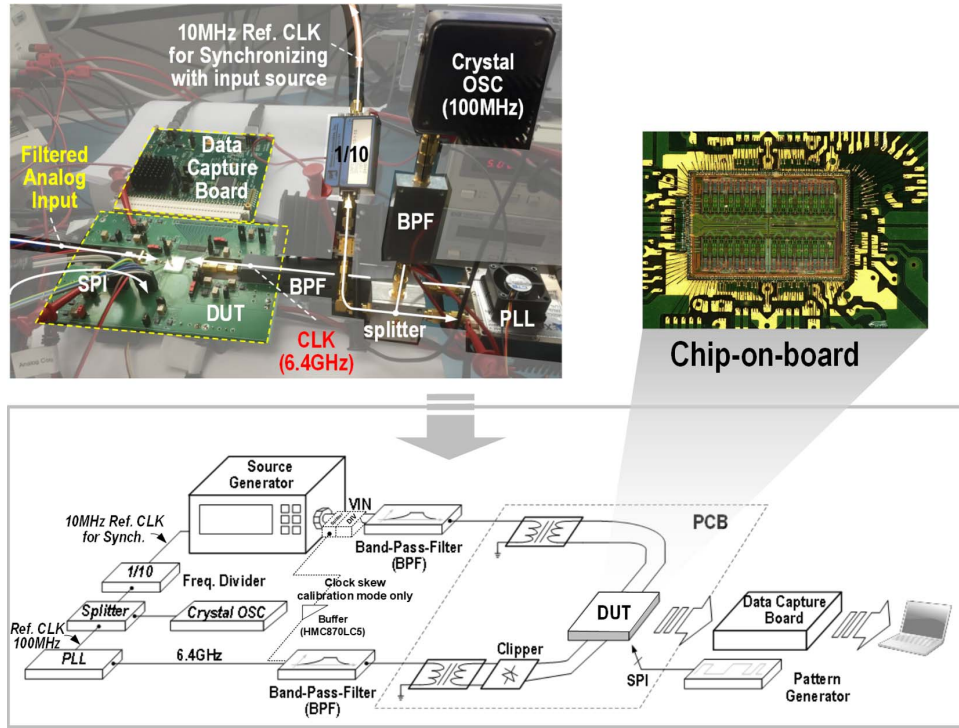
Fig. 16.   Test setup of the ADC prototype.

residue (V_{RES}) and reference (V_{REF}) paths are not matched, causing SAR conversion errors. To resolve this issue, we insert cross-coupled resistive paths to balance the voltage gains, which is basically a replica of the original resistor ladder. As shown in Fig. 11(b), the common-mode signal now has extra current paths among two G_m-cells. Therefore, the output impedance of G_m-cell (R_O) in parallel with half of the resistive ladder value determines the voltage gain. For the differential mode, the reference voltage gain remains the same without any disturbance from the additional resistor ladders. Thus, we resolve the gain mismatch issue, as the residue and reference path gains are now equalized.

Regarding the implementation of the G_m-cell (Fig. 12), as the non-linear gain error of the interpolator results overall DNL and INL errors, we employ the complementary input pair in order to achieve large output swing and small transconductance variations. Note that the MSB conversion errors can be corrected as long as total amount of errors are within the conversion redundancy.

In addition, we design the G_m-cell with two programmable voltage gains via configuring the output load resistance. The high gain mode is used for the last two SAR conversions for better noise performance. In contrast, the first two SAR conversions utilize the low gain mode and thus a wider bandwidth to achieve fast settling behavior. In addition, each G_m-cell equips output referred offset cancellation 7-b current DACs (I-DACs) and gain correction purposed 6-b I-DACs.

In order to determine proper interpolation resistance, we consider the mismatch requirement and settling error for a 4-bit conversion resolution. Additionally, the total resistance value determines the voltage gain of the pre-amplifiers as well.
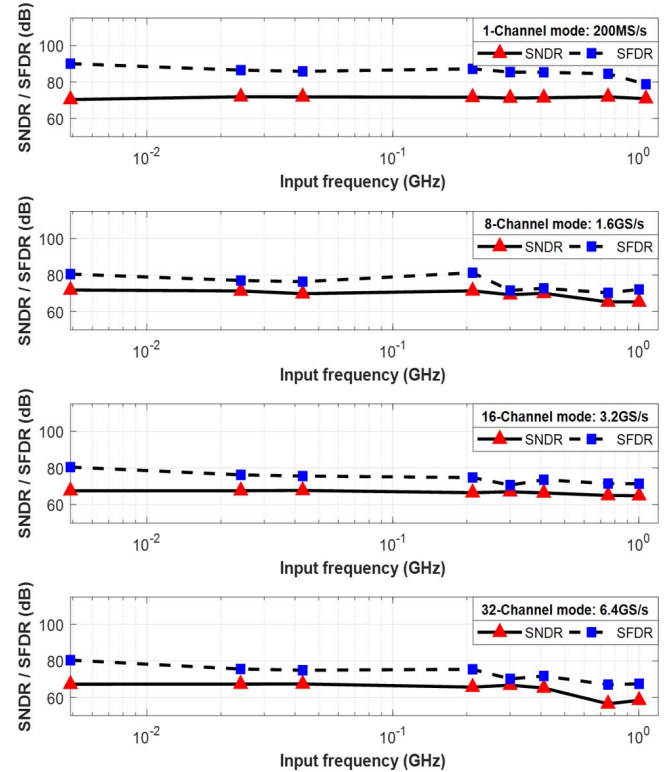

Fig. 17.   Measured ADC dynamic performances versus different input frequencies and sampling rates.

Therefore, we leverage an open-loop amplifier topology to achieve sufficient bandwidth while ensuring the required voltage gain. Unlike the reference voltage resistive ladder of a flash ADC, the proposed resistor interpolation placed in between
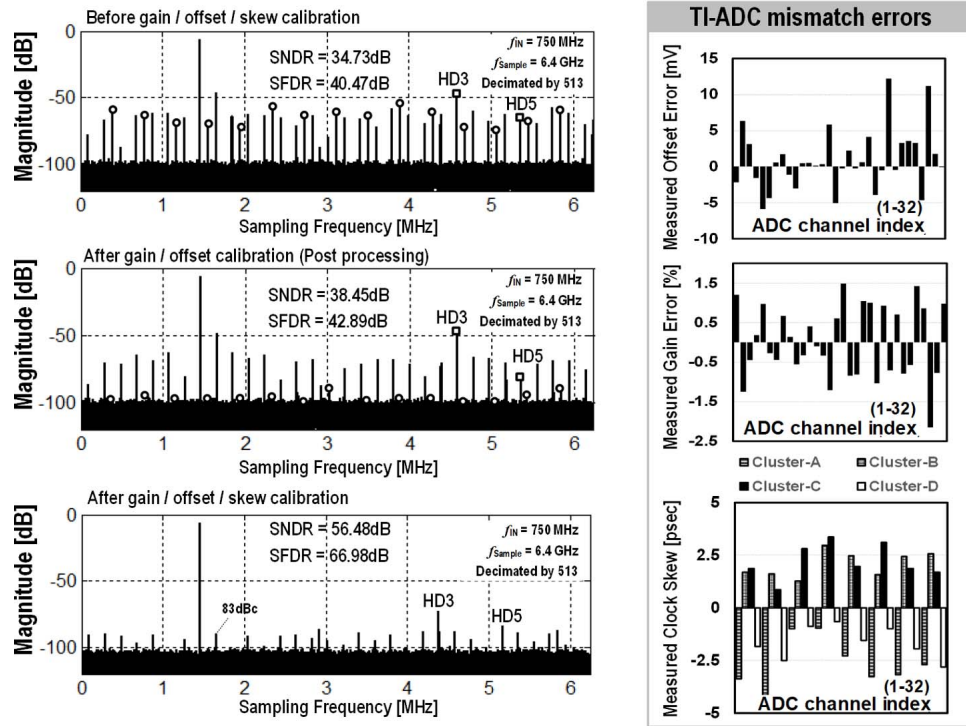
Fig. 18.   Measured channel-to-channel TI-ADC mismatches and FFT plots after calibration.
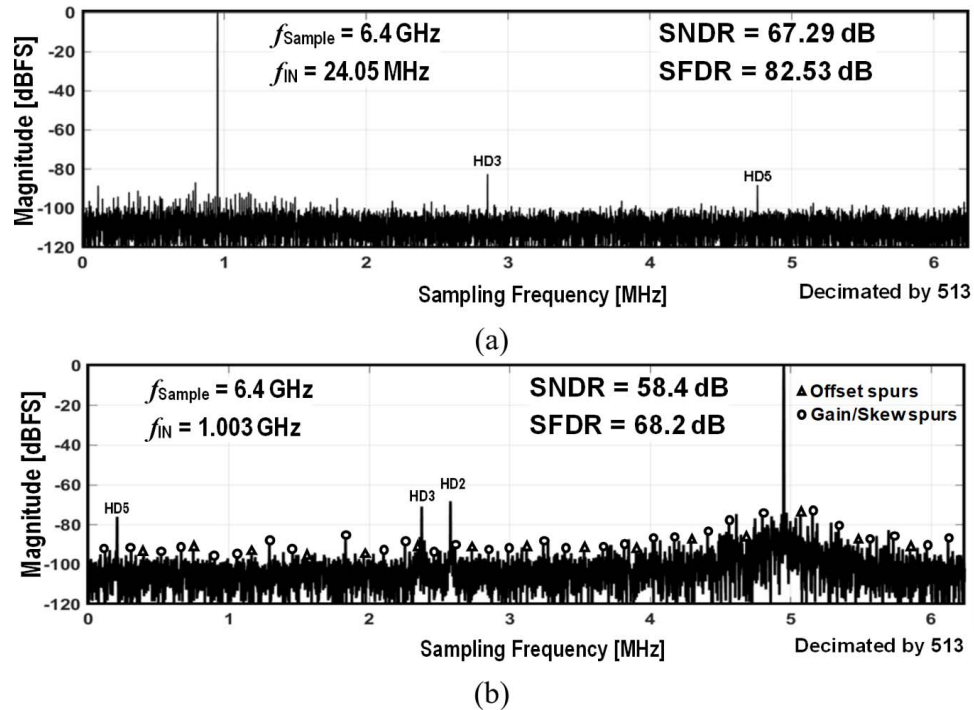

Fig. 19.   FFT plots at (a) low frequency and (b) high frequency input under 6.4 GS/s.

two pre-amplifiers does not consume dc power assuming there is no mismatch. The area of the resistor ladder network consumes about 0.0048 mm^2.

3) Clock Generator: The multi-phase clocks required in the SAR ADC are generated via two cascaded pulse generators and delay lines, as shown in Fig. 13(a). Basically, the sampling clock and all the control signals for SAR conversions are generated to be non-overlapping. The first pulse generator is initially triggered by the ADC sampling clock (CK$_X$), and the strobing clock for the comparators (CK$_{COMP}$) is then sequentially created. Next, the falling edge of CK$_{COMP}$ triggers the second pulse generator and creates the G_m-Cell
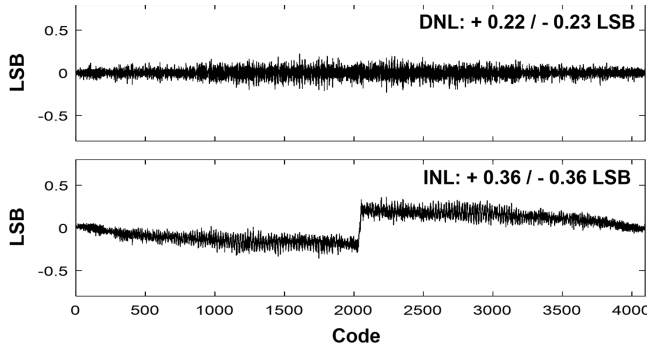
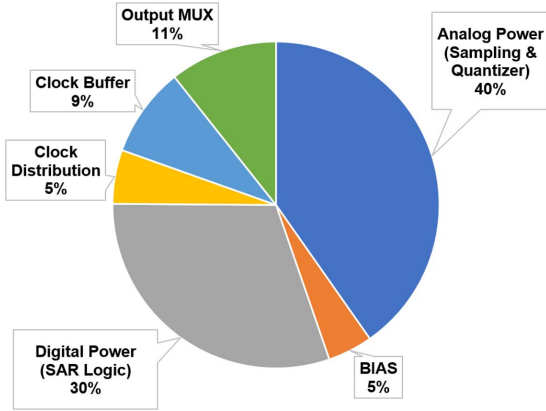Fig. 20.   Measured DNL and INL of a single ADC channel after calibration.

Fig. 22.   FOM comparison with the state-of-the-art ADCs (ISSCC and VLSI 1997–2017).

Fig. 21.   Power breakdown.

reset signal (Q_{RESET}). After CK$_{COMP}$ completes four cycles, the internal sequencer logic disables the entire clock generator. By tuning the delay lines, we can set the desired phase and the duty cycle of the clock pulses, as illustrated in Fig. 13(b). To implement the tunable delay line, we use a current-starved buffer chain, whose bias is adjusted with a 9-bit R-to-R DAC.

4) Calibration Circuits: As multiple comparators are used to quantize the voltage level, the offset mismatch between them can cause differential non-linearity (DNL) errors. Fig. 14(a) shows the details of the comparator offset calibration process. The offset of the comparator is measured by shorting its input and observing the statistics of ones and zeros at output over 32 samples. Ideally, when the comparator is free of offset, we should observe ones and zeros with equal probability. The on-chip calibration process is performed by counting the number of ones and zeros and successively adjusting the 5-bit offset DAC attached at the comparator output. To minimize the comparator noise impact on the counting process, we further average the statistics over multiple iterations (up to 64) for better offset measurement accuracy. All the comparators in each ADC channel are calibrated in sequence according to the flowchart in Fig. 14(a), and one example of the measured offset compensation codes is shown in Fig. 14(b), showing the distribution of the comparator offsets for that particular silicon chip. Similarly, the offset voltages of the two pre-amplifiers are calibrated in the same strategy with 7-bit current steering DACs shown in Fig. 12. Note that two extra comparators are used to detect the polarity of the pre-amplifier output and compensate the pre-amplifier
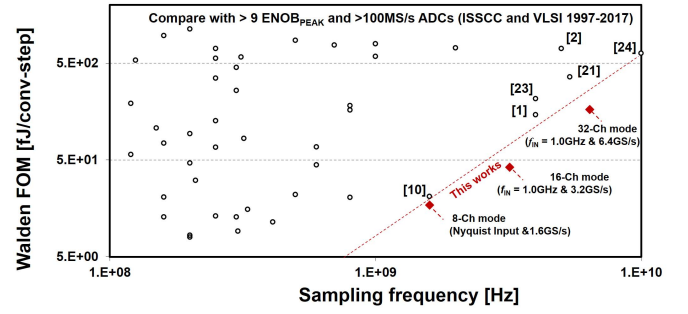
offset similar to the comparator offset calibration routines, while their offsets should be calibrated first.

According to the gain error analysis described in Section III-A, relative gain mismatches between two pre-amplifiers can degrade ADC performance. Therefore, we measure the gain mismatch from the circuit configuration as shown in Fig. 15. One critical element of the gain mismatch detection is the middle comparator whose input should be zero when the inputs of pre-amplifiers are set to be $\pm V_{REF}/16$ without gain mismatch. Based on this property, we then adjust pre-amplifier's gain by sweeping each 6-b I-DAC in the G_m-cell (shown in Fig. 12) until the middle comparator yields similar probability of ones and zeros. In order to suppress the noise effect, we average the results over a few hundred samples. Note that, both offset calibrations for the comparator array and pre-amplifiers should be performed first. Ultimately, the resistor mismatch in the interpolator limits the gain calibration accuracy, which was ensured via Monte Carlo simulations.

V. MEASUREMENT

Fig. 16 shows the measurement setup for the ADC prototype characterization. We use a low-noise clock source that synchronizes the input signal generator. Next, we filter the input and clock signals using high-order bandpass filters. In addition, to sharpen the clock edge from a large signal swing, we use clipping diodes in the clock signal path to ensure low clock jitter. For the ADC output, on-chip digital circuits decimate the digital data stream, which is then recorded with an external logic analyzer.

The ADC prototype is fabricated in 65-nm CMOS and assembled via chip on board (COB). The measured dynamic performances of the ADC at a sampling rate of 200 MS/s (enabling single ADC channel only), 1.6 GS/s (enabling eight ADC channels), 3.2 GS/s (enabling 16 ADC channels), and 6.4 GS/s (enabling 32 ADC channels) with differential 1.6 V_{PP} sinusoids are illustrated in Fig. 17. In the 6.4-GS/s mode, the SNDR measures from 67.2 to 58.4 dB at an input frequency of 1 GHz. In the measurement of amplitude versus input frequency, the signal attenuation is less than 1 dB up to about 2.0 GHz (enabling eight ADC channels) and up to about 1.0 GHz (enabling 16 or 32 ADC channels) mainly due to the bandwidth limitation of the input network.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

		This work			VLSI-12 D. Stepanović	ISSCC-16 M. Straayer	ISSCC-16 C.-Y. Lin	VLSI-16 A.M.A. Ali	VLSI-13 J. Wu	ISSCC-17 S. Devarajan	ISSCC-17 B. Vaz	ISSCC-16 J. Wu
Resolution (bit)		12			11	14	10	14	12	12	13	13
Architecture (Interleaving)		TI-SAR (8x / 16x / 32x)			TI-SAR (24x)	TI-Pipeline (16x)	TI-SAR (16x)	TI-Pipeline (2x)	TI-Pipeline (2x)	TI-Pipeline (8x)	TI-Pipeline-SAR (8x)	Pipeline (4x@stage2)
Speed (GS/s)		1.6	3.2	6.4	2.8	4.0	2.6	5.0	5.4	10	4.0	4.0
Input Frequency (GHz)		1.0			1.379	1.842	1.3	2.0	2.7	4.0	1.9	1.9
High Frequency	SNDR (dB)	65.3	64.91	58.4	49.72	55.5	50.6	*58	*50	55	57.3	56
	SFDR (dB)	72.14	71.46	68.2	59.06	64	57.8	*70	65	66	67	68
Power Dissipation (mW)		***40.7	**120.6	**225	44.6	2214	**18.4	2300	500	2900	513	300
FOM_Walden (fJ/conv.-step)		16.9	39.1	165.5	75.8	1130	25.6	*708.7	*358.4	631.2	214.2	145.5
FOM_Schreier (fJ/conv.-step)		169.2	164.4	154.9	153.2	145.1	159.1	*148.4	*147.3	147.4	153.2	154.2
Technology		65nm			65nm	65nm	40nm	28nm	28nm	28nm	16nm	16nm

* Estimated value based on published data
** Excluding power dissipation on ref. driver
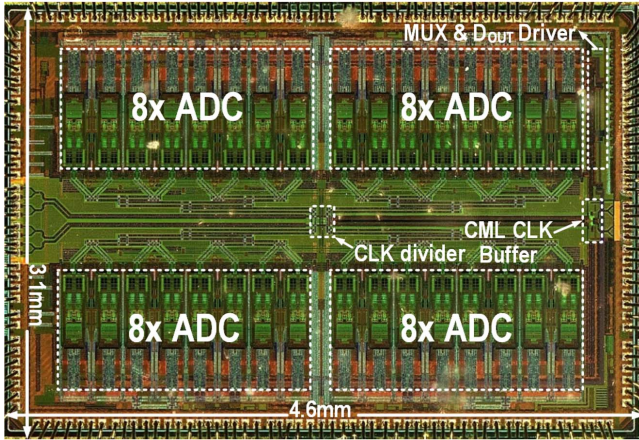*** Excluding power dissipation on ref. and clock drivers

Fig. 23. Chip micrograph.

We use several calibration routines to compensate for time-interleaving errors, including the foreground inter-channel gain, offset, and clock skew calibrations. For clock skew calibration, we first measure the clock skew and compensate it via an on-chip clock skew tuning circuit in each ADC channel, as explained in Section IV-B2 and shown in Fig. 16. In order to perform the clock skew calibration, additional signal splitter, divider, and clock buffer are needed, and the calibration process should run in the foreground. The measured spur level is reduced by 35 dB before and after the calibration routines are applied, as shown in Fig. 18. Fig. 19 shows the output spectrum of the 32-way TI-ADC, i.e., 6.4 GS/s, at an input frequency of 24 MHz and 1 GHz, where the ADC outputs are decimated by a factor of 513. Fig. 20 shows the measured single ADC channel INL/DNL after digital radix calibration. The DNL is $+0.22/-0.23$ LSB and INL is $+0.36/-0.36$ LSB after calibration [20], [21]. The power breakdown of the ADC is organized at Fig. 21, the ADC uses 1.1-, 1.2-, and 2.5-V supply for analog, digital/clock, and digital output driver power domain, respectively. The performance summary and comparison with the state-of-the-art ADCs [25] are reported in Fig. 22 and Table II.

The figure-of-merit (FOM_Walden), defined as power dissipation/($2^{ENOB} \cdot \min\{2 \cdot ERBW, f_{Sample}\}$), where ERBW is the effective resolution bandwidth, achieves a 16.9-fJ/conversion step at 1.6 GS/s with Nyquist input frequency and a 39.1-fJ/conversion step and 165.5-fJ/conversion step at the input frequency of 1 GHz in 3.2 and 6.4 GS/s, respectively. The ADC die micrograph is shown in Fig. 23. The overall chip area is 14.26 mm^2 ($= 4.6$ mm $\times$ 3.1 mm).

VI. CONCLUSION

This paper presents a TI 4-bit/cycle SAR ADC architecture with the proposed DRSI technique. The architecture has been shown to enhance power efficiency with reduced hardware burden. This is crucial in forging a path toward higher resolutions and higher speeds but with lower power consumption in analog-to-digital conversion. Despite efforts to reduce the input loading of the ADC, the input bandwidth is still limited to about 1 GHz mainly due to the parasitics of long routing that connects all ADC channels. We expect this issue can be alleviated by inserting on-chip buffers [12] through the sampling network at a cost of higher distortion or using a scaled technology to further reduce the area of the single ADC channel. Finally, as the ADC is mostly a digital implementation, the area and power efficiency is expected to be improved in the scaled technology [21].

REFERENCES

[1] J. Wu *et al.*, "A 4 GS/s 13 b pipelined ADC with capacitor and amplifier sharing in 16 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 466–467.

[2] A. M. A. Ali *et al.*, "A 14-bit 2.5 GS/s and 5 GS/s RF sampling ADC with background calibration and dither," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 206–207.

[3] M. Brandolini *et al.*, "A 5 GS/S 150 mW 10 b SHA-less pipelined/SAR hybrid ADC in 28 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 468–469.

[4] K. Poulton *et al.*, "A 20 GS/s 8 b ADC with a 1 MB memory in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2003, pp. 318–319.

[5] J.-W. Nam, M. Hassanpourghadi, A. Zhang, and M. S.-W. Chen, "A 12-bit 1.6 GS/s interleaved SAR ADC with dual reference shifting and interpolation achieving 17.8 fJ/conv-step in 65 nm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 1–2.

[6] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.6 mW 6 bit 2.2 GS/s fully dynamic pipeline ADC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2080–2090, Oct. 2010.

[7] K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, and G. van der Weide, "A 480 mW 2.6 GS/s 10 b time-interleaved ADC with 48.5 dB SNDR up to Nyquist in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 180–181.

[8] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.

[9] S. Lee, A. P. Chandrakasan, and H.-S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 862–873, Dec. 2014.

[10] B.-R.-S. Sung *et al.*, "A 21 fJ/conv-step 9 ENOB 1.6 GS/S 2× time-interleaved FATI SAR ADC with background offset and timing-skew calibration in 45 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 464–465.

[11] L. Kull *et al.*, "Implementation of low-power 6–8 b 30–90 GS/s time-interleaved ADCs with optimized input bandwidth in 32 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 636–648, Oct. 2016.

[12] M. Straayer *et al.*, "A 4 GS/s time-interleaved RF ADC in 65 nm CMOS with 4 GHz input bandwidth," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 464–465.

[13] B. Setterberg *et al.*, "A 14 b 2.5 GS/s 8-way interleaved pipelined ADC with background calibration and digital dynamic linearity correction," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 466–467.

[14] Y.-C. Lien, "A 14.6 mW 12 b 800 MS/s 4×time-interleaved pipelined SAR ADC achieving 60.8 dB SNDR with Nyquist input and sampling timing skew of 60fsrms without calibration," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 1–2.

[15] Z. Cao, S. Yan, and Y. Li, "A 32 mW 1.25 GS/s 6b 2 b/step SAR ADC in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 862–873, Mar. 2009.

[16] H. Wei *et al.*, "An 8-b 400-MS/s 2-b-per-cycle SAR ADC with resistive DAC," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2763–2772, Nov. 2012.

[17] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. B. U, and R. P. Martins, "A 6 b 5 GS/s 4 interleaved 3 b/cycle SAR ADC," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 365–377, Feb. 2016.

[18] H.-K. Hong *et al.*, "A 2.6 b/cycle-architecture-based 10 b 1 JGS/s 15.4 mW 4×-time-interleaved SAR ADC with a multistep hardware-retirement technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 470–471.

[19] C.-H. Chan, Y. Zhu, I.-M. Ho, W.-H. Zhang, S.-P. U, and R. P. Martins, "5 mW 7 b 2.4 GS/s 1-then-2 b/cycle SAR ADC with background offset calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 282–283.

[20] J.-W. Nam and M. S.-W. Chen, "An embedded passive gain technique for asynchronous SAR ADC achieving 10.2 ENOB 1.36-mW at 95-MS/s in 65 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 10, pp. 1628–1638, Jul. 2016.

[21] S.-W. M. Chen and R. W. Broderson, "A 6 b 600 MS/s 5.3 mW asynchronous ADC in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2669–2680, Dec. 2006.

[22] J. Wu *et al.*, "A 5.4 GS/s 12 b 500 mW pipeline ADC in 28 nm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Feb. 2013, pp. C92–C93.

[23] B. Vaz *et al.*, "A 13 b 4 GS/s digitally assisted dynamic 3-stage asynchronous pipelined-SAR ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 276–277.

[24] S. Devarajan, "A 12 b 10 GS/s interleaved pipeline ADC in 28 nm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 288–289.

[25] B. Murmann. *ADC Performance Survey 1997-2017*. Accessed: Oct. 2017. [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

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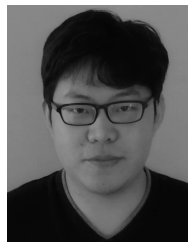
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