High Step-Up Soft-Switched Converters Using Voltage Multiplier Cells

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***Abstract*—In this paper, a soft-switched dc–dc converter using voltage multiplier cells is proposed for high-step up application. The proposed converter has the following advantages: 1) doubled voltage conversion ratio of the basic configuration ($N = 1$) compared to the conventional boost converter; 2) zero voltage switching turn ON of switches and zero current switching turn OFF of diodes; 3) low input current ripple, reduced size of the passive component and current stresses of switches due to interleaved structure, and 4) increased flexibility in device selection by adjusting the number of voltage multiplier cells. The proposed converter is compared to some high step-up converters. Experimental results from a 1-kW prototype are provided to validate the proposed concept.**

***Index Terms*—Active-clamping, high step-up, interleaved, soft switched, voltage multiplier cell.**

I. Introduction

RECENTLY, nonisolated high step-up dc–dc converters are used in many applications, such as high-intensity discharge lamp for automotives, dc back-up energy systems for UPS, renewable energy systems, fuel cell systems, and hybrid electric vehicles. In order to provide high output voltage, the classical boost converter should operate at extreme duty cycle, and hence the rectifier diode must sustain a short pulse current with high amplitude. This results in severe reverse recovery as well as high electromagnetic interference problems. Using extreme duty cycle may also lead to poor dynamic responses to line and load variations. Moreover, the input current in these high step-up applications is usually large, but low-voltage-rated MOSFETs with small $R_{\mathrm{DS(ON)}}$ may not be selected since voltage rating of the switch is the same as the high output voltage in the boost converter.

High step-up converters with coupled inductors [1]–[7] can provide high output voltage without using extreme duty cycle and yet reduce the switch voltage stress. The reverse recovery problem associated with rectifier diodes is also alleviated. However, some topologies suffer from losses associated with leakage energy of the coupled inductor. Also, most of the converters with a coupling inductor have large input current ripple due to the operation of the coupling inductor.

The switched-capacitor converter [8], [9] does not employ any inductor making it feasible to achieve high power density. However, the efficiency could be reduced to perform output voltage regulation. A major drawback of theses topologies is that attainable voltage gain and power level without degrading system performances are restricted. An effective way of extending these schemes to achieve higher voltage gain or power level has not been discussed.

A single-switch converter with multiplier cells was proposed to attain high output voltage by adding multiplier cells, but current stress of the switch is not trivial to get higher power. It has been demonstrated that the interleaved technique provides the advantages of handling high current and reducing passive component size [10] and [11]. An interleaved converter with voltage doubler characteristic [12] can have low input current ripple and reduced switch current stresses due to interleaved operation; however, extending the scheme to achieve higher voltage gain has not been discussed. An interleaved converter with voltage multiplier cells [13] has been proposed to provide higher voltage gain. A modified SEPIC converter with high-voltage gain has been proposed in [14]. It uses only single switch with reduced voltage rating, and obtains very high voltage gain with small number of components. These schemes are based on the hard-switching operation, and therefore, the switching frequency is limited. Recently, soft-switched interleaved high step-up converters [15]–[19] have been proposed. They are basically operated with zero voltage switching (ZVS) or zero current switching (ZCS) turn ON of switches and do not require additional snubber circuits to clamp voltage spikes associated with magnetic components.

In this paper, an active clamped dc–dc converter is proposed for high step-up applications where the active clamping circuit is able to achieve ZVS turn ON of switches and ZCS turn OFF of diodes as well as clamp the voltage spikes caused by parasitic inductance. Analysis of the inclusion of the active clamping to obtain soft commutation and voltage clamping is carried out. The voltage multiplier cells of the proposed converter can be increased to get high output voltage and/or reduce voltage stresses of components, which results in increased flexibility in device selection.

II. Proposed High Step-Up Soft-Switched Converter

A. Operating Principles

Fig. 1 shows the generalized circuit configuration of the proposed high step-up converter which consists of two

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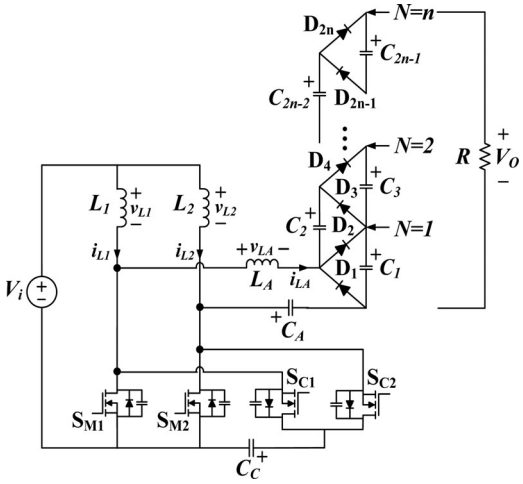

Fig. 1. Proposed high step-up soft-switched converter.

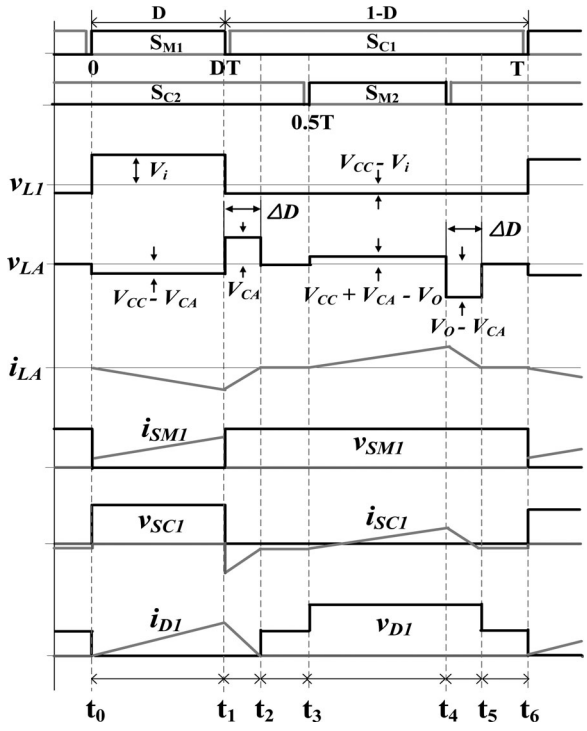

Fig. 2. Key waveforms of the proposed converter with $N = 1$ ($D < 0.5$).

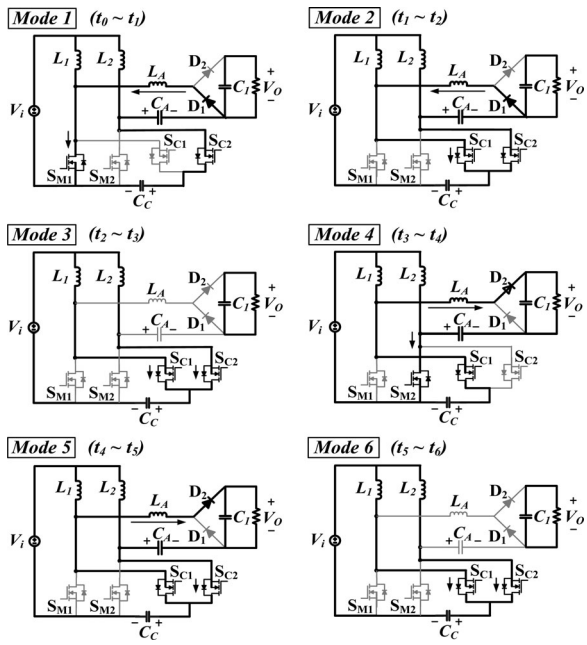

Fig. 3. Operating states of the proposed converter with $N = 1$ ($D < 0.5$).

inductor-switch legs, an active clamp circuit, an auxiliary capacitor and inductor, and voltage multipliers. The number N denotes number of voltage multipliers where each multiplier is composed of two diodes and two capacitors. The number N should be chosen properly considering the required voltage gain and voltage ratings of the diodes and capacitors. Owing to the operation of the clamp switch the duty cycle of the converter can be extended to the range between 0 and 1. The active clamping operation helps not only clamp the voltage spikes caused by parasitic inductance in the circuit layout, but also achieve ZVS turn ON of switches and ZCS turn OFF of diodes. The key waveforms and operating states of the proposed converter with $N = 1$ are shown in Figs. 2–5. The proposed converter operates under two different regions according to the duty cycle: $D < 0.5$ and $D > 0.5$. The operating modes of the proposed converter are analyzed based on the two regions.

1) Operation in $D < 0.5$: Fig. 2 shows key waveforms of the proposed converter in the case of $D < 0.5$. The operation states of the proposed converter are shown in Fig. 3.

   Mode 1 [t_0–t_1]: main switch S_{M1} is turned ON at t_0, and current on input filter inductor L_1 starts linearly increasing. The voltage across auxiliary inductor L_A can be obtained by $V_{LA} = -V_{CC} + V_{CA}$.
   Since voltage V_{LA} becomes negative values, it leads to the conduction of diode D_1 and the current on auxiliary inductor L_A starts increasing in the direction shown in the equivalent circuit. Switch S_{M1} carries the current on both filter inductor L_1 and auxiliary inductor L_A.

   Mode 2 [t_1–t_2]: main switch S_{M1} is turned OFF at time t_1, and the current through main switch S_{M1} is commutated to the body diode of the clamp switch S_{C1}. The gating signal for S_{C1} is applied during this mode, and S_{C1} is turned ON under ZVS conditions. The voltage across auxiliary inductor L_A becomes equal to V_{CA} which is large positive value leading to fast decrease of current i_{LA}. This mode ends when current i_{LA} reaches 0 A. It is noted that diode D_1 is turned OFF under ZCS condition.

   Mode 3 [t_2–t_3]: the output capacitor supplies the load during this mode. Clamp switch S_{C2} is turned OFF, and the current i_{L2} is commutated to the body diode of the clamp switch S_{C2}. It is noted that S_{C2} is turned OFF under ZVS conditions. This mode ends when main switch S_{M2} is turn ON at t_3. The other half of a cycle is repeated in the same fashion.

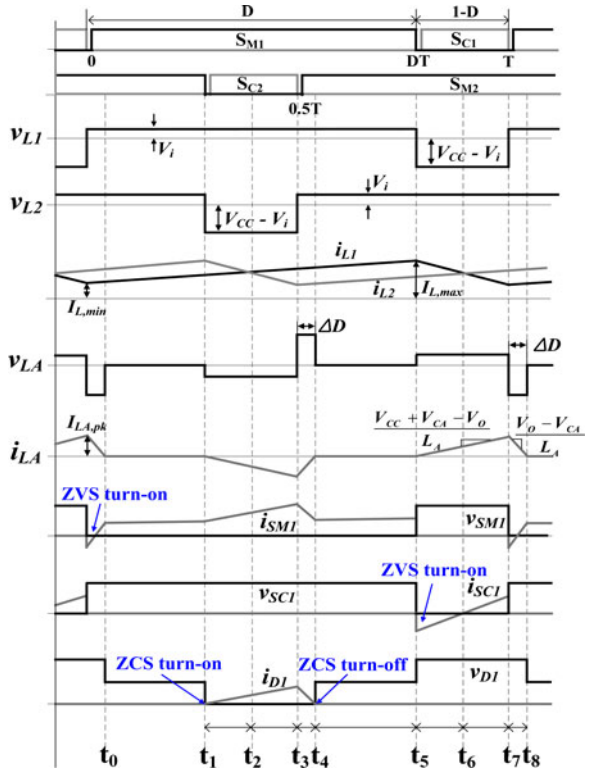

Fig. 4. Key waveforms of the proposed converter with $N = 1$ ($D > 0.5$).

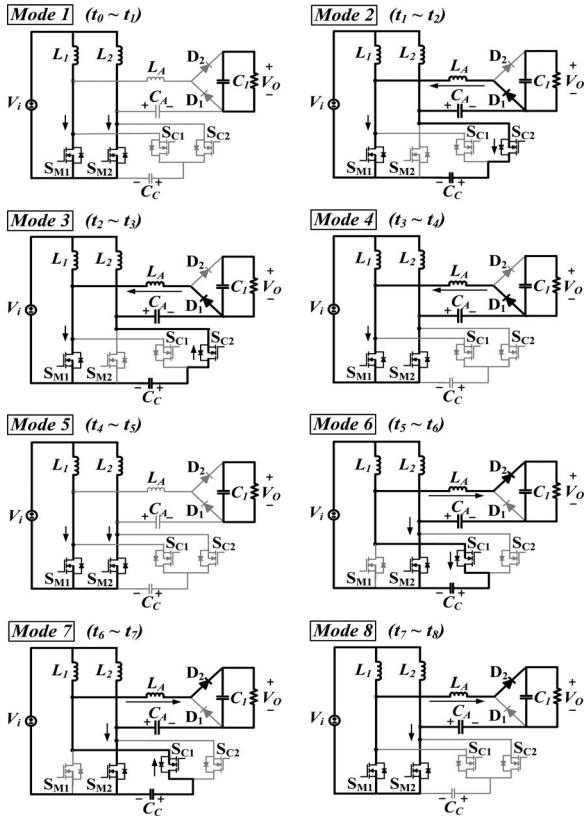

Fig. 5. Operating states of the proposed converter with $N = 1$ ($D > 0.5$).

2) Operation in $D > 0.5$: Fig. 4 shows key waveforms of the proposed converter in the case of $D > 0.5$. The operation states of the proposed converter are shown in Fig. 5.

Mode 1 [t_0–t_1]: main switches S_{M1} and S_{M2} are conducting linearly increasing filter inductor currents i_{L1} and i_{L2}, respectively. The output capacitor supplies the load during this mode.

Mode 2 [t_1–t_2]: main switch S_{M2} is turned OFF at t_1, and the current through main switch S_{M2} is commutated to the body diode of the clamp switch S_{C2}. The gating signal for S_{C2} is applied during this mode, and S_{C2} is turned ON under ZVS conditions. The voltage across auxiliary inductor L_A can be obtained by $V_{LA} = -V_{CC} + V_{CA}$.

Since voltage V_{LA} becomes negative values, it leads to the conduction of diode D_1 and current i_{LA} starts increasing in the direction shown in the equivalent circuit.

Mode 3 [t_2–t_3]: at the instant when current i_{LA} becomes larger than current i_{L2}, the current through S_{C2} changes its direction. Current i_{LA} keeps linearly increasing.

Mode 4 [t_3–t_4]: clamp switch S_{C2} is turned OFF at time t_3, and the current through S_{C2} is commutated to the body diode of the main switch S_{M2}. The gating signal for S_{M2} is applied during this mode, and S_{M2} is turned ON under ZVS conditions. The voltage across auxiliary inductor L_A becomes equal to V_{CA} which is large positive value leading to fast decrease of current i_{LA}. This mode ends when current i_{LA} reaches 0 A. It is noted that diode D_1 is turned OFF under ZCS condition. The other half of a cycle is repeated in the same fashion.

TABLE I
SWITCHING CHARACTERISTICS OF MOSFETS AND DIODES BASED ON DUTY CYCLE

Duty cycle range		$0 < D < 0.5$	$0.5 < D < 1$
Main Switches S_{M1}, S_{M2}	Turn on	Hard Switching	ZVS
	Turn off	Hard Switching	Hard Switching
Clamp Switches S_{C1}, S_{C2}	Turn on	ZVS	ZVS
	Turn off	ZVS	Hard Switching
Diodes D_1, D_2	Turn on	ZCS	ZCS
	Turn off	ZCS	ZCS

It can be seen from Fig. 4 that both main and clamp switches are turned ON with ZVS while they are hard-switched at turning off. However, the hard-switched turn-off should not be a problem since the voltage rating of the main switches can be designed low enough even though the output voltage is high. This is because the voltage rating of the switches is determined by the input voltage, duty cycle, and number of voltage multiplying cells N, not directly by the output voltage. For the whole duty cycle range, the diodes are turned OFF with ZCS leading to negligible surge caused by the diode reverse recovery characteristic. The switching characteristics of the switching devices based on the duty cycle are summarized in Table I. For this high-step application, it is recommended that the duty cycle be

designed to be operated greater than 0.5 so that the switching losses of MOSFETs can be minimized.

B. Voltage Gain Expression

The initial development of the voltage gain expression is considered for $N = 1$. It is assumed that the voltage across C_C and C_A are constant during the switching period of T. From the volt-second balance equation for inductor L_1 or L_2, the voltage across the clamp capacitor V_{CC} becomes

$$V_{CC} = \frac{1}{1-D} V_i. \tag{1}$$

Applying the volt-second balance equation to auxiliary inductor L_A the voltage across the auxiliary capacitor V_{CA} is obtained by

$$V_{CA} = \frac{1}{2} V_O. \tag{2}$$

As Figs. 2 and 4 illustrate, the parameter ΔD can be introduced to represent the amount of time it takes the inductor current i_{LA} to travel from its peak value to its zero crossing. For $D < 0.5$, this is defined as $\Delta D = (t_2 - t_1)/T$ in Fig. 2. For $D > 0.5$, this is defined as $\Delta D = (t_4 - t_3)/T$ in Fig. 4. Using this parameter and applying the volt-second balance equation to auxiliary inductor L_A between t_1 and t_4 results in

$$\frac{V_{CA}}{V_{CC}} = \frac{1-D}{1-(D-\Delta D)}. \tag{3}$$

From (1)–(3), the voltage gain can be expressed as

$$\frac{V_O}{V_i} = \frac{2}{1-(D-\Delta D)}. \tag{4}$$

ΔD may cause an output voltage drop as we can see from (4). Since the average value of the diode currents is the same as the average value of the output current I_O, the peak value of the diode currents can be expressed as

$$I_{D1,pk} = I_{D2,pk} = \frac{2I_O}{1-(D-\Delta D)}. \tag{5}$$

The peak value of the diode currents can be expressed as (see the slope of the current i_{LA} in Fig. 4)

$$I_{D1,pk} = I_{D2,pk} = \frac{(V_{CC} + V_{CA} - V_O)(1-D)T}{L_A} \tag{6}$$

where $T(=1/f_S)$ is the switching period. From (1), (2), (5), and (6), the duty cycle ΔD can be obtained by

$$\Delta D = D - 1 + \frac{4L_A I_O f_S}{2V_i - V_O(1-D)}. \tag{7}$$

From (4) and (7), the voltage gain of the proposed converter with $N = 1$ for $D > 0.5$ can be obtained by

$$\frac{V_O}{V_i} = \frac{D - 1 + \sqrt{(1-D)^2 + 16k}}{4k}, \quad D > 0.5 \tag{8}$$

where $k = (L_A \cdot f_S)/R$ and R is the load resistance. In the same way, the voltage gain of the proposed converter with $N = 1$ for $D < 0.5$ can also be obtained by

$$\frac{V_O}{V_i} = \frac{D(D - \sqrt{D^2 + 16k})}{4k(D-1)}, \quad D < 0.5. \tag{9}$$

Similarly, the voltage gain of the proposed converter with $N \geq 2$ can be obtained by

$$\frac{V_O}{V_i} = \frac{N\left\{(D-1) + \sqrt{(1-D)^2 + 8k}\right\}}{2k}, \quad 0 < D < 1. \tag{10}$$

From (8)–(10), the voltage gain of the proposed converter is drawn in Fig. 6 as a function of duty ratio D for several N and k. Table II lists the voltage ratings of the components of the proposed converter.

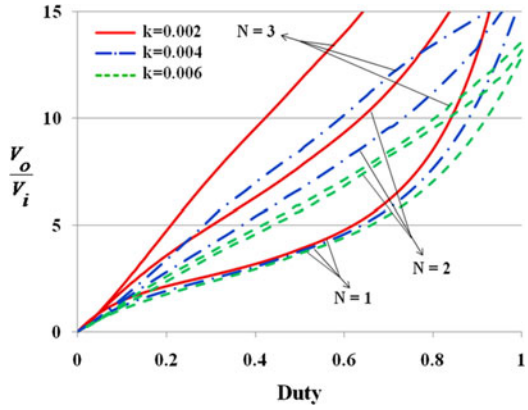

Fig. 6. Voltage gain of the proposed converter as a function of duty ratio D for several N and k.

TABLE II
COMPONENTS' VOLTAGE RATING OF THE PROPOSED CONVERTER

Components	Voltage rating
Main and Clamp Switches	$\frac{V_i}{1-D}$
Clamp Capacitor C_C	
Auxiliary Capacitor C_A	$\frac{V_O}{2N}$
Diodes	$\frac{V_O}{N}$
Output Capacitors $C_1 \sim C_{2N-1}$	

C. ZVS Current and ZVS Range

From Fig. 4, the average value and ripple magnitude of inductors L_1 and L_2 can be obtained, respectively, by

$$I_{L,av} = \frac{P_O}{2V_i} \tag{11}$$

$$\Delta I_L = \frac{V_i}{L \cdot f_S} D \tag{12}$$

where $L_1 = L_2 = L$.

The peak value of the auxiliary inductor L_A can also be obtained by

$$I_{LA,pk} = \frac{V_{CC} + V_{CA} - V_O}{L_A \cdot f_S}(1-D). \tag{13}$$

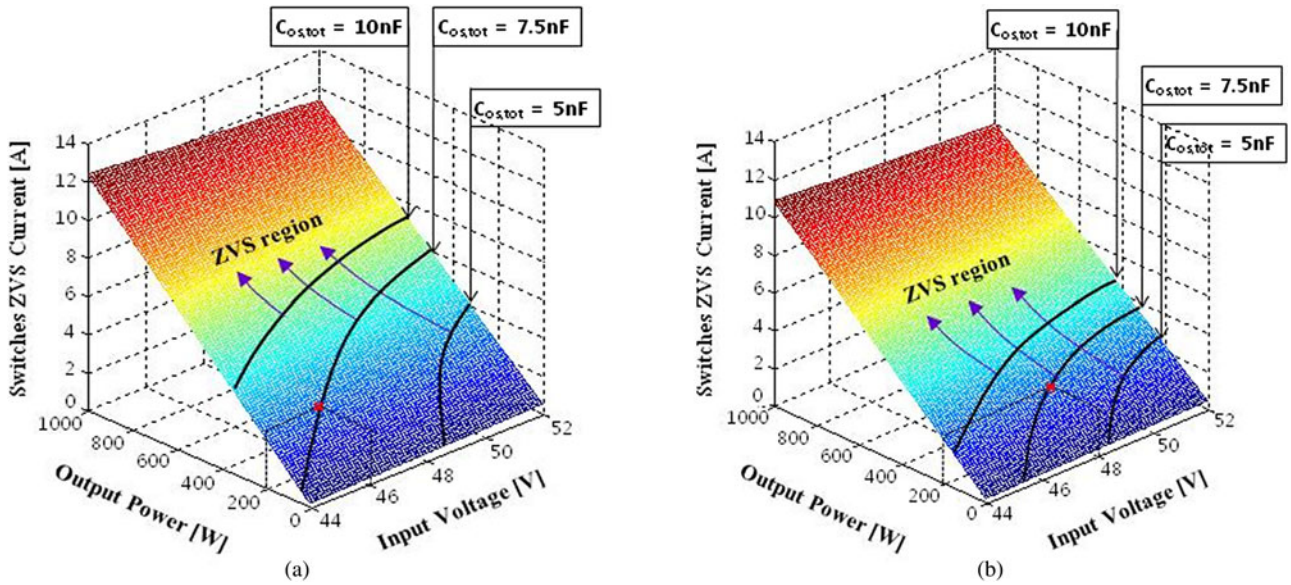

Fig. 7. ZVS currents and ZVS ranges of main switches as the function of the input voltage and output power (a) $N = 1$ ($V_O = 380$ V, $L = 720$ μH, $L_A = 6.3$ μH, $f_S = 50$ kHz). (b) $N = 2$ ($V_O = 380$ V, $L = 120$ μH, $L_A = 6.3$ μH, $f_S = 50$ kHz).

The ZVS current of main switches is the difference of inductor current i_L and auxiliary inductor current i_{LA} at t_7, as shown in Fig. 4, can be obtained by

$$I_{\mathrm{SM,ZVS}} = I_{LA,pk} - I_{L,\min} = \frac{V_i^2(2 \cdot L + D \cdot L_A) + V_i \cdot V_O \cdot L\,(D-1) - P_O \cdot L \cdot L_A \cdot f_S}{2V_i \cdot L \cdot L_A \cdot f_S}. \tag{14}$$

The ZVS current of clamp switches is the peak value of inductor current i_L at t_5, as shown in Fig. 4, can be obtained by

$$I_{\mathrm{SC,ZVS}} = I_{L,\max} = \frac{P_O \cdot L \cdot f_S + V_i^2 \cdot D}{2V_i \cdot L \cdot f_S} \tag{15}$$

To ensure the ZVS turn ON of main switches, the following condition should be satisfied

$$\frac{1}{2} L_A \cdot I_{\mathrm{SM,ZVS}}^2 > \frac{1}{2} C_{os,\mathrm{tot}} \left(\frac{V_i}{1-D} \right)^2 \tag{16}$$

where $C_{os,\mathrm{tot}} = C_{os,\mathrm{SM}} + C_{os,\mathrm{SC}}$ and $C_{os,\mathrm{SM}}$ and $C_{os,\mathrm{SC}}$ are output capacitances of main and clamp switches, respectively.

To ensure the ZVS turn ON of clamp switches, the following condition should be satisfied

$$\frac{1}{2} L \cdot I_{\mathrm{SC,ZVS}}^2 > \frac{1}{2} C_{os,\mathrm{tot}} \left(\frac{V_i}{1-D} \right)^2 \tag{17}$$

In fact, the condition of (17) can easily be satisfied, and therefore ZVS of clamp switches can be achieved over the whole load range. Using (14) and (16), the ZVS currents and ZVS ranges of main switches as the function of input voltage and output power are plotted in Fig. 7. The ZVS current of the main switch tends to increase as the output power increases. This means that the ZVS turn ON of the main switch can be more easily achieved under the condition of higher output power. It is noted that the ZVS range of the main switch becomes broader for smaller total output capacitance $C_{os,\mathrm{tot}}$ of MOSFETs. For example, if MOSFETs with total output capacitance $C_{os,\mathrm{tot}}$ of 7.5 nF are selected, the ZVS turn ON of the main switch can be achieved with output power greater than 200 W at input voltage of 46 V [see Fig. 7(a)]. It should be noted that the ZVS range of the proposed converter with $N = 2$ is wider than that with $N = 1$ even though it has smaller ZVS current since the right-hand term of (16), the capacitive energy of the MOSFET's output capacitor that should be discharged for ZVS operation, gets much smaller due to the decreased duty cycle.

D. Design Example

1) Auxiliary Inductor: The auxiliary inductor L_A is an important design parameter which determines ZVS turn ON of main switches. From (14) and (16), the minimumvalue of inductor L_A for ZVS turn ON of main switches can be obtained as shown in (18) at the bottom of the page. As L_A becomes large, the duty cycle should be increased to regulate the output voltage due to the voltage drop across L_A, leading to increased

$$L_A > \frac{V_i \cdot L \cdot [(A - V_i^2 \cdot D) \cdot (1-D)^2 \cdot \{2V_i - V_O \cdot (1-D)\} + 2B - 2\sqrt{B \cdot [(A - V_i^2 \cdot D) \cdot (1-D)^2 \cdot \{2V_i - V_O \cdot (1-D)\} + B]}]}{(A - V_i^2 \cdot D)^2 \cdot (1-D)^2} \tag{18}$$

where $A = P_O L f_S$ and $B = C_{os,\mathrm{tot}} V_i^3 L f_S^2$

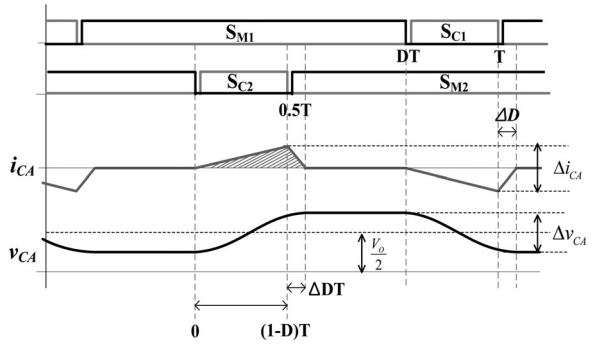

Fig. 8. Key waveforms of auxiliary capacitor C_A with $N = 1$ ($D > 0.5$).

voltage rating of switches. Therefore, L_A should be selected as small as possible once (18) issatisfied.

2) Auxiliary Capacitor: The key waveforms of auxiliary capacitor C_A with $N = 1$ are shown in Fig. 8. The peak-to-peak voltage ripple Δv_{CA} can be obtained by considering the shaded area of i_{CA} as shown in (19) at the bottom of the page. Rearranging (19) gives

$$\therefore C_A = \frac{\Delta i_{CA} \cdot (1 - D + \Delta D)}{4 \cdot \Delta v_{CA} \cdot f_S}. \tag{20}$$

E. Output Capacitor Voltages

The operating principles of the proposed converter with $N = 1$ discussed in the aforementioned sections can also be applied to the proposed converter with $N \geq 2$. The key waveforms of the proposed converter with $N = 2$ are shown in Fig. 9. In Fig. 9, only voltage and current waveforms associated with output capacitors are shown since the other waveforms are identical to case of $N = 1$. It should be noted that the current waveforms of each output capacitor are different each other, leading to unequal average values and ripple magnitudes of each output capacitor voltage in the multiplier cells. Fig. 10(a) shows the unbalance ratio which is sharply decreased by increasing output capacitances. Output capacitances are chosen to be 6 μF, and the unbalance ratios are smaller than 3.7%. The ripple ratio which is determined by capacitor ripple magnitude normalized to average value is shown in Fig. 10(b). The ripple ratios of all capacitor voltages are smaller than 6.6% with output capacitances of 6 μF. The ripple ratio of the total output voltage is 5%.

III. Performance Comparison

In this section, design examples of the proposed converter are presented to illustrate how to determine optimum number of N for given example specifications:

$$P_O = 1 \text{ kW},\ V_i = 48 \text{ V},\ V_O = 380 \text{ V}$$
$$f_S = 50 \text{ kHz},\ C_A = 9\ \mu\text{F},\ C_{1-3} = 6\ \mu\text{F}.$$

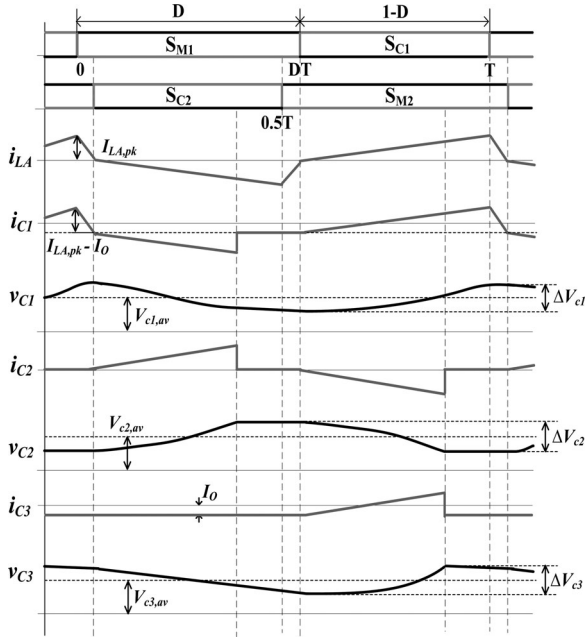

Fig. 9. Key waveforms of output capacitors with $N = 2$ ($D > 0.5$).

TABLE III
Component Rating Comparison ($P_O = 1$ kW, $V_i = 48$ V, $V_O = 380$ V, $C_A = 9\ \mu$F, $C_{1-3} = 6\ \mu$F)

Components	Design items	*N=1*	*N=2*
Switch	D	0.78	0.51
	V_{pk}	220V	102V
Diode	V_{pk}	385V	205V
Auxiliary Capacitor C_A	V_{av}	193V	100V
Output Capacitor $C_1 \sim C_3$	V_{av}	380V	197V 190V 184V

First, the duty cycle that affects voltage ratings of switches, diodes, and capacitors are calculated for several N using (8)–(10). It should be noted that choosing higher value of N reduces the required duty cycle, resulting in reduced voltage ratings of the component. However, this in turn increases the numbers of components. In case of $N > 2$, the operating duty cycle becomes smaller than 0.5, which causes hard-switched turn ON of main switches. The component ratings of the proposed converter with $N = 1$ and $N = 2$ are shown in Table III, respectively.

In this section, the proposed converter is compared to some of the recently introduced high step-up interleaved soft-switching converters [15]–[17]. The comparison has been performed in terms of the utilization factor of switching devices and energy volume of passive components, etc., and the results are listed in Table IV. In terms of switch and diode utilization factors of the topologies, [15] and [16] are the best, respectively. The switch utilization factor of the proposed converter is moderate. But

$$\Delta v_{CA} = \frac{1}{C_A}\left[\int_0^{(1-D)T}\left\{\frac{\Delta i_{CA}}{2(1-D)T}t\right\}dt + \int_{(1-D)T}^{(1-D+\Delta D)T}\left\{-\frac{\Delta i_{CA}}{2\cdot\Delta DT}t + \frac{\Delta i_{CA}(1-D+\Delta D)}{2\cdot\Delta D}\right\}dt\right] \tag{19}$$

TABLE IV
COMPARISON BETWEEN CONVENTIONAL HIGH STEP-UP CONVERTERS AND PROPOSED CONVERTER
(P_O = 1 kW, V_i = 48 V, V_O = 380 V, f_S = 50 kHz, $\Delta I_{\rm in}$ = 2%, ΔV_O = 5%)

		Reference [15]	Reference [16]	Reference [17]	Proposed
Chosen topology		Fig. 2	Fig. 6	Fig. 2 (d)	Fig. 1 with *N*=2
Operating duty cycle		0.64	0.66	0.72	0.51
Switches	V_{pk}, I_{pk}	2× 136V, 20.8A	144V, 20.5A 144V, 19A 144V, 18.6A 144V, 17A	190V, 37.1A 190V, 36A 121V, 12.6A	104V, 29.3A 104V, 28.8A 104V, 21.9A 104V, 20.4A
	q	2	4	3	4
	U※	0.1768	0.0925	0.0649	0.0958
	Switching method	ZCS	ZVS	ZVS	ZVS
Diodes	V_{pk}, I_{pk}	256V, 11A 256V, 9.7A 136V, 12.2A 136V, 11.7A	141V, 8.4A 137V, 13.6A 128V, 14.5A 120V, 7.9A	2× 737V, 7.6A	204V, 14.9A 193V, 13.9A 2× 185V, 14.8A
	q	4	4	2	4
	U※	0.1170	0.1709	0.0893	0.0893
	Reverse recovery losses	small	negligible	negligible	negligible
Filter inductors L_1,L_2		900uH	650uH	900uH	120uH
Output capacitors		2uF	5uF	1uF	6uF
Total energy volume of inductors (ΣLI^2)		0.03J	0.07J	0.1J	0.01J
Total energy volume of capacitors (ΣCV^2)		1.23J	2.74J	0.14J	0.76J

※ $\text{U(Utilization factor)} = \dfrac{P_O}{V_{pk} \times I_{pk} \times \text{q}}$, where q = number of components.

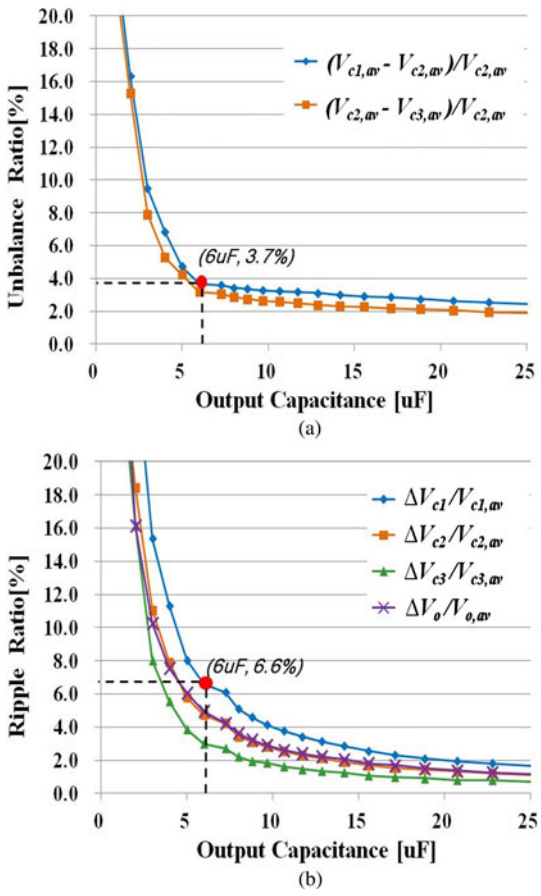

Fig. 10. Output capacitor voltages as a function of output capacitance (a) unbalance ratio and (b) ripple ratio (P_O = 1 kW, V_i = 48 V, V_O = 380 V).

the proposed converter and topology [17] have the lowest diode utilization factors. The reverse recovery loss of the topology [15] was alleviated, but somewhat larger compared to other topologies. The topology [17] has the smallest total energy volume of the capacitors, but the requirement for input current ripple was not satisfied even with the filter inductance larger than 900 μH. The topology [16] has the largest total energy volume of the capacitors.

IV. EXPERIMENTAL RESULTS

The proposed converter with $N = 1(N = 2)$ has been built in the laboratory. The system parameters used in the experiment is as follows:

$$P_O = 1\text{ kW},\ V_i = 48\text{–}60\text{ V},\ V_O = 380\text{ V},\ D = 0.78\ (0.51)$$
$$f_S = 50\text{ kHz},\ L = 720\ \mu\text{H}(120\ \mu\text{H}),\ L_A = 6.3\ \mu\text{H}$$
$$C_A = 9\ \mu\text{F},\ C_C = 3\ \mu\text{F},\ C_{1-3} = 6\ \mu\text{F}.$$

The component ratings along with the respective selected devices from the manufactures are provided in Table V. Fig. 11 shows experimental waveforms of the proposed converter. Fig. 11(a) shows the input current and two inductor currents illustrating the interleaving effect. As can be seen from Fig. 11(b) and (c) that both main and clamp switches are turned ON with ZVS. As is also seen from Fig. 11(d) that the diode is turned OFF with ZCS leading to negligible turn-off losses associated with reverse recovery characteristic.

Fig. 12 shows measured efficiency of the proposed converter. The peak measured efficiencies of the proposed converter with $N = 1$ and $N = 2$ are 97.6% at 400 W and 98.4% at 600 W,

TABLE V
COMPONENT RATINGS AND SELECTED DEVICES

Components		Rating	Selected devices
Main switches	V_{pk}	218V	IXFH52N30Q (300V, 52A)
	I_{rms}	14A	
Clamp switches	V_{pk}	218V	IXFH52N30Q (300V, 52A)
	I_{rms}	3A	
Diodes	V_{pk}	380V	C3D10060A (600V, 10A)
	I_{av}	2.7A	
Filter inductors L_1, L_2	Inductance	720/120uH	Powder core CH467125
	I_{rms}	11A	
Auxiliary inductor L_A	Inductance	6.3uH	Powder core CH400125
	I_{rms}	8.6A	
Clamp capacitor C_C	Capacitance	3uF	PCPW 225 3uF
	V_{pk}	218V	
	I_{rms}	4.2A	
Auxiliary capacitor C_A	Capacitance	9uF	PCPW 225 9uF
	V_{pk}	190V	
	I_{rms}	8.6A	
Output capacitors C_1~C_3	Capacitance	6uF	PCPW 225 6uF
	V_{pk}	380V	
	I_{rms}	5.5A	

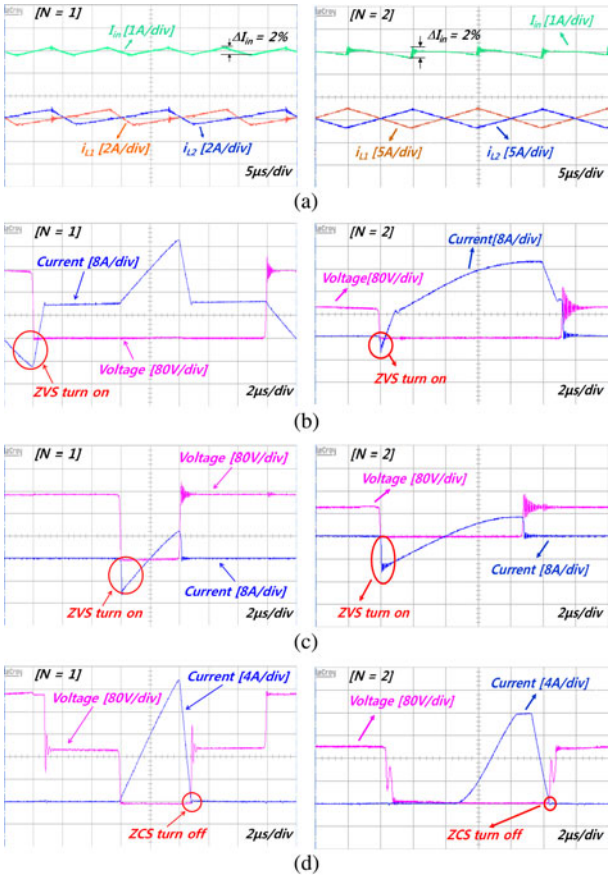

Fig. 11. Experimental waveforms of the proposed converter (a) input and inductor currents, (b) voltage and current waveforms of main switch, (c) voltage and current waveforms of clamp switch, and (d) voltage and current waveforms of diode.

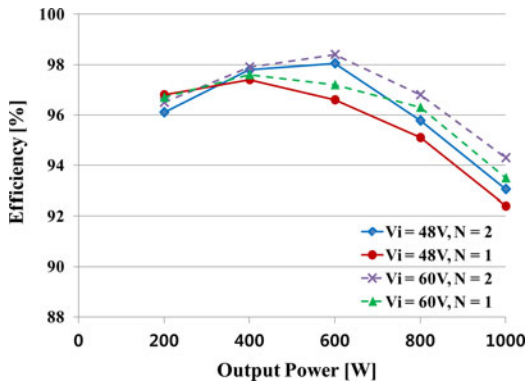

Fig. 12. Measured efficiency of the proposed converter.

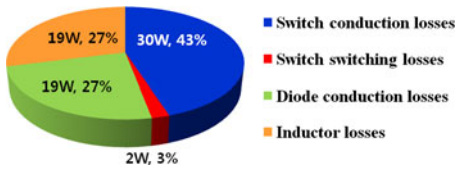

Fig. 13. Loss analysis of the proposed converter with $N = 2$ at full load.

respectively, when the input voltage V_i is 60 V. The measured full-load efficiencies of the proposed converter with $N = 1$ and $N = 2$ are 93.5% and 94.3%, respectively, when the input voltage V_i is 60 V. In case of $N = 1$ the switch conduction loss decreases, but the switch current at turn-off instant increases due to the increased duty cycle resulting in much increased turn-off switching losses. Since the turn-off switching loss is dominant the efficiency of the proposed converter with $N = 1$ is approximately 1% lower than that of the proposed converter with $N = 2$.

Fig. 13 shows loss analysis of the proposed converter with $N = 2$ at full load. The total loss of the proposed converter is 70 W. The large portion of the losses comes from switch and diode conduction losses, which are 43% and 27% of the total loss, respectively. The switching loss of switches is very small due to ZVS turn-on operation. The switching loss of diodes associated reverse recovery is negligible due to the ZCS turn-off operation.

V. CONCLUSION

This paper proposes a soft-switched dc–dc converter using voltage multiplier cells for high-step up application. The proposed converter employs two clamp switches which help not only clamp the voltage spikes caused by parasitic inductance, but also achieve ZVS turn ON of switches and ZCS turn OFF of diodes. The basic converter with $N = 1$ has doubled voltage conversion ratio compared to the conventional boost converter. Combining the basic converter with multiplier cells increases flexibility in device selection. The proposed converter is compared to some high step-up converters in terms of component ratings. Experimental results from a 1-kW prototype are provided to validate the proposed concept.

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