# A Family of ZVT DC–DC Converters With Low-Voltage Ringing

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***Abstract*—In this paper, a new low-voltage ringing zero voltage transition (ZVT) cell is proposed for a family of non-isolated dc–dc converters. In the proposed converter, all semiconductor devices operate under soft-switching condition at both turning ON and OFF. The proposed ZVT cell resolves the issues appeared in the previous works: no online calculation required to achieve ZVS turn-ON of the main switch; no extra voltage stress imposed on the main or snubber components; no floating gate driver required for the main and snubber switches; low component count of the ZVT cell; operation principles and design guideline of the boost converter with the proposed ZVT cell are presented. Also, three different positions of a snubber diode considering its junction capacitor are analyzed to clarify the advantage of the proposed ZVT cell. A 2-kW laboratory prototype of the boost converter with the proposed ZVT cell operating at 100 kHz is built and tested to verify the theoretical analysis. Finally, a comparative analysis is given to demonstrate the superiority of the proposed converter.**

***Index Terms*—Active snubber, dc–dc converter, junction capacitor, zero voltage switching (ZVS), zero voltage transition (ZVT).**

## I. Introduction

NON-ISOLATED pulsewidth modulation dc–dc converters (NPDC) such as buck, boost, Cúk, and SEPIC have been widely used in many applications due to their simple structure and ease of control [1]–[3]. However, switching loss, electromagnetic interference noise, and voltage surge associated with the hard-switching operation are the major drawbacks of these converters, which limits their use in high-frequency applications. Regarding the above-mentioned issues, the soft-switching technique is a key solution. Furthermore, increasing the switching frequency leads to high power density and fast dynamic performance.

A well-known method to achieve soft switching is by integrating an active snubber cell (ASC) into the NPDC converter [4]–[32]. The ASC operates only at a small fraction of a whole operating period under a constant switching frequency. Therefore, the converter using the ASC can stay in the pulsewidth modulation (PWM) control method. Moreover, the component ratings of the ASC are much smaller than those of the main circuit, which results in a small portion of the whole converter volume.

Usually, the ASCs can be divided into zero voltage transition (ZVT) [4]–[26] and zero current transition (ZCT) [27]–[32] cells, according to the switching characteristic of the main switch in the converter. The ZVT (ZCT) cell provides complete ZVS turn-ON (ZCS turn-OFF) for the main switch, and therefore, it is preferred for the converters using MOSFETs (IGBTs) as a switching device. For the sake of operating the converter in high switching frequency, MOSFETs are normally used. Therefore, this paper focuses mainly on the ZVT cells.

In the literature, a large number of the ZVT cells have been presented with the ability to provide soft-switching condition for the NPDC converters.

The converters proposed in [8] achieve complete ZVS turn-ON of the main switch and ZCS turn-OFF of the main diode. However, a major drawback is that gate turn-ON for ZVS of the main switch varies according to the load, and therefore, the online calculation for accurate timing control is required, which makes the controller complicated. The online calculation becomes more critical in the high-frequency applications due to limitations on the speed of the microcontroller. Furthermore, the main switch in this converter turns OFF under hard-switching condition.

The topology in [18] provides fully soft-switched operation for both main and snubber switches. Also, all the diodes turn OFF under ZCS condition. Moreover, only one more diode is in need for each additional interleaved phase, which makes it suitable for high power applications. However, extra voltage stress is imposed on the snubber switch. Besides, the snubber circuit employs two auxiliary inductors that increase the converter size and cost.

Although the ZVT cell in [13] has lower component count compared to the aforementioned converters, they require floating gate drivers for main and snubber switches. Moreover, an extra capacitor is connected in parallel to the main switch to reduce the turn-OFF loss, which makes ZVS turn-ON of the main switch failed at the light load condition.

The converters in [12] and [20] utilize many auxiliary components that contribute to circuit complexity as well as high volume and cost.

Several interesting ZVT cells introduced in [5]–[7], [10], and [11] provide fully soft-switched operation for all of the semiconductor devices of the boost converter. However, the peak voltage of the snubber diodes is twice of the output voltage due to the

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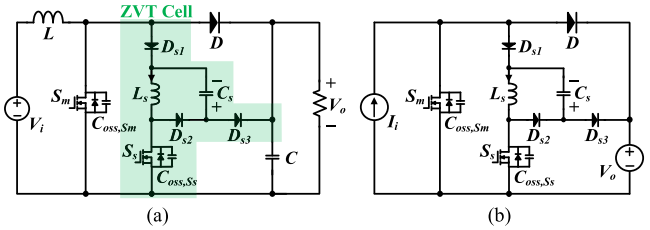


Fig. 1. Boost converter with the proposed ZVT cell. (a) General structure. (b) Equivalent circuit.

ringing cause by the resonance between the snubber inductor and the junction capacitor of the snubber diodes, which results in higher cost and conduction losses, and makes the converter unrealizable in high output voltage applications. The cause of the voltage ringing will be detailed in Section III. Additionally, while the converter in [11] has high component count, the snubber switches of [6] and [10] have to turn ON and OFF two times during one switching cycle of the main switch, which increases the related loss resulting in reducing the benefits of the snubber circuit.

From the brief overview mentioned above, it can be seen that the previously presented ZVT cells have at least one of the following drawbacks.

1) Online calculation is required to achieve ZVS turn-ON.
2) Extra voltage stresses are imposed on the snubber components.
3) Snubber circuit has a high component count.
4) Floating gate driver is required for the main and snubber switches.

In this paper, a ZVT cell for the family of NPDC is proposed. The proposed ZVT cell is able to resolve all the above-mentioned problems: It provides the soft-switching condition for all the semiconductor devices without any extra voltage and current stresses; neither floating gate driver nor online calculation is required; the number of components in the ZVT cell is acceptable.

Three possible positions of the snubber diode considering its junction capacitor are analyzed to clarify the advantages of the proposed ZVT cell, which have not been investigated in the previous work. Theoretical analysis of the boost converter with the proposed ZVT cell is presented. Then, the soft-switching conditions are discussed, and the design procedures for the ZVT cell are introduced. In addition, other family members of the proposed converter and their variants are developed. Finally, the 2-kW laboratory prototype of the boost converter with the proposed ZVT cell is built and tested to verify the theoretical analysis.

## II. Proposed ZVT Cell

Fig. 1(a) shows the circuit diagram of the boost converter with the proposed ZVT cell. Inductor *L*, capacitor *C*, diode *D*, and switch $S_m$ are the main components of the boost converter. The proposed ZVT cell is shown in the shaded block, which consists of snubber switch $S_s$, snubber inductor $L_s$, snubber capacitor $C_s$, and snubber diodes $D_{s1}$, $D_{s2}$, and $D_{s3}$. $C_{oss,Sm}$

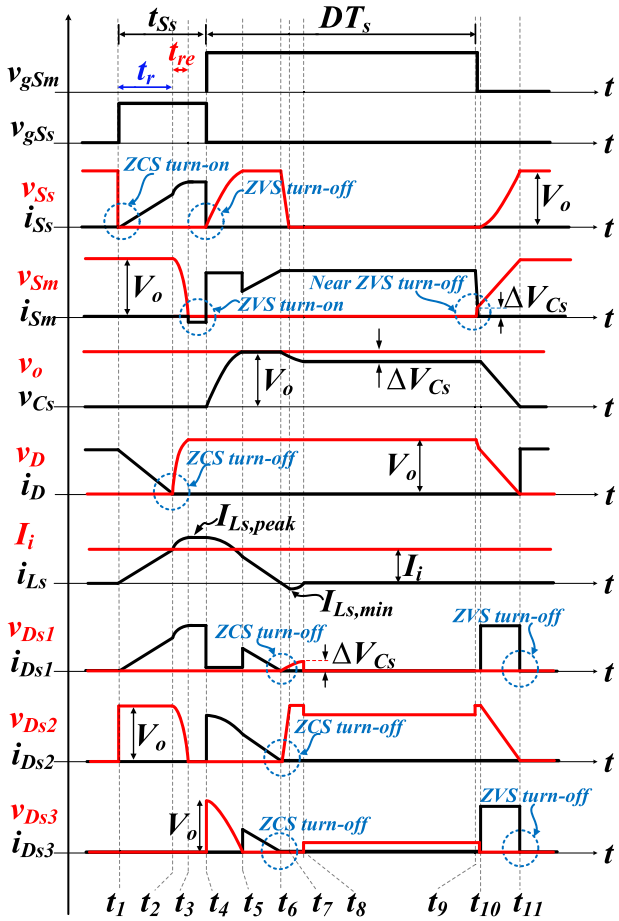


Fig. 2. Key waveforms of the boost converter with the proposed ZVT cell.

and $C_{oss,Ss}$ represent the parasitic capacitors of main switch $S_m$ and snubber switch $S_s$, respectively. The snubber switch turns ON for a short duration before the main switch turns ON and turns OFF simultaneously with the main switch turn-ON. While the snubber inductor ensures ZCS operation of the snubber switch and the main diode by limiting *di/dt* at the transition, the snubber capacitor reduces turn-OFF losses of the switches. Under the turn-ON condition of $S_s$, parasitic capacitor $C_{oss,Sm}$ of the main switch resonates with snubber inductor $L_s$, and then the body diode of the main switch turns ON, which causes ZVS turn-ON of the main switch.

For the sake of simplicity of the steady-state operation analysis of the converter, the following assumptions are made: The output capacitor and input inductor are large enough to make constant output voltage and input current; the turn-ON loss of the snubber switch associated with stored energy in the MOSFET's output capacitor $C_{oss,Ss}$ is negligible; all the passive components are ideal. The equivalent circuit of the proposed converter according to these assumptions is shown in Fig. 1(b). There are 11 operating modes in one switching cycle, and the equivalent circuits and the key waveforms for each mode are shown in Figs. 2 and 3, respectively. The explanation for each operating mode is given as follows.

1) *Mode 0 (before snubber switch turns ON)*: Prior to $t_1$, the converter is operating as normal OFF-state. Main switch

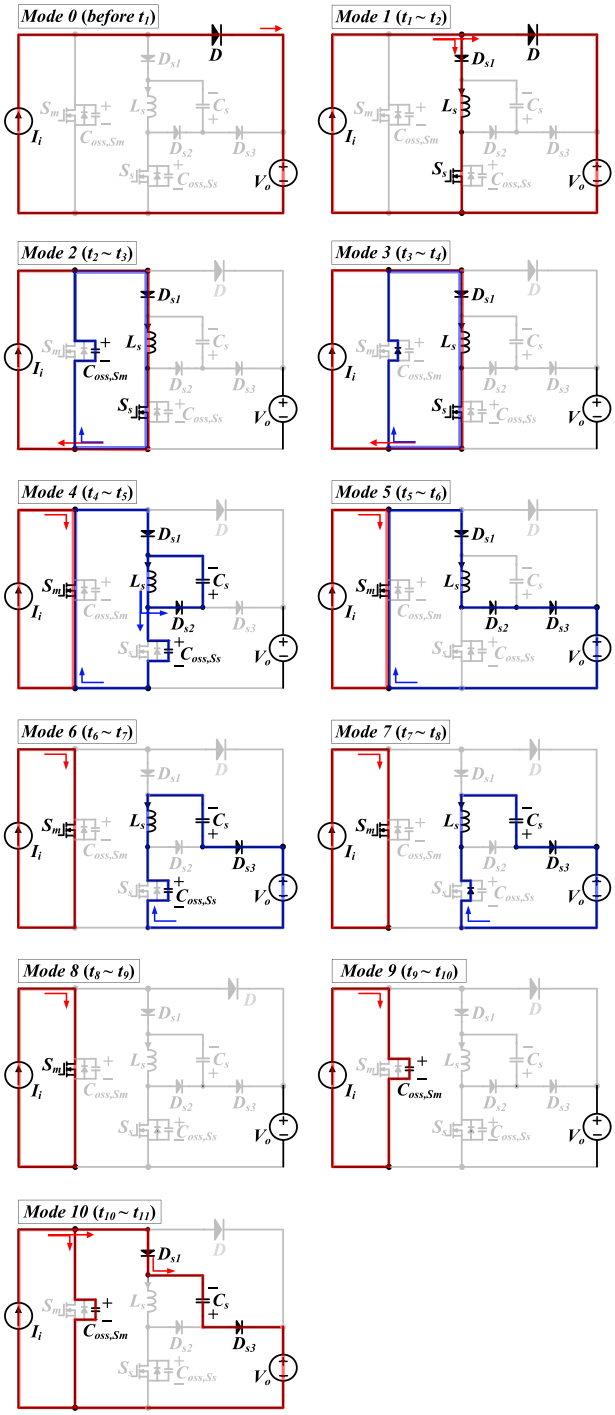


Fig. 3. Equivalent circuits of the operating modes.

and snubber switch are in the OFF-state, and main diode is in the ON-state, conducting the input current to the load. This mode ends when the snubber switch $S_s$ turns ON at time $t = t_1$.

2) *Mode 1 ($t_1$–$t_2$):* At $t_1$, snubber switch $S_s$ is turned ON, and current $i_{Ls}$ increases linearly with the slope determined as follows:

$$\frac{di_{Ls}}{dt} = \frac{V_o}{L_s}. \tag{1}$$

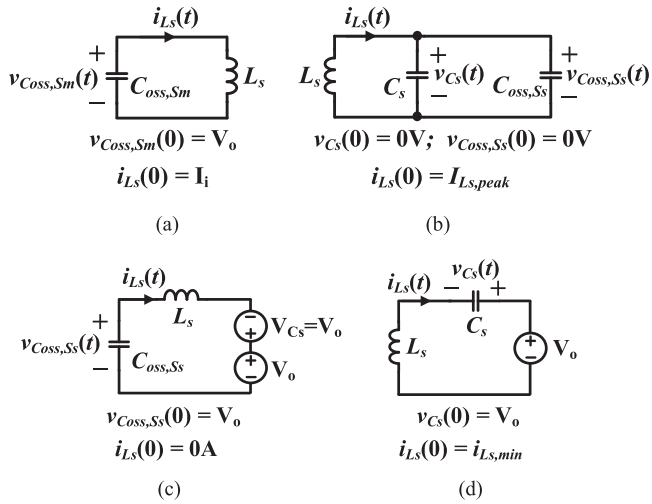


Fig. 4. Equivalent resonant circuits: (a) *Mode 2*. (b) *Mode 4*. (c) *Mode 6*. (d) *Mode 7*.

The current is being diverted away from main diode $D$. It is noted that the snubber switch $S_s$ turns ON with ZCS at $t_1$ and main diode $D$ turns OFF with ZCS at $t_2$ due to series connection of switch $S_s$ and inductor $L_s$. This mode ends at $t_2$ when $i_{Ls}$ and $i_D$ reach input current $I_i$ and zero, respectively. The time interval from $t_1$ to $t_2$ in Fig. 2 can be obtained from (1) by

$$t_r = t_2 - t_1 = \frac{I_i}{V_o} L_s = \frac{P_o}{V_i V_o} L_s. \tag{2}$$

3) *Mode 2 ($t_2$–$t_3$):* At $t_2$, the main diode turns OFF, and then $L_s$ and $C_{oss,Sm}$ start to resonate. At the end of this mode, all the energy stored in $C_{oss,Sm}$ is transferred to $L_s$. The voltage across $C_{oss,Sm}$ is discharged to zero while the current of snubber inductor $L_s$ is charged to maximum value $I_{Ls,\text{peak}}$. The equivalent resonant circuit of this mode is shown in Fig. 4(a). The current and voltage of the resonant components are determined, respectively, as follows:

$$i_{Ls}(t) = I_i + V_o \sqrt{\frac{C_{oss,Sm}}{L_s}} \sin(\omega_1 (t - t_2)), t_2 < t < t_3 \tag{3}$$

$$v_{\text{Coss},Sm}(t) = V_o \cos(\omega_1 (t - t_2)), \quad t_2 < t < t_3 \tag{4}$$

where $\omega_1 = 1/\sqrt{L_s C_{oss,Sm}}$. From (3), $I_{Ls,\text{peak}}$ can be obtained at time $t = t_3$ by

$$I_{Ls,\text{peak}} = I_i + V_o \sqrt{\frac{C_{oss,Sm}}{L_s}}. \tag{5}$$

This mode takes a quarter of the resonant cycle caused by $C_{oss,Sm}$ and $L_s$; therefore, the time duration of this mode can be calculated as

$$t_{re} = t_3 - t_2 = \frac{\pi}{2} \sqrt{L_s C_{oss,Sm}}. \tag{6}$$

4) *Mode 3 ($t_3$–$t_4$):* This mode begins when the voltage across $C_{oss,Sm}$ reaches to zero at time $t = t_3$, which makes the body diode of the main switch to turn ON.

Thus, the voltage across $S_m$ and $L_s$ are clamped to zero, and $i_{Ls}$ is maintained at $I_{Ls,\text{peak}}$. As a result, the main switch $S_m$ is ready to turn ON with ZVS. The current passing through the body diode of $S_m$ during this mode becomes$I_{Ls,\text{peak}} - I_i$.

5) *Mode 4 ($t_4$–$t_5$):* At $t_4$, the gating signals of main switch $S_m$ and snubber switch $S_s$ are applied and removed, simultaneously, and then $S_m$ and $S_s$ turn ON and OFF with ZVS. After $S_s$ turns OFF, diode $D_{s2}$ is turned ON, and a resonant operation begins between $C_s + C_{oss,Ss}$ and $L_s$. The equivalent resonant circuit of this mode is shown in Fig. 4(b). During this resonance, $v_{Coss,Ss}$ and $v_{Cs}$ are charged from zero to $V_o$ by $i_{Ls}$. The equations that describe this resonant stage are given as follows:

$$i_{Ls}(t) = I_{Ls,\text{peak}}\cos(\omega_2(t-t_4)), \quad t_4 < t < t_5 \tag{7}$$

$$v_{\text{Coss},Ss}(t) = v_{Cs}(t) = I_{Ls,\text{peak}}\sqrt{\frac{L_s}{C_s + C_{oss,Ss}}}\sin(\omega_2(t-t_4)),\ t_4 < t < t_5 \tag{8}$$

where $\omega_2 = 1/\sqrt{L_s(C_s + C_{oss,Ss})}$. The time duration of this resonant mode is

$$t_5 - t_4 = \sqrt{L_s(C_s + C_{oss,Ss})}\sin^{-1}\left(\frac{V_o}{I_{Ls,\text{peak}}\sqrt{\frac{L_s}{C_s + C_{oss,Sm}}}}\right). \tag{9}$$

In fact, the turn-OFF voltage of the snubber switch mostly depends on $C_s$ and $L_s$ due to much smaller capacitance of $C_{oss,Ss}$ compared to $C_s$. This mode ends when $v_{Cs}$ and $v_{\text{Coss},Ss}$ reach to $V_o$ at time $t = t_5$, which makes $D_{s3}$ forward biased.

6) *Mode 5 ($t_5$–$t_6$):* Diode $D_{s3}$ turns ON at $t_5$, and the energy stored in snubber inductor $L_s$ is transferred to the load. At the end of this mode, current $i_{Ls}$ reduces to zero at time $t = t_6$, which causes $D_{s1}$, $D_{s2}$, and $D_{s3}$ to turn OFF under ZCS condition.

7) *Mode 6 ($t_6$–$t_7$):* At $t_6$, $C_{oss,Ss}$ and $L_s$ start resonating. The equivalent resonant circuit of this mode is shown in Fig. 4(c). Since $C_s \gg C_{oss,Ss}$, $V_{Cs}$ is considered constant during this resonant mode. Therefore, the voltage and current of the resonant components are determined, respectively, as follows:

$$i_{Ls}(t) = -V_o\sqrt{\frac{C_{oss,Ss}}{L_s}}\sin(\omega_3(t-t_6)), \quad t_6 < t < t_7 \tag{10}$$

$$v_{\text{Coss},Ss}(t) = V_o\cos(\omega_3(t-t_6)), \quad t_6 < t < t_7 \tag{11}$$

where $\omega_3 = 1/\sqrt{L_s \cdot C_{oss,Ss}}$. This mode ends when the voltage across $C_{oss,Ss}$ reaches to zero, and the current through $L_s$ reaches minimum values $I_{Ls,\min}$, which can be obtained from (10) by

$$I_{Ls,\min} = -V_o\sqrt{\frac{C_{oss,Ss}}{L_s}}. \tag{12}$$

The time duration of this mode can be calculated by the following equation:

$$t_7 - t_6 = \frac{\pi}{2}\sqrt{L_s C_{oss,Ss}}. \tag{13}$$

8) *Mode 7 ($t_7$–$t_8$):* At $t_7$, body diode of the snubber switch is turned ON. A resonant starts between $L_s$ and $C_s$, and the equivalent resonant circuit of this mode is shown in Fig. 4(d). The current and voltage equations of $L_s$ and $C_s$ are determined, respectively, as follows:

$$i_{Ls}(t) = I_{Ls,\min}\cos(\omega_4(t-t_7)), \quad t_7 < t < t_8 \tag{14}$$

$$v_{Cs}(t) = V_o + I_{Ls,\min}\sqrt{\frac{L_s}{C_s}}\sin(\omega_4(t-t_7)), t_7 < t < t_8 \tag{15}$$

where $\omega_4 = 1/\sqrt{L_s C_s}$. This mode ends when current $i_{Ls}$ reaches to zero. Therefore, the time duration of this mode can be calculated by the following equation:

$$t_8 - t_7 = \frac{\pi}{2}\sqrt{L_s C_s}. \tag{16}$$

During this mode, voltage across $C_s$ is discharged a value of $\Delta V_{Cs}$, which can be determined from (12), (15), and (16) by

$$\Delta V_{Cs} = V_o\sqrt{\frac{C_{oss,Ss}}{C_s}}. \tag{17}$$

9) *Mode 8 ($t_8$–$t_9$):* During this mode, main switch $S_m$ is conducting the input current, and all the semiconductor devices of the snubber circuit are in the OFF-state. The converter is operating as the normal ON-state of the conventional boost converter. This mode ends when the switch $S_m$ turns OFF at time $t = t_9$.

10) *Mode 9 ($t_9$–$t_{10}$):* At $t_9$, main diode $D$ and snubber diode $D_{s1}$ are still reverse biased and kept in the OFF-state. Input current $I_i$ charges parasitic capacitor $C_{oss,Sm}$ to the value of $\Delta V_{Cs}$. It is noted that the main switch turns OFF under near ZVS since $\Delta V_{Cs}$ is much smaller than $V_o$, as can be seen from (17). This mode ends when voltage $v_{\text{Coss},Sm}$ reaches to $\Delta V_{Cs}$. The time duration of this mode can be obtained by

$$t_{10} - t_9 = \frac{\Delta V_{Cs}}{I_i}C_{oss,Sm}. \tag{18}$$

11) *Mode 10 ($t_{10}$–$t_{11}$):* This mode begins when diodes $D_{s1}$ and $D_{s3}$ turn ON. Parasitic capacitor $C_{oss,Sm}$ is charged while snubber capacitor $C_s$ is discharged by input current $I_i$. The voltages and currents of the components in this mode can be obtained as follows:

$$v_{Cs}(t) = V_o - \Delta V_{Cs} - \frac{I_{\text{in}}}{C_s + C_{oss,Sm}}(t - t_{10}) \tag{19}$$

$$v_{\text{Coss},Sm}(t) = V_o - v_{Cs}(t). \tag{20}$$

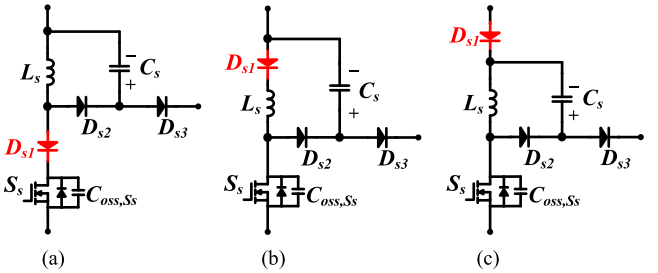


Fig. 5. Three possible positions of diode $D_{s1}$. (a) *Position I*. (b) *Position II*. (c) *Position III* (*Proposed*).

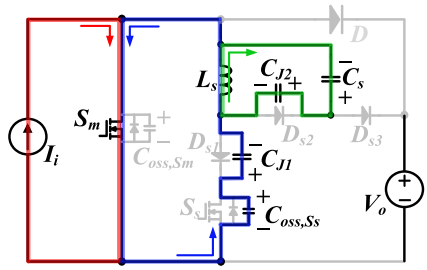


Fig. 6. Equivalent circuit of *Mode 6* corresponding to *Position I*.

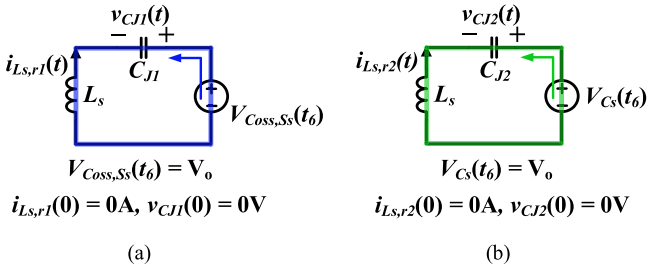


Fig. 7. Two resonant loops of *Mode 6* corresponding to *Position I*. (a) *Resonant loop 1*. (b) *Resonant loop 2*.

This mode ends when the voltage across parasitic capacitors $C_{oss,Sm}$ reaches to $V_o$ while the voltage across $C_s$ reduces to zero. Because of $C_{oss,Sm} << C_s$, the time duration of this mode can be calculated approximately as

$$t_{11} - t_{10} = C_s \frac{V_o - \Delta V_{Cs}}{I_{\text{in}}}. \tag{21}$$

After this mode, a next switching cycle begins and main diode $D$ conducts current from source to the load like the normal OFF-state of the conventional boost converter.

According to (8) and (19), the turn-OFF voltage waveforms of the both main and snubber switches depend mostly on the charging and discharging of the snubber capacitor $C_s$ due to the much smaller capacitance of the parasitic capacitors compared to the snubber capacitor. Thus, with the proposed ZVT cell, soft-switching turn-OFF for both switches are achieved without adding the extra capacitor to the MOSFETs, resulting in lower energy to provide ZVS turn-ON for the main switch. Therefore, the converter with the proposed ZVT cell achieves ZVS turn-ON within a wide range of load.

## III. Performance Comparison According to Position of the Blocking Diode

In this section, the effect of the position of the blocking diode $D_{s1}$, considering its junction capacitor, and the advantage of the proposed ZVT cell over the previous works, which have different positions of the blocking diode, will be analyzed. The main function of the blocking diode is as follows. At $t = t_7$, the current conducting in the snubber inductor $L_s$ is negative, as presented in the previous section. If there is no blocking diode $D_{s1}$, the negative current of inductor $L_s$ with the value of $I_{Ls,\min}$ will flow in a loop included inductor $L_s$, main switch $S_m$, and body diode of snubber switch $S_s$. This current circulates until $S_m$ turns OFF, which results in increased current rating and conduction loss of the converter. Therefore, the blocking diode is essential in eliminating the circulating current. Now, regarding the positions of the blocking diode, three possible positions (*I*, *II*, and *III*) could be considered to locate diode $D_{s1}$, as shown in Fig. 5. Operation principles of the converter with three different positions of $D_{s1}$ are nearly the same except *Mode 6*, which has a strong effect on the quality of the converter. The difference in the three positions will be detailed as follows.

### A. Position I

In this case, the position of $D_{s1}$ is similar to that of the snubber circuits presented in [7] and [11]. With this configuration, the resonant operations of *Mode 6* in the previous section change into two different resonant loops, as shown in Figs. 6 and 7.

1) *Resonant loop 1:* As shown in Fig. 7(a), junction capacitor $C_{J1}$ of the blocking diode, and snubber inductor $L_s$ start resonating and resonant current $i_{Ls1}$ flows through $C_{J1}$, $L_s$, $C_{oss,Ss}$, and $S_m$. During the resonance mode, the voltage across the snubber switch is assumed to be constant and equal to $V_o$ since $C_{oss,Ss}$ is of larger capacitance if compared with $C_{J1}$.The voltage and current of the resonant components are determined, respectively, as follows:

$$v_{C_{J1}}(t) = V_o(1 - \cos(\omega_5(t - t_5)), \quad t_5 < t < t_6 \tag{22}$$

$$i_{Ls,r1}(t) = -V_o\sqrt{\frac{C_{J1}}{L_s}}\sin(\omega_5(t - t_5)), \quad t_5 < t < t_6 \tag{23}$$

where $\omega_5 = 1/\sqrt{L_s C_{J1}}$. The maximum voltage stress applying to diode $D_{s1}$ can be obtained from (22) by

$$V_{C_{J1,\max}} = 2V_o. \tag{24}$$

2) *Resonant loop 2:* As shown in Fig. 7(b), the other resonance occurs between inductor $L_s$ and junction capacitor $C_{J2}$ of snubber diode $D_{s2}$. Resonant current $i_{Ls,r2}$ flows through $L_s$, $C_s$, and $C_{J2}$. The capacitor $C_s$ in this case is considered as a constant voltage source with the value of $V_o$. The equations that describe the voltage and current in

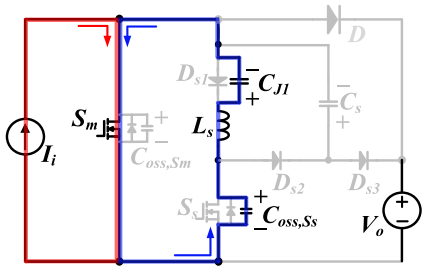


Fig. 8. Equivalent circuit of *Mode 6* corresponding to *Position II*.

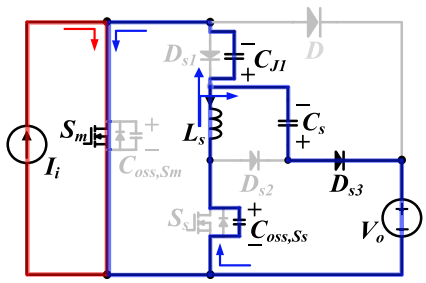


Fig. 9. Equivalent circuit of *Mode 6* corresponding to *Position III*.

this resonant loop can be written as follows:

$$v_{C_{J2}}(t) = V_o(1 - \cos(\omega_6(t - t_5)), \quad t_5 < t < t_6 \tag{25}$$

$$i_{Ls,r2}(t) = -V_o\sqrt{\frac{C_{J2}}{L_s}}\sin(\omega_6(t - t_5)),\ t_5 < t < t_6 \tag{26}$$

where $\omega_6 = 1/\sqrt{L_s C_{J2}}$.The maximum voltage stress applying to diode $D_{s2}$ can be obtained from (25) by

$$V_{C_{J2,\max}} = 2V_o. \tag{27}$$

As seen in (24) and (27), the voltage rating of both snubber diodes $D_{s1}$ and $D_{s2}$ is twice of the output voltage, which increases the cost and loss of the snubber circuit and makes the converter unrealizable in the high output voltage applications.

### B. Position II

In this case, the configuration of the ZVT cell, which can be seen in Fig. 5(b), has the same position of the blocking diode as presented in [5], [6], and [10]. Assuming that the voltage across parasitic capacitor $C_{oss,Ss}$ is constant at $V_o$ during the resonant operation, the voltage across diode $D_{s2}$ is clamped to zero since $v_{Ds2} = V_{Cs} - v_{\mathrm{Coss,Ss}}$ at $t = t_6$. Therefore, *resonant loop 2* described in *Position I* does not occur. The equivalent resonant circuit of *Mode 6* corresponding to *Position II* is shown in Fig. 8, which is the same as the *resonant loop 1* as presented above. By doing a similar analysis to the *resonant loop 1*, the maximum voltage stress applied to diodes $D_{s1}$ is shown to be twice of the output voltage. Besides that, diode $D_{s1}$ in the case of *Position II* must conduct for a longer time compared to *Position I* to dissipate all the snubber inductor energy in the circuit, which results in larger current rating and conduction loss.

### C. Position III (Proposed)

This is the case of the proposed ZVT cell, and the operation principles were presented in detail in Section II. Considering the junction capacitor of diode $D_{s1}$, the equivalent circuit of the converter during *Mode 6* is shown in Fig. 9. The amplitude of the ringing voltage caused by the resonant loop between $C_{J1}$ and $L_s$ is low since the voltage across $C_{J1}$ is clamped to $V_o - v_{Cs}$, as seen in Fig. 9. Therefore, the maximum voltage stress of diode $D_{s1}$ that occurs at the end of *Mode 7* is $\Delta V_{Cs}$, which is much smaller than the output voltage. Simulation results of the voltage waveforms of snubber switch $S_s$, diodes $D_{s1}$, and $D_{s2}$ in three different positions considering the junction capacitors are shown in Fig. 10 in which the proposed ZVT has much lower voltage ringing of the snubber diodes compared to *Positions I* and *II*. The comparison between three different positions of diode $D_{s1}$ in the converter is given in Table I.

## IV. Design Procedures of the Proposed ZVT Cell

The ZVT cell is designed to achieve soft-switching operation of the main and snubber switch, which results in soft-switching operation of all diodes. Due to simple structure of the snubber circuit, only snubber inductor $L_s$ and snubber capacitor $C_s$ need to be designed.

### A. Snubber Inductor Design

The value of snubber inductor $L_s$ determines the ratio *di/dt* of the snubber switch current at turn-ON instant. According to Fig. 2, in order to provide ZVS turn-ON for the main switch, the following relationship should be satisfied for turn-ON time of snubber switch $t_{Ss}$:

$$t_{Ss} \geq t_r + t_{re}. \tag{28}$$

Based on (2), (6), and (28), the inductance value of the snubber inductor can be selected by

$$L_s \leq \left(\frac{-b + \sqrt{\Delta}}{2a}\right)^2 \tag{29}$$

where

$$\Delta = b^2 - 4ac,\ a = \frac{I_i}{V_o},\ b = \frac{\pi}{2}\sqrt{C_{oss,Sm}},\ c = -t_{Ss}. \tag{30}$$

According to (29) and (30), in order to determine the value of $L_s$, $t_{Ss}$ should be selected in advance. Due to the advantage of no timing issue, the online calculation of $t_{Ss}$ is not necessary, which makes the selection of $t_{Ss}$ simple. The following are the procedures to select $t_{Ss}$. First, for significant reduction of the reverse recovery loss of main diode $D$, rising time $t_r$ of the snubber inductor current during *Mode 1* should be greater than three times $t_{rr}$, which is the reverse recovery time of the diode $D$ [5], [7]. Considering the resonant time $t_{re}$ of *Mode 2*, $t_{Ss}$ is maintained five times larger than $t_{rr}$. Second, $t_{Ss}$ should be small enough to guarantee the small size and low conduction loss of the snubber circuit; therefore, it is preferred to select $t_{Ss}$

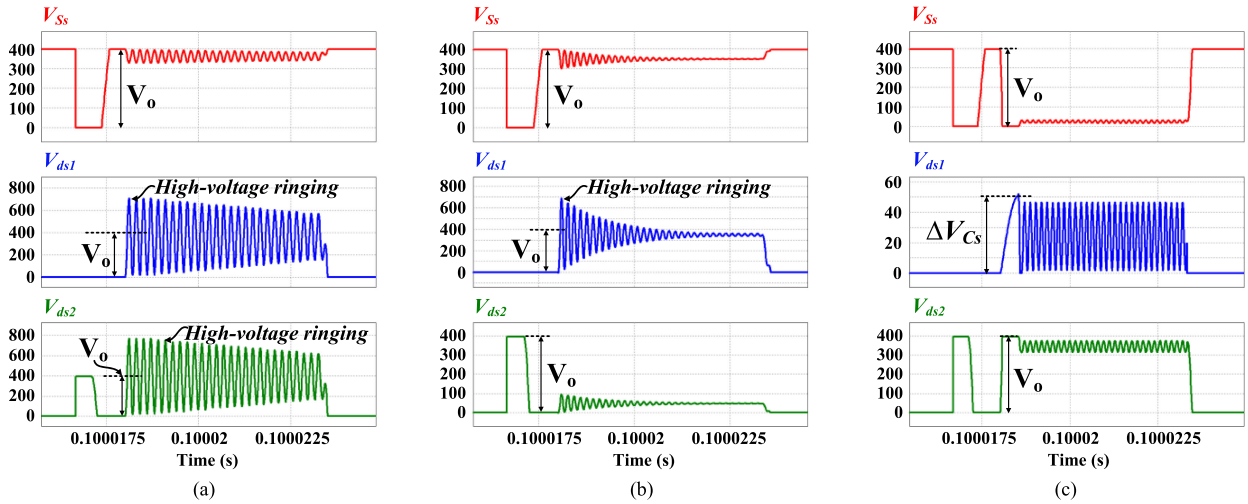


Fig. 10. Simulation waveforms of $V_{Ss}$, $V_{Ds1}$, and $V_{Ds2}$. (a) *Position I*. (b) *Position II*. (c) *Position III* (*Proposed*).

TABLE I
COMPARISON BETWEEN THREE POSSIBLE POSITIONS OF DIODE $D_{s1}$

| Features | *Position I* [7] [11] | *Position II* [5] [6] [10] | *Position III* (Proposed) |
|---|---|---|---|
| Voltage rating of $D_{s1}$ | $2V_o$ | $2V_o$ | $\Delta V_{Cs}$ |
| Voltage rating of $D_{s2}$ | $2V_o$ | $V_o$ | $V_o$ |

TABLE II
DESIGN SPECIFICATION OF THE PROPOSED CONVERTER

| Parameters | values |
|---|---|
| Input voltage $V_i$ [V] | 150 |
| Output voltage $V_o$ [V] | 400 |
| Output power $P_o$ [W] | 2000 |
| Switching frequency $f_s$ [kHz] | 100 |

smaller than ten times switching period $T_s$ of the boost converter. Consequently, $t_{Ss}$ is restricted by

$$5t_{rr} \le t_{Ss} \le \frac{1}{10}T_s. \tag{31}$$

After $t_{Ss}$ is selected, the value of $L_s$ can be obtained from (29) and (30) at the maximum input current, which is the worst case condition as

$$L_s \le \left( \frac{-\frac{\pi}{2}\sqrt{C_{oss,Sm}} + \sqrt{\frac{\pi^2}{4}C_{oss,Sm} + 4\frac{I_{i,\max}}{V_o}t_{Ss}}}{2\frac{I_{i,\max}}{V_o}} \right)^2. \tag{32}$$

## B. Snubber Capacitor Design

Snubber capacitor $C_s$ limits *dv/dt* of snubber switch $S_s$ during its turn-OFF period. Moreover, $C_s$ determines turn-OFF voltage $\Delta V_{Cs}$ of main switch $S_m$ during *Mode 9* since parasitic capacitor of the snubber switch $C_{oss,Ss}$ is already known by selecting the snubber switch in advance. The design of a snubber capacitor is as follows. First, assuming that $\Delta V_{Cs} \le \alpha V_o$, then the lower limit of $C_s$ can be obtained from (17) by

$$C_s \ge \frac{C_{oss,Ss}}{\alpha^2}. \tag{33}$$

Second, in order to achieve near ZVS turn-OFF for the main switch, the voltage across snubber capacitor $C_s$ should be charged to at least $(V_o - \Delta V_{Cs})$ at the end of *Mode 4* by the stored energy of a snubber inductor $L_s$, which can be expressed as

$$L_s i_{Ls,\text{peak}}^2 \ge C_s (V_o - \Delta v_{Cs})^2. \tag{34}$$

Therefore, the upper limit of $C_s$ can be determined from (34) by

$$C_s \le L_s \frac{i_{Ls,\text{peak}}^2}{(V_o - \Delta v_{Cs})^2}. \tag{35}$$

Finally, the snubber capacitor $C_s$ can be selected based on the restriction of (33) and (35).

## C. Design Example

In this section, a design example of the proposed ZVT cell used in the boost converter is given. The specifications of the proposed converter are shown in Table II. Input current and output voltage are assumed to be constant current source and voltage source, respectively; for this reason the design of input inductor and output capacitor is not taken into consideration. The voltage rating of the components is the same as the output voltage. Therefore, only the current ratings of the utilized components are calculated in this design example.

1) *Turn-ON time of the snubber switch* $t_{Ss}$: In general, the reverse recovery time of the main diode is within several tens of nanoseconds, therefore, based on the selected switching frequency and (31), $t_{Ss} \le 1$ $\mu$s is determined. If $t_{Ss}$ is too short, the inductance of the snubber inductor will be small. This makes the ZVS turn-ON of the main switch

fail at the light load. However, if $t_{Ss}$ is too long, the conduction loss on the snubber components will be high. For this reason, $t_{Ss} = 700$ ns is selected in this paper.

2) *Snubber inductor*: Based on the selection of the main switch, the maximum value of the snubber inductor is determined according to (32) as $L_s \leq 17.3\ \mu$H. To minimize the freewheeling interval as presented in Section II, $L_s$ should be selected as close as possible to the maximum value, and therefore, in this paper, $L_s = 15\ \mu$H is selected.

3) *Snubber switch*: According to Fig. 2, the current of the snubber switch is considered as a rectangular waveform with the peak value being obtained from (5) as $I_{Ls,\text{peak}} = 15.2$ A. Hence, the *rms* current of the snubber switch can be approximated as follows:

$$I_{Ss,\text{rms}} \approx I_{Ls,\text{peak}} \sqrt{\frac{t_{Ss}}{3T_s}} = 2.3 \text{ A}. \tag{36}$$

4) *Snubber capacitor*: In order to calculate the snubber capacitance, $\Delta V_{Cs}$ is selected to be less than 15% of the output voltage ($\alpha = 0.15$, and $\Delta V_{Cs} \leq 60$ V). Then, based on (33) and (35), the snubber capacitor is restricted as $4.6\ n\text{F} \leq C_s \leq 30\ n\text{F}$. To further extend the ZVS turn-OFF range at the light load of the converter, $C_s$ should be selected as small as possible within the range calculated above; therefore, in this paper $C_s = 6.8\ n\text{F}$ is selected. Based on the selected value of the snubber capacitance, the real value of $\Delta V_{Cs}$ can be calculated from (17) by $\Delta V_{Cs} = 49.5$ V.

5) Snubber diodes: According to Fig. 2, the average current of the snubber diode $D_{s1}$ can be calculated approximately as follow:

$$\begin{aligned} I_{Ds1,\text{avg}} &= \frac{1}{T_s}\int_0^{T_s} i_{Ds1}(t)dt \\ &= \frac{1}{T_s}\left(0.5 I_{Ls,\text{peak}}(2t_{Ss} - (t_5 - t_4))\right. \\ &\quad \left. + I_{i,\max}(t_{11} - t_{10})\right) \end{aligned} \tag{37}$$

where ($t_5$–$t_4$) and ($t_{11}$–$t_{10}$) are the durations of *Mode 4* and *Mode 10,* respectively, and these values are calculated from (9) and (21) as $t_5 - t_4 = 197$ ns and $t_{11} - t_{10} = 179$ ns. As a result, the value of $I_{Ds1,\text{avg}} = 1.2$ A is determined from (37). In this paper, the same model is used for three snubber diodes, and according to Fig. 2, $D_{s1}$ has the highest current rating. Therefore, it is not necessary to calculate the current rating for other two snubber diodes.

Finally, based on the calculations mentioned above and simulation results, the current ratings and selected devices for the 2-kW prototype of the proposed converter are listed in Table III.

TABLE III
COMPONENT RATINGS AND SELECTED DEVICES

| Components | | Ratings | Selected devices |
|---|---|---|---|
| Main switch ($S_m$) | | 400V, 10.2A | ON Semiconductor: NTH027N65S3F<br>650V, 60A, $C_{oss(er)}$ = 352pF, $R_{ds,on}$ = 27.4mΩ |
| Main diode ($D$) | | 400V, 4.4A | IXYS: DSEI30-06A<br>600V, 37A, $V_F$ = 1.4V, $t_{rr}$ = 35ns |
| Input inductor ($L$) | | $I_{rms}$ = 13.3A<br>$I_{peak}$ = 14.7A | Changsung's core CH508060<br>$L$ = 350μH |
| Output capacitor ($C$) | | 400V, 6.2A | HEMET: C4AEHBW5300A3JJ<br>600V, 30μF |
| Snubber switch ($S_s$) | | 400V, 2.3A | FAIRCHILD: FCPF067N65S3<br>650V, 28A, $C_{oss(er)}$ = 104pF, $R_{ds,on}$ = 67mΩ |
| Snubber diodes | $D_{s1}$ | 46V, 1.2A | VISHAY: VS-15EVL06-M3 (*Proposed*)<br>600V, $V_F$ = 1.15V, $C_J$ = 17pF |
| | $D_{s2}$ | 400V, 0.6A | VS-HFA16TB120SPbF (*Positions I & II*)<br>1200V, $V_F$ = 2.7V, $C_J$ = 20pF |
| | $D_{s3}$ | 400V, 0.6A | |
| Snubber inductor ($L_s$) | | $I_{rms}$ = 3.4A<br>$I_{peak}$ = 15.2A | WE: 74439370150<br>$I_{Rate}$ = 10A, $I_{SAT}$ = 34A, $L_s$ = 15μH |
| Snubber capacitor ($C_s$) | | 400V , 2.6A | TDK: B32620A6682J189<br>630V, 6.8nF |

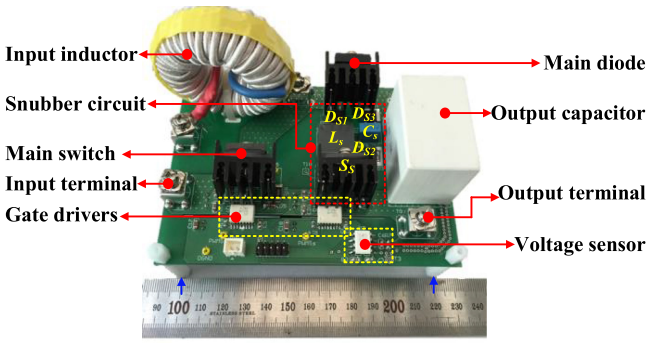


Fig. 11. Photograph of the 2 kW laboratory prototype.

## V. EXPERIMENTAL RESULTS

### A. Experimental Setup

Based on the selected components as shown in Table III, the 2-kW laboratory prototype of the boost converter with the proposed ZVT cell has been built and tested. A Photograph of the 2-kW prototype is shown in Fig. 11, which is implemented using DSP TMS320F28335. The current and voltage waveforms are measured by an oscilloscope YOKOGAWA DLM4058, and a digital power meter YOKOGAWA WT3000 is used to measure the efficiency.

### B. Results and Discussions

The experimental results are obtained from the 2-kW laboratory prototype and shown in Fig. 12. As can be seen from Fig. 12(a), the main switch turns ON with complete ZVS and turns OFF with near ZVS. In Fig. 12(b), ZCS turn-ON of the snubber switch as well as ZCS turn-OFF of the main diode are observed from the snubber inductor current, and ZVS turn-OFF of the snubber switch is seen from the gating signal and drain voltages of the snubber switch. The output and snubber capacitor voltages are shown in Fig. 12(c), in which, $\Delta V_{Cs}$ is measured at 47 V, which corresponds to 11.75% of the output voltage, this value of $\Delta V_{Cs}$ is a little bit different compared to the calculation as shown in the previous section due to existing of the parasitic capacitor in the circuit. The voltages across the snubber diodes are shown in Fig. 12(d), where diode $D_{s1}$ has voltage rating of $\Delta V_{Cs}$, and diodes $D_{s2}$ and $D_{s3}$ have voltage rating of $V_o$. It is seen from Fig. 12 that there is no extra voltage imposed on the main or snubber components, and voltage rating of the

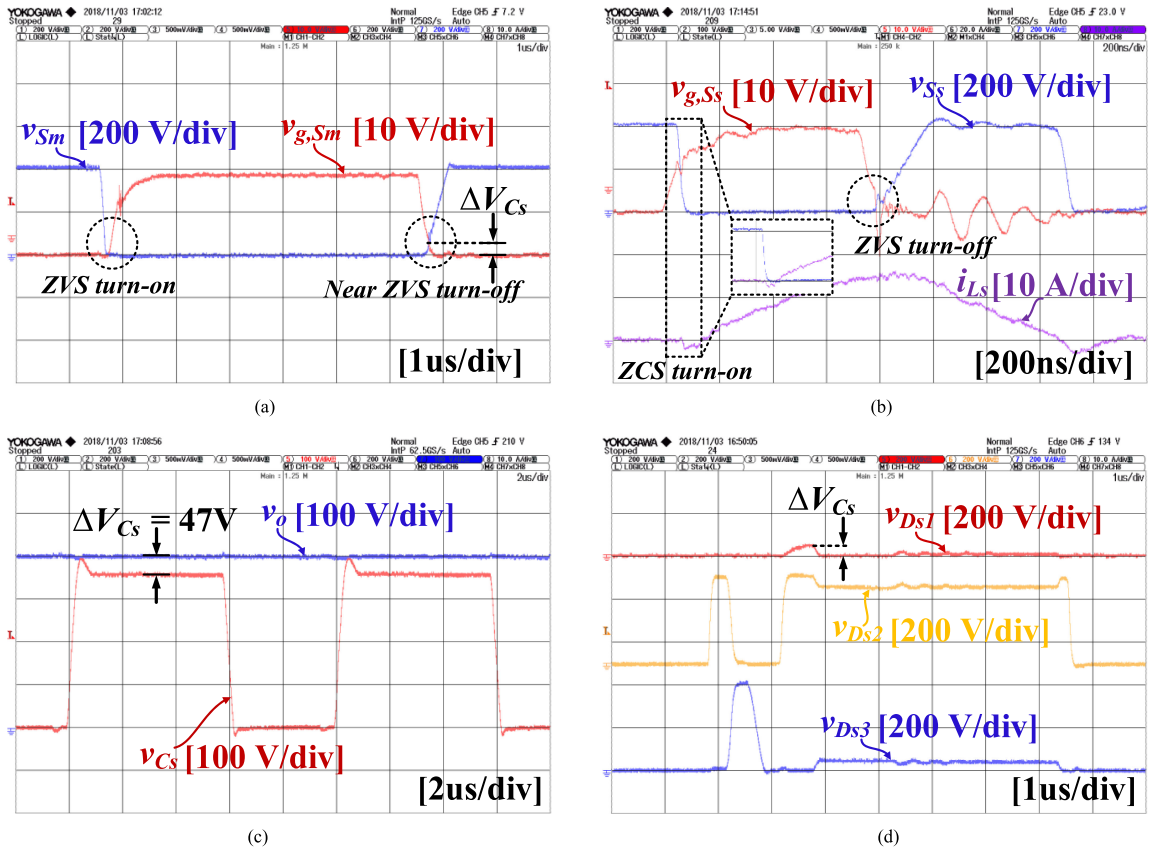


Fig. 12. Experimental results of the boost converter with the proposed ZVT cell. (a) $S_m$. (b) $S_s$ and $L_s$. (c) $v_o$ and $v_{Cs}$. (d) $v_{Ds1}$, $v_{Ds2}$ and $v_{Ds3}$.

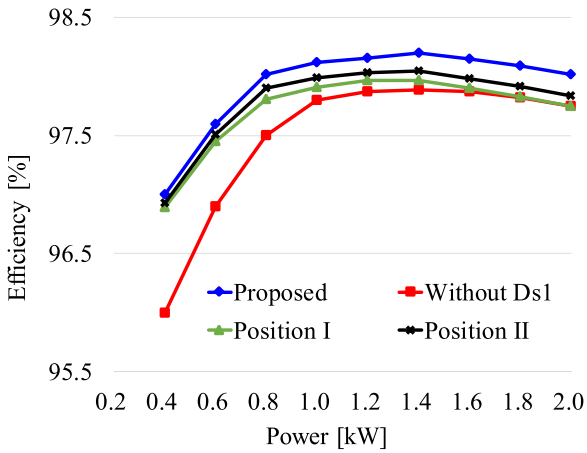


Fig. 13. Measured efficiency of the converter in different cases of the blocking diode.

components is equal to or lower than the output voltage. The experimental results verified the theoretical analysis.

The efficiencies of the converter with three different positions of diode $D_{s1}$ and without diode $D_{s1}$ are measured and compared in Fig. 13. The peak efficiency of the proposed converter is 98.2% at 1.4 kW and the full load efficiency is 98.02%.

In order to implement the ZVT cell in case of *Position I* (*Position II*), diodes $D_{s1}$ and $D_{s2}$ ($D_{s1}$) are replaced by diode VS-HFA16TB120SPbF, which has the voltage rating and the forward voltage drop of 1200 V and 2.7 V, respectively. The voltage waveforms with high-voltage ringing of diodes $D_{s1}$ and $D_{s2}$ in these cases are shown in Fig. 14. As seen in Fig. 14, while the high-voltage ringing is imposed on both diodes $D_{s1}$ and $D_{s2}$ in case of *Position I*, it is imposed only on diode $D_{s1}$ in case of *Position II*. As time goes by, the amplitude of ringing voltages is damped due to the parasitic resistances in the circuit. As shown in Fig. 13, the efficiencies at full load of the converter in cases of *Position I* and *II* are reduced by 0.27% and 0.18%, respectively, compared to the proposed ZVT cell. Moreover, the price of diode VS-HFA16TB120SPbF ($7) is much higher than diode VS-15EVL06-M3 ($1), which is used in the proposed ZVT cell. If the blocking diode $D_{s1}$ is not used, then the efficiency becomes lower due to the circulating current, especially at the light load condition. As seen from Fig. 13, in comparison with other cases of locating diode $D_{s1}$, the proposed converter has the highest efficiency over the whole range of load. At 100 kHz switching frequency, the experimental prototype without using ZVT cell could not operate up to 2 kW due to the excessive heat caused by the switching loss.

The comparison of the proposed converter and some of the well-known ZVT converters is summarized in Table IV. It is noted that the proposed converter resolves almost all problems of the other ZVT converters, which was mentioned in Section II, with the minimum component count.

## VI. Family of the Proposed ZVT Converters

The proposed ZVT cell can be applied to the other family members of NPDC, such as buck, buck–boost, Cúk, and SEPIC converters as shown in Fig. 15. In these converters, the polarities of the current and voltage of all the snubber components are

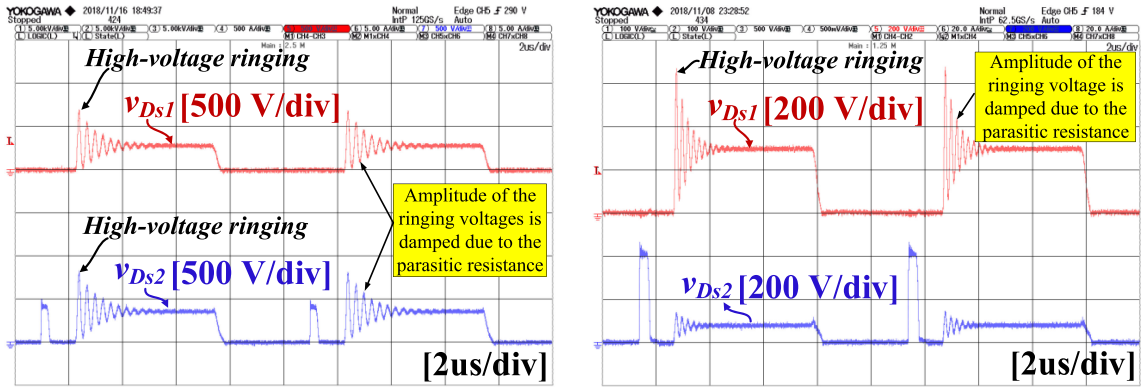


Fig. 14. Experimental waveforms of the high-voltage ringing imposed on $D_{s1}$ and $D_{s2}$. (a) *Position I*. (b) *Position II*.

TABLE IV
COMPARISON BETWEEN THE PROPOSED ZVT CELL AND OTHER COUNTERPARTS

| Features | Proposed | [8] | [12] | [13] | [18] |
|---|---|---|---|---|---|
| Online calculation | No | Yes | No | No | No |
| Voltage rating of $S_s$ | $V_o$ | $V_o$ | $V_o$ | $V_o$ | $V_o + V_{Cs}$ |
| Floating gate driver | No | No | No | Yes | No |
| Number of magnetic components | 1 inductor | 1 transformer | 2 inductors | 1 inductor | 2 inductors |
| Number of capacitors | 1 | 1 | 2 | 2 | 1 |
| Number of diodes | 3 | 3 | 4 | 2 | 3 |

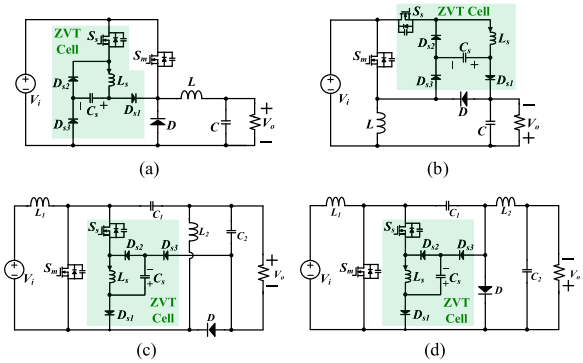


Fig. 15. Basic dc–dc converters with the proposed ZVT cell. (a) Buck. (b) Buck–Boost. (c) SEPIC. (d) Cúk.

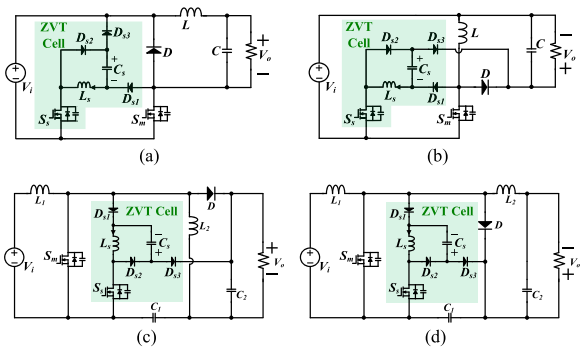


Fig. 16. Basic dc–dc converters with the proposed common-source switches ZVT cell. (a) Buck. (b) Buck–Boost. (c) SEPIC. (d) Cúk.

reversed compared to the boost type, but the related operation principles, design procedures, and soft-switching characteristics are preserved. However, the main and the snubber switches require the floating gate driver. Avoiding the floating gate driver leads to reducing circuit complexity and cost; therefore, these converters are modified with the common-source switches as shown in Fig. 16.

## VII. CONCLUSION

This paper proposed a new ZVT cell for NPDC. The features of the proposed ZVT cell are as follows.

1) Providing ZVS turn-ON/near ZVS turn-OFF for the main switch and ZCS turn-OFF for the main diode.
2) The snubber switch turns ON with ZCS and turns OFF with ZVS. All snubber diodes have low-voltage ringing and are turned OFF under soft-switching condition.
3) No extra voltage and current stresses are imposed on the main or snubber components.
4) No floating gate driver is required for the main and snubber switches.
5) It can be applied to all of the basic non-isolated dc–dc converters.

From the comparative analysis of three different positions of the blocking diode, it is concluded that the proposed ZVT cell has the lowest voltage ringing of the snubber diodes. This positioning analysis can be generalized for all of the ZVT cells

using the blocking diode. Operation principles and designed procedures of the boost converter with the proposed ZVT cell are presented and verified by the 2-kW laboratory prototype operating at 100 kHz. The maximum and full load efficiency are measured at 98.2% and 98.02%, respectively. Finally, the integration of the proposed ZVT cell into other family members of NPDC and their variants are introduced.

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