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A 10-bit 30-MS/s successive approximation register analog-to-digital converter for low-power sub-sampling applications

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ABSTRACT

A 10-bit 30-MS/s successive approximation register analog-to-digital converter (ADC), which is suitable for low-power sub-sampling applications, is presented. Bootstrapped switches are used to enhance the sampling linearity at the high input frequency. The proposed ADC adopts a binary-weighted split-capacitor array with the energy efficient switching procedure and includes an asynchronous clock scheme to yield more power and speed-efficiency. The ADC is fabricated in a 65 nm complementary metal-oxide-semiconductor technology and occupies an active area of 0.07 mm^2. The differential and integral nonlinearities of the ADC are less than 0.82 and 1.13 LSB, respectively. The ADC shows a signal-to-noise-distortion ratio of 56.60 dB, a spurious free dynamic range of 73.35 dB, and an effective number of bits (ENOB) of 9.11-bits with a 2.5-MHz sinusoidal input at 30-MS/s. It exhibits higher than 8.86 ENOB for input frequencies up to 78-MHz. The ADC consumes 0.85 mW at a 1.1 V supply and achieves a figure-of-merit of 51 fJ/conversion-step.

1. Introduction

Analog-to-digital converters (ADCs) used for sub-sampling applications such as the digital video broadcasting over terrestrial and handheld systems have become popular because they not only perform analog-to-digital conversion but also reduce the number of down-conversion stages in the receiver signal chain [1–6]. Such sub-sampling ADCs, which can translate the input bandwidth to an intermediate or baseband frequency, operate at several tens of MS/s with a high effective resolution bandwidth (ERBW) typically between 30 and 70-MHz and have a 10-bit resolution. Thus, the input sampling network should be carefully designed to adopt in these ADCs.

Recently, successive approximation register (SAR) ADCs have proven to be very efficient for meeting the above requirements of conversion rate and resolution with low-power consumption and small area [7–12]. Meanwhile, the input capacitances in SAR ADCs based on a capacitive digital-to-analog converter (DAC) [8,11] increase exponentially with the number of bits. To drive such large capacitance load, the proceeding stages, such as variable gain amplifiers or filters, need to provide high driving capability. Furthermore, large capacitances consume excessive area and more power with longer settling times. Therefore, considerable efforts have to take place in reducing the complexity and the area of the DAC without sacrificing robustness.

In this paper, we present a low-power and small-area 10-bit 30-MS/s SAR ADC with wide input frequency range in a 65 nm CMOS. The ADC adopts a bootstrapped n-type metal-oxide-semiconductor (nMOS) switch to enhance the sampling linearity. In order to reduce the input capacitance of the DAC, binary-weighted split-capacitor arrays (BSA) with a merged-capacitor switching (MCS) technique is used. The ADC also includes an asynchronous clock scheme for a suitable conversion rate. This paper is organized as follows. Section 2 introduces the proposed ADC architecture, Section 3 describes the circuit implementation, Section 4 shows measurement results, and Section 5 includes the conclusion.

2. Architecture of the proposed SAR ADC

The block diagram of the proposed SAR ADC operating at a 1.1 V supply is described in Fig. 1. The main blocks of the SAR ADC comprise of a DAC with bootstrapped switches, a regenerative comparator, an asynchronous clock, an SAR logic, two thermometer decoders, an error correction logic (ECL), and a bias circuit. Bootstrapped nMOS switches are located in front of the DAC and directly connected to the input signal. The control signal of the switches is boosted to achieve a constant on-resistance at a 1.1 V supply voltage and minimizes the signal distortion. The split-capacitor array with the MCS technique is used to sample the input signal and serves as a DAC for creating and subtracting reference voltages. The DAC includes switch drivers, which

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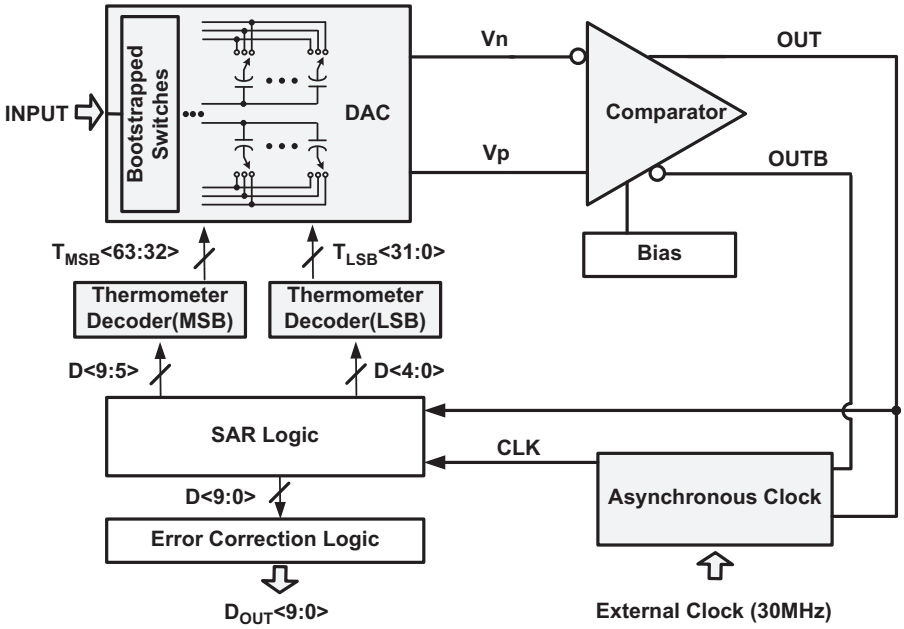

Fig. 1. Block diagram of the proposed SAR ADC.

control the DAC operation by performing the unary-scaled feedback during the successive approximation. In addition, the thermometer decoders are incorporated in the ADC, which translate the binary output of the SAR logic to thermometer codes and address the local decoders inside the DAC. This block can decrease the power consumption and the switching noise of the DAC because fewer capacitors are needed to be charged depending on the value of the input sample. The comparator is composed of a preamplifier and a regenerative latch. To improve the operation speed of the proposed converter, the asynchronous clock scheme is employed. The SAR logic consists of a shift register and a set of switch drive registers [13]. The error correction technique is adopted to prevent the effects of dynamic noise sources such as reference or signal glitches and supply variation [9]. The entire conversion is divided into three parts. The first phase is for input sampling assigned to 25% of the whole period. Data conversion is then performed during the next phase, and error correction follows as the last phase.

3. ADC circuit implementation

3.1. Bootstrapped switch

To reduce the distortion of a single switch by keeping the gate–source voltage nearly constant, gate bootstrapped switches are used as the input sampling switches. The performance of the ADC at a relatively high frequency input signal is largely dependent on these switches. Fig. 2 shows the schematic of the switches with their associated circuits. A single capacitor C_b is used to bootstrap the sampling clock signal. The switch circuits should be designed such that the gate oxide is not subject to voltages exceeding the supply voltage difference. This requires protection circuits by including additional transistors [14]. Instead of employing protection circuits, we simply use I/O transistors denoted as DN1, DN2, DP1, DP2, and DP3, which are exposed to the high potential from the charge pump.

The bootstrapped switch circuit is operated as follows. Initially the clock signal (Q1) is low, then transistors MN1 and MP1 will be turned off. Transistor MN2 will be turned on and the bottom plate

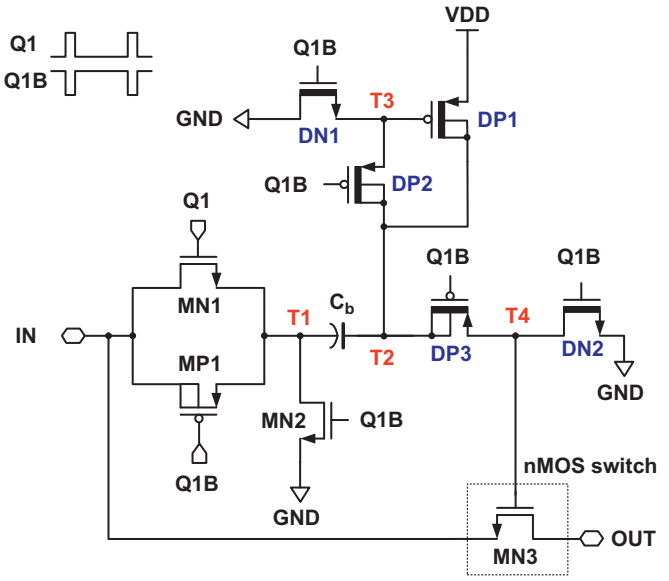

Fig. 2. Schematic of the bootstrapped switch.

of C_b (node T1) will be at GND. At the same time, DN1 will be turned on making the gate of DP1 (node T3) low. This connects node T2 to VDD. As a result of this operation, the capacitor C_b will be charged to VDD-GND. The gate of the nMOS switch MN3 (node T4) is at GND because DN2 is switched on. When Q1 becomes high, then DP2 will be switched on making DP1 to act as an MOS diode. DP3 will be switched on and the voltage at node T4 becomes high. The input signal is now applied at node T1 and the stored voltage on the capacitor C_b will increase furthermore the node voltage T2 and via DP3 node voltage T4.

As a result, the switching voltage of MN3 is added to the input signal level and with the full voltage on C_b a low impedance of the switch is obtained. This then keeps the gate-to-source voltage of MN3 constant with varying input signal, ensuring that the bootstrapped switch's on-resistance is virtually constant. Under the high frequency input condition, the nonlinear distortion of the

switch on-resistance is prominently decreased, and the dynamic performance of high frequency is improved, resulting in the sub-sampling design.

3.2. Switched-capacitor DAC with an energy efficient switching

The DAC using the BSA with a MCS (BSA-MCS) technique is shown in Fig. 3. The BSA-MCS technique merges two unit capacitors into one both in the MSB and LSB sides, and the number of unit capacitors required in proposed split-capacitor arrays is reduced by about 95% compared to that in [8]. The split-capacitor array consists of 32 unit capacitors and a coupling capacitor (C_c), which reduces the required number of unit capacitors. The top plates of the capacitor arrays are connected to the comparator inputs and the bottom plates are switched between two reference voltages. The function of the DAC employing the BSA-MCS is identical to that of the previous one [9]. The only difference is that the input common mode voltage (CM) is not needed in the proposed DAC, equivalent to when two different references are applied to two unit capacitors. Instead of implementing CM, the capacitor bottom plate charge sharing technique is implemented through nMOS switches [10]. Connecting the bottom plates of the two differential capacitor arrays to each other, the bottom plate voltage of the capacitor arrays becomes averaging and realizes CM. The switch drivers, which control the DAC operation, are addressed by two 5-bit thermometer decoders. Each unit capacitance ($C_{1n,p}\sim C_{32n,p}$) is 63 fF, the coupling capacitance is 47 fF, and the total sampling capacitance of the DAC is 1 pF. Post-layout simulation with parasitic extraction was performed to compensate the gain error of the coupling capacitor. The external voltage sources of 0.85 V and 0.35 V are used as the positive and negative reference voltages for the ADC, respectively.

The detailed operations of the DAC are carried out as follows. Although capacitor arrays in the DAC are differentially operated, the switching operation of the DAC is described for the positive capacitor array for simplicity. At a sampling phase, the input voltage (IN) is sampled only on the MSB side to maintain the sampling value. The LSB side is grounded through nMOS switches. After the sampling phase, the bottom plate of all capacitors is switched to the negative reference voltage (REFN). Next, 8-capacitors of the MSB side are switched to the positive reference voltage (REFP) and the comparator performs the first comparison. If IN is higher than $1/2V_{REF}$, the MSB code D9 is decided to 1. V_{REF} is the difference of REFP and REFN. Otherwise, D9 is decided to 0 and the MSB code triggers the SAR logic to control reference switching of the DAC by the binary search algorithm [13,15]. Then, 4-capacitors are switched to REFN and the comparator does the comparison again. The ADC repeats this sequence until the LSB is decided.

The binary search algorithm of the conventional DAC is efficient when all the output settings are correct, as in the "up" transition. However, the switching method wastes considerable energy when the output settings are incorrect, as in the "down" transition. In other words, the sequences that 8-capacitors are reconnected to REFN, and then other 4-capacitors are set to REFP when D9 is 0 are not energy efficient because unnecessary capacitor switching is performed. To reduce the switching energy in the down transition, the half capacitors only have to be reconnected to REFN. Then, the gratuitous switching of the capacitor array can be eliminated. The switching sequence of the proposed capacitor array is compared with the conventional one in Fig. 4.

These switching procedures are easily implemented by the thermometer decoders. Although the thermometer decoders increases the complexity of the digital circuit design and propagation delay of the ADC, the proposed conversion scheme with the BSA-MCS technique is more energy efficient than that of previous one [16,17]. In addition, the thermometer decoders can decrease switching noise of the DAC because fewer capacitors are needed to be charged depending on the value of the input sample.

For a 10-bit case, the behavioral simulation results of average switching energy for different schemes are shown in Fig. 5. The conventional switching procedure consumes $1365.3CV^2_{REF}$, the split-capacitor scheme [16] consumes $852.3CV^2_{REF}$, the set-and-down scheme [7] consumes $255.5CV^2_{REF}$, while the proposed switching procedure consumes only $26.6CV^2_{REF}$. Because the number of the unit capacitors in the capacitor array using the BSA-MCS technique is only 1/32 of that of the split-capacitor scheme, the proposed switching sequence requires 95% less switching energy than that of the split-capacitor scheme. Thus the proposed DAC using BSA-MCS technique has the advantage of power consumption and the relaxation of matching requirement for the capacitor array.

3.3. Asynchronous clock

An asynchronous clock, which is implemented to avoid the need for the high-speed clock, supplies clock signals to the SAR logic and the comparator. Fig. 6(a) shows the block and timing diagram of the proposed asynchronous clock, which consists of a NOR gate, 2-bit variable delay, and latch clock (L_{EN}) generator. Due to the variable delay cell, which optimizes the pre-amplifying time, this clock scheme improves the power and speed-efficiency compared to that of the asynchronous design [13].

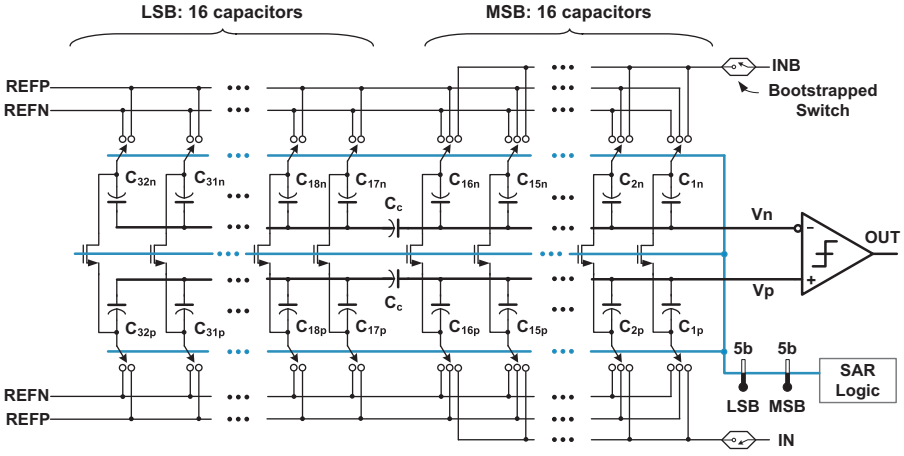

Fig. 3. Proposed 10-bit DAC using the binary-weighted split-capacitor arrays with a merged-capacitor switching technique.

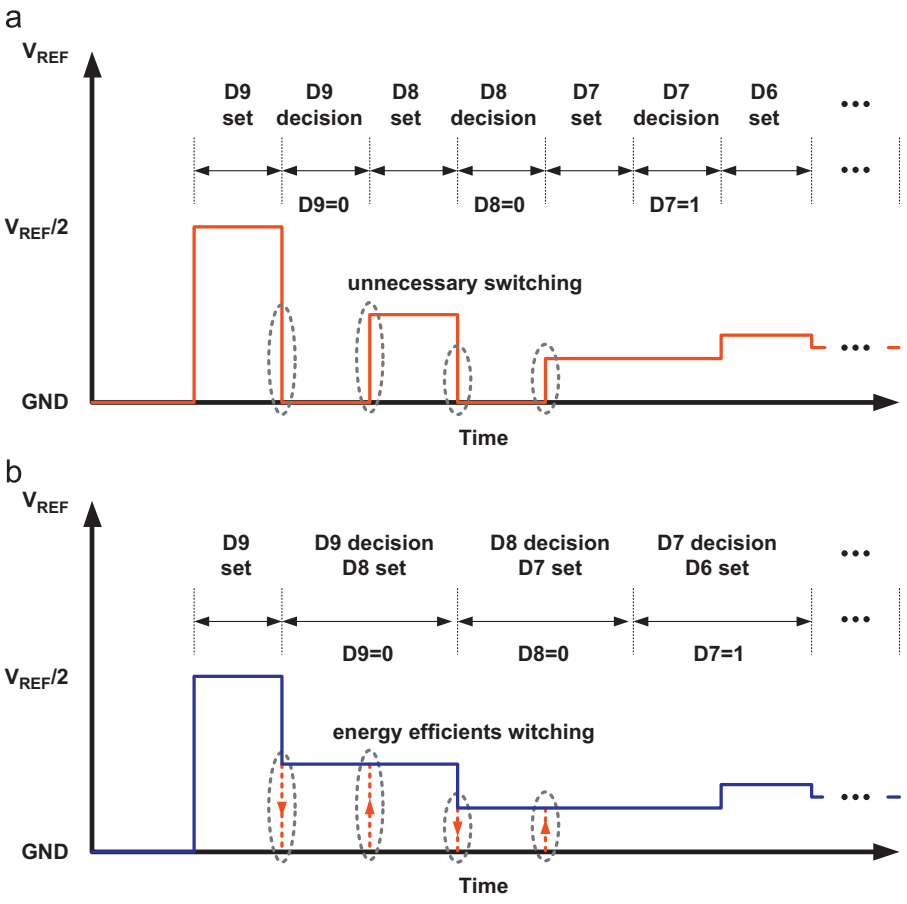

Fig. 4. Comparisons of the switching sequence of the DAC. (a) Conventional switching procedure. (b) Proposed switching procedure.

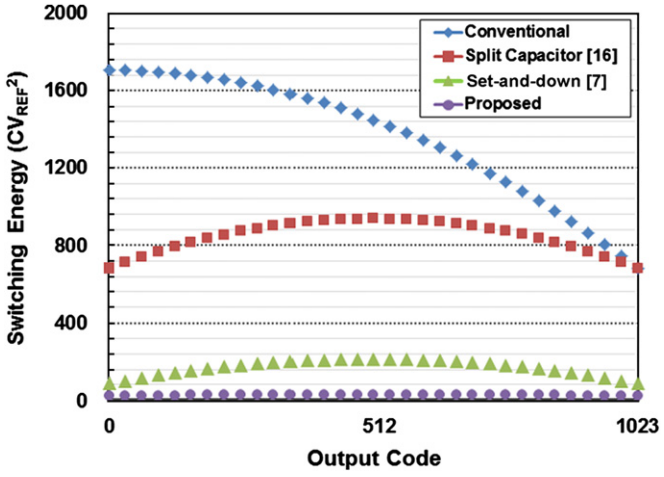

Fig. 5. Switching energy versus output code.

Initially, the preamplifier resets at the falling edge of an initial clock (INI), which is the start of the SAR operation (OPR). During the bit cycling, the clock period is divided into three phase for the settling of the DAC (P_{RS}), i.e., reset of the preamplifier, pre-amplifying of the DAC output, and regeneration of the latch. Using the reset phase prior to the pre-amplification, the comparator, does not amplify the crossed input signal from the DAC, which helps in reducing the comparator recovery time.

In Fig. 6(c), the details of the proposed asynchronous clock operation are described. With the falling clock edge of DO, L_{EN} is set to high, which triggers the latch and has the effect that one of the output signals CO or COB changes to high, depending on the input voltages of V_n and V_p. When the high signal is detected by the NOR gate, L_{EN} is reset to low, the bits for the DAC are set and a new successive approximation is started. After the settling of the DAC, P_{RS} is set to low, which triggers the preamplifier. The variable delay cell controls the duration of the pre-amplification. The next falling clock edge of DO begins this procedure anew. Finally, the SAR operation is terminated with the last falling edge of CLK.

The dynamic comparator is used that is composed of a preamplifier [13], a regenerative latch [18], and dynamic gate bias circuit as shown in Fig. 7. The resolution of the comparator is limited by the combination of the input offset and the AC noise. To enhance the signal-to-noise ratio of the comparator, the input transistor of the preamplifier is designed with a large size to lower the thermal noise at all frequencies and the flicker noise at low frequencies. The width and length of the input transistors M1 and M2 in Fig. 7 are 60 μm and 0.5 μm, respectively. In this condition, the preamplifier circuit has a gain of 13.8 dB and a −3 dB bandwidth of 350-MHz. The input signal of the comparator can be amplified to about 80% of the settling value. To reduce power consumption of the preamplifier during the idle time, a dynamic gate bias circuit is adopted for controlling the bias current on the preamplifier. The proposed scheme improves the dynamic power consumption of the ADC by 6% at a nominal operating condition.

4. Experimental results and discussion

The proposed ADC is implemented in a 65 nm 1P6M CMOS process with metal-oxide–metal capacitors. Fig. 8 shows the die photograph of the chip. The active area of the ADC occupies

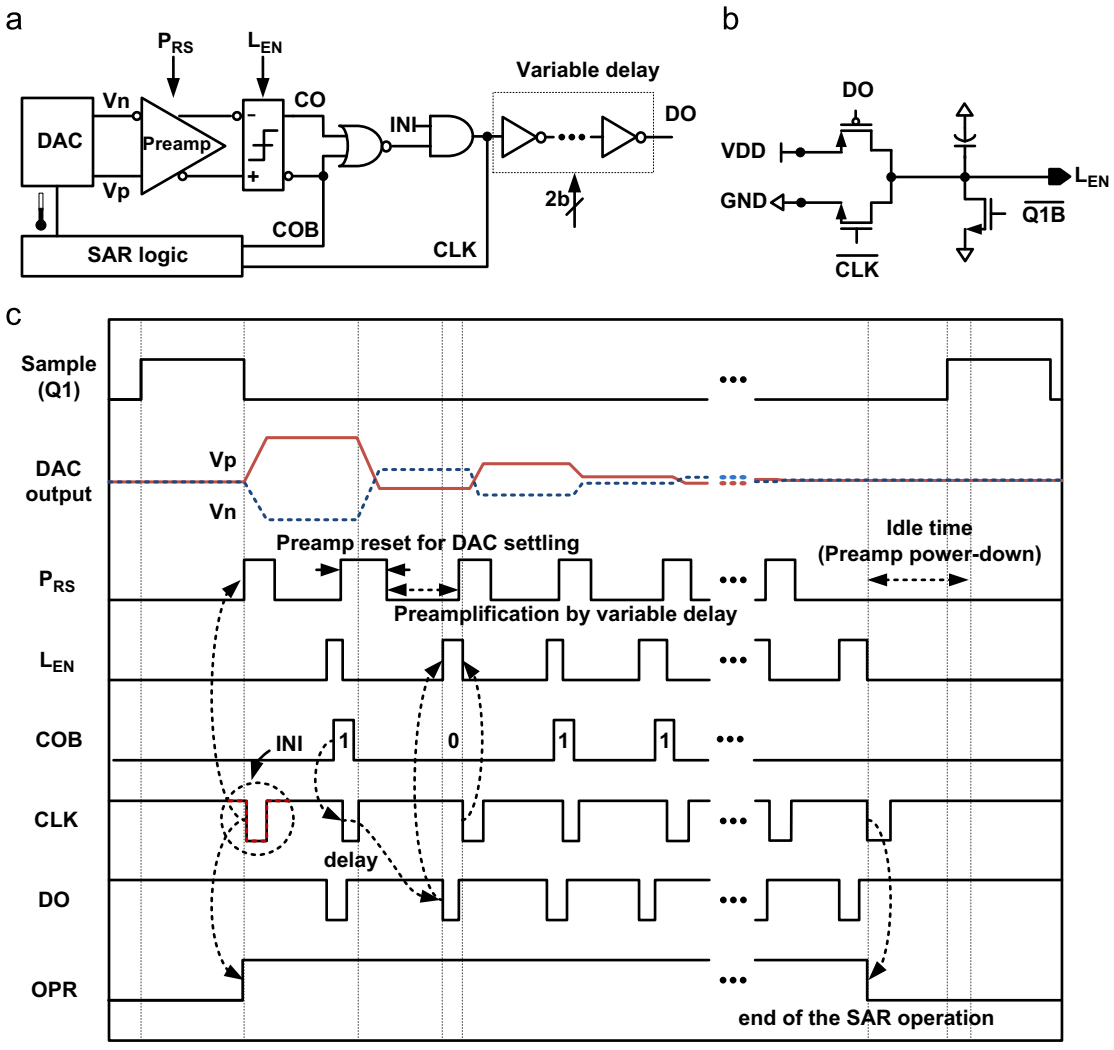

Fig. 6. An asynchronous clock. (a) Block diagram. (b) Latch clock generator. (c) Timing diagram.

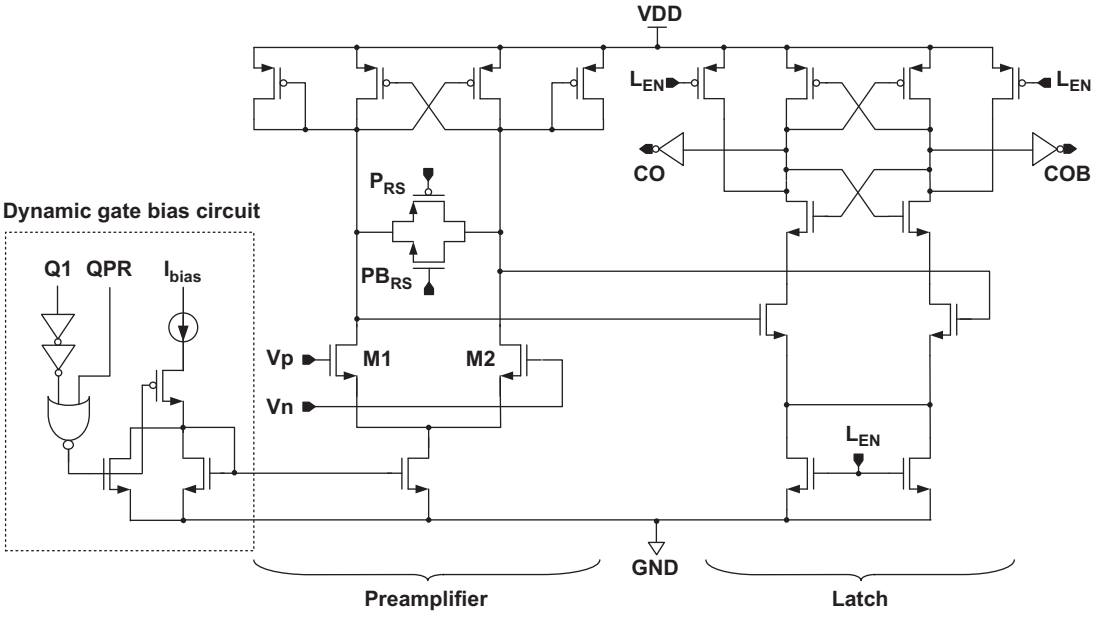

Fig. 7. Comparator with the dynamic gate bias circuit.

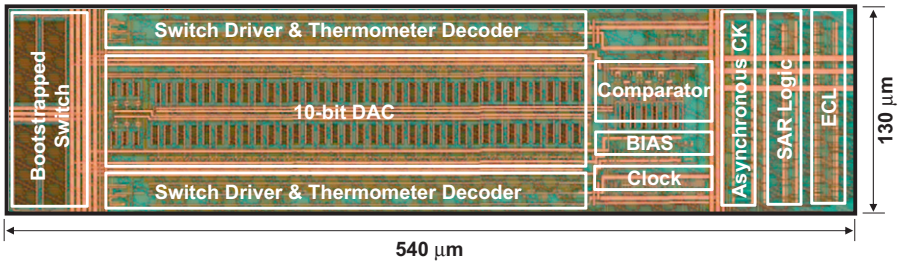

Fig. 8. Die photograph of the prototype ADC.

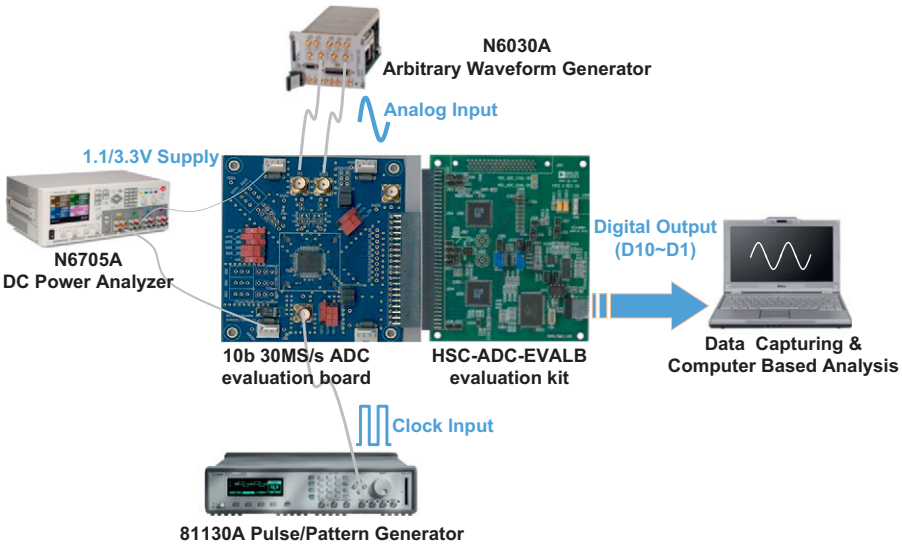

Fig. 9. Diagram of the measurement setup.

0.07 mm^2 (0.54 mm × 0.13 mm). The DAC block with the thermometer decoder occupies 70% of the total area, and the bootstrapped switch and the digital logics occupy 10% and 8%, respectively. The remaining 12% is for the comparator, asynchronous clock, and bias.

The measurement setup is illustrated in Fig. 9. The chip is packaged in a 64-pin quad flat package and mounted on a printed circuit board. The supply voltage is provided by Agilent N6705A DC power analyzer. Reference voltages are generated on the board. A differential input signal is generated by Agilent N6030A arbitrary waveform generator with 15 bit resolution. The clock signal is provided by Agilent 81130 A pulse/pattern generator. The digital outputs of the proposed ADC are captured by Analog Device HSC-ADC-EVALB evaluation board and analyzed using Matlab to extract differential nonlinearity (DNL) and integral nonlinearity (INL) of the converter.

At 30-MS/s, the ADC consumes 0.85 mW from a 1.1 V supply. The analog blocks and the digital blocks use about 45% and 55% of the power, respectively. The segmented area and power is represented in Fig. 10. Fig. 11 shows the DNL and INL of the ADC at a 10-bit accuracy. The peak DNL and INL are −0.71/0.82 LSB and −0.92/1.13 LSB, respectively. The measured Fast Fourier transform spectra for input frequencies of 2.5-MHz and 78-MHz at the 30-MS/s are shown in Fig. 12. At 2.5-MHz input frequency, the spurious-free dynamic range (SFDR) is 73.35 dB, and the signal-to-noise-distortion ratio (SNDR) is 56.60 dB. At an input frequency of 78-MHz, the ADC achieves an SFDR and an SNDR of 70.67/55.11 dB, and an effective number of bits (ENOB) of 8.86-bits. The overall dynamic performance versus input frequency at 30-MS/s is summarized in Fig. 13. It exhibits higher

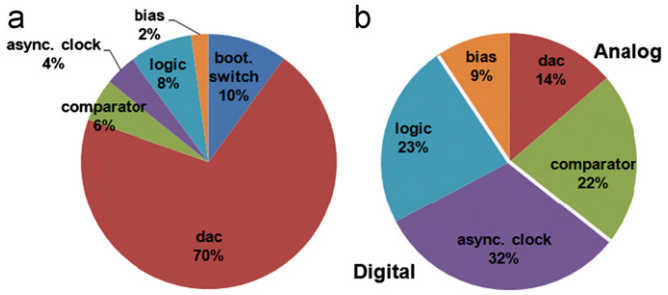

Fig. 10. Segmented area and power. (a) Area. (b) Power.

than 9.02 ENOB for input frequencies up to twice the Nyquist rate (30-MHz) and 8.86 ENOB for 78-MHz input. The dynamic performance is not degraded as the signal frequency is increased up to 5 times the Nyquist input bandwidth.

Fig. 14 shows the measured performance versus the sampling frequency with a 2.5-MHz sinusoidal input. When the sampling rate was 35-MS/s the ENOB was still close to 9 bits. Further increasing the sampling rate rapidly degraded the performance because the conversion time was insufficient.

A well-known figure-of-merit (FOM) is used to evaluate the overall performance of the ADC, which is given as

$$FOM = \frac{P_w}{2^{ENOB}\min\{2ERBW, f_s\}} \quad (1)$$

where P_w and f_s are the power consumption and sampling frequency of the ADC, respectively. The FOM of the ADC is

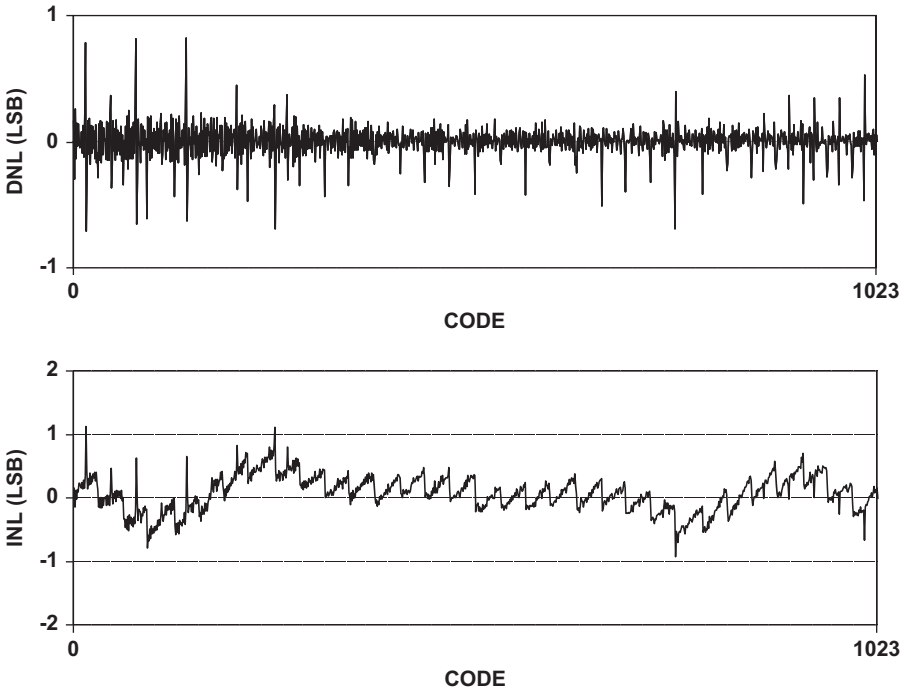

Fig. 11. Measured DNL and INL.

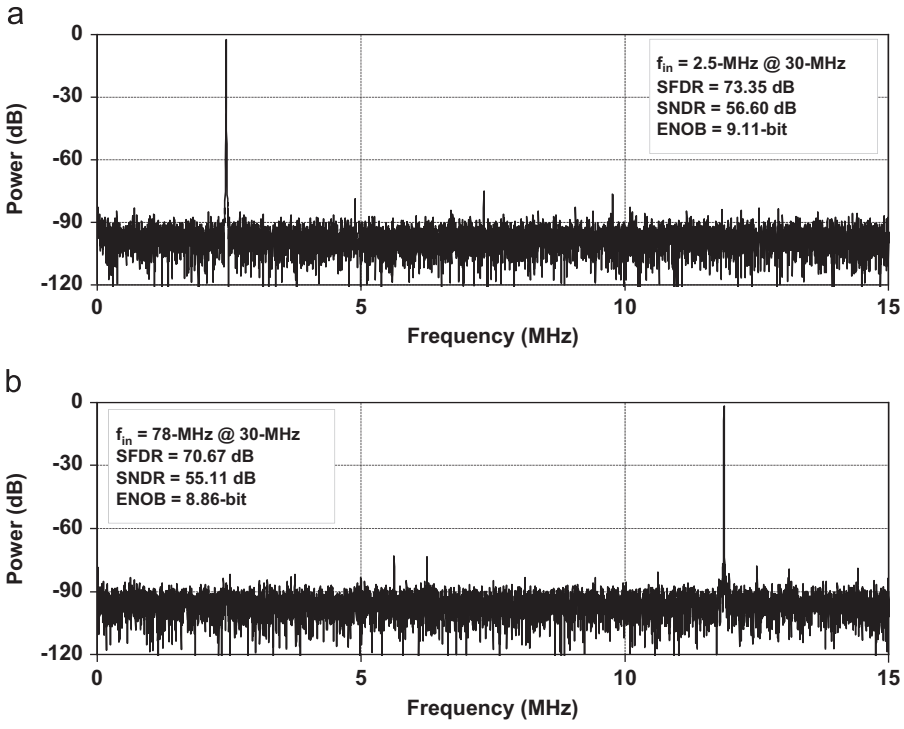

Fig. 12. Measured FFT plots. (a) f_{in}=2.5-MHz at f_s=30-MS/s. (b) f_{in}=78-MHz at f_s=30-MS/s.

51 fJ/conversion-step at 30-MS/s. The measured performance summary and comparison are given in Table 1.

5. Conclusion

A 10-bit 30-MS/s SAR ADC has been presented. The ADC adopts a binary-weighted split-capacitor array with an energy efficient switching procedure and an asynchronous clock scheme. The proposed techniques can effectively improve speed, power consumption, and chip area of the SAR ADC. The ADC also includes a bootstrapped switch for sub-sampling. The prototype ADC with 78-MHz input at 30-MS/s achieves 8.86 ENOB and SFDR of 70.67 dB at a 1.1 V supply voltage and dissipates 0.85 mW. Experimental results have demonstrated that the proposed ADC circuit is suitable for low-power sub-sampling applications.

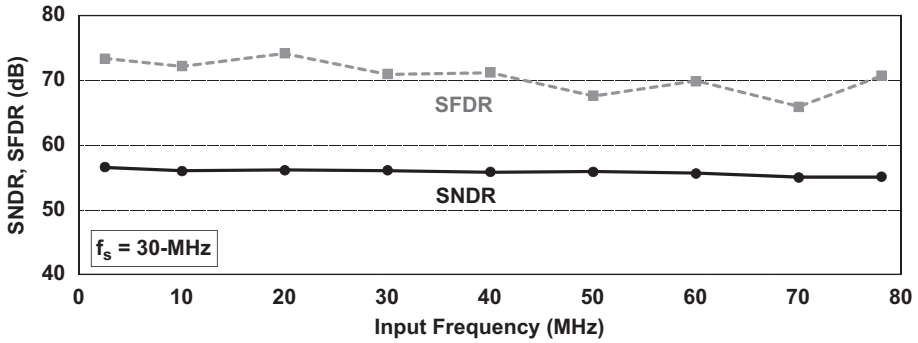

Fig. 13. Dynamic performances versus input frequency.

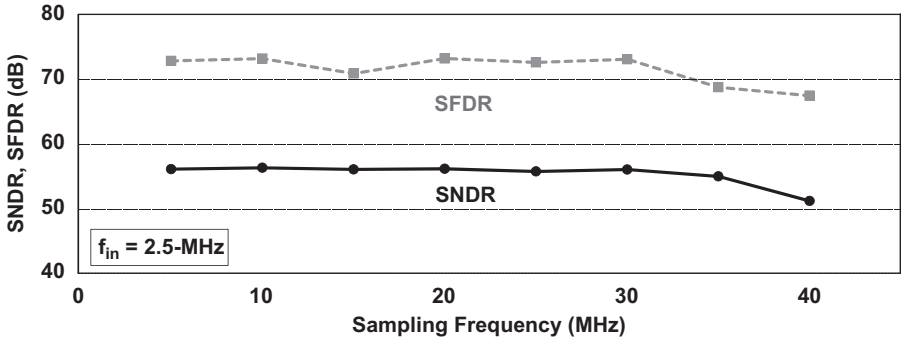

Fig. 14. Measured performances versus sampling frequency.

Table 1
Performance summary and comparisons.

Parameters	[3]	[7]	[10]	[19]	This work
Process (nm)	180	130	65	130	65
Resolution (bit)	10	10	9	10	10
Supply voltage (V)	1.8	1.2	1.2	1.2	1.1
Sample rate (MS/s)	30	50	100	40	30
ERBW (MHz)	70	50	50	20	78
DNL (LSB)	±0.57	±1.00	±0.30	±0.78	±0.82
INL (LSB)	±0.80	±2.20	±0.40	±1.55	±1.13
SFDR (dB)	65.93	67.7	65.2	57.7	73.35
SNDR (dB)	57.41	52.8	51.0	50.6	56.6
ENOB (bit)	9.24	8.48	8.17	8.4	9.11
Power (mW)	21.6	0.92	1.46	0.55	0.85
Area (mm^2)	0.7	0.075	0.012	0.32	0.07
FOM (fJ/conv-step)	1187	52	39	42	51

Acknowledgments

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