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A 12-bit 200-MS/s pipelined A/D converter with sampling skew reduction technique

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ABSTRACT

This paper presents a 12-bit 200-MS/s dual channel pipeline analog-to-digital converter (ADC). The ADC is featured with a digital timing correction for reducing a sampling skew and the capacitor swapping for suppressing nonlinearities at the first stage in the pipelined ADC. The prototype ADC occupies $0.8 \times 1.4\ mm^2$ in a 65-nm CMOS technology. The differential nonlinearity is less than 1.0 least significant bit with a 200 MHz sampling frequency. With a sampling frequency of a 200-MS/s and an input of a 2.4 MHz, the ADC, respectively, achieves a signal to noise-and-distortion ratio and a spurious-free dynamic range of 61.49 dB–70.71 dB while consuming of 112 mW at a supply voltage of 1.1 V.

1. Introduction

Recently, demands of high-speed and high-accuracy analog-to-digital converters (ADCs) for HDTV and WLAN applications are dramatically increased. In these applications, the ADC is required to be low-power and small-size at several hundreds of MS/s with 12-bit resolution [1]. Among various ADC architectures, pipelined ADCs are efficient for satisfying the requirement due to high speed that is compatible to a parallel or flash architecture. Moreover, the implementation area and power dissipation can be significantly reduced [2–4].

In conventional pipelined ADCs, to drive same input signal to multiplying digital-to-analog converter (MDAC) and the sub-ADC, a front-end sample-and-hold amplifier (SHA) is used before the first pipelined stage [2–4]. Moreover, to mitigate the sampling skew caused by eliminating the SHA, approaching a careful layout method [5] and employing delayed clock scheme [6] have been suggested. However, the former scheme could be easily affected by PVT variations, resulting unexpected mismatch between two paths, and the latter shows inferior performance at the high-speed applications due to the technical difficulty of providing fixed clock delay time.

The capacitor mismatch of the first MDAC significantly affects to a nonlinearity of each sub-channel ADC. Moreover, the sub-channel's nonlinearity between two channels hardly becomes same value, and it causes output spurious tones [7]. In particular, in the applications of high definition video process, a low differential nonlinearity (DNL) is strongly required rather than achieving a low integral nonlinearity (INL), due to people's recognition nature.

In this paper, a pipelined ADC is proposed with a sampling skew correction and a modified capacitor swapping technique. With adoption of both techniques, the proposed ADC has efficiently-maintained dynamic performance and improved nonlinearity. The paper is organized as follows: Section 2 presents the proposed ADC architecture, Section 3 introduces the proposed sampling correction technique, Section 4 explains the capacitor swapping technique, Section 5 shows measurement results, and Section 6 is the conclusion.

2. Proposed ADC topology

Fig. 1(a) shows the proposed ADC, which adopts a time-interleaved architecture. For high speed and high resolution performance, two pipelined ADCs (PADCs) are used in the sub-channels, CH-1 and CH-2 as shown in Fig. 1(a), respectively. To support a time-interleaving operation, a master clock generator transfers fundamental and its phase-inverted signal (V_{CK1} and V_{CK2}) to CH-1 and CH-2. A back-end multiplexer is operated with alternative treating each dual channel digital code ($D_{OUT\text{-}CH1}$ and $D_{OUT\text{-}CH2}$) and converts them to a single output stream (D_{OUT}) as shown in Fig. 1(b).

Fig. 1(c) shows a block diagram of the sub-channel PADC CH-1. The PADC has 6 pipelined stages based on effective 2.5-bit/stage without the front-end SHA block to satisfy both low power consumption and small-die area. However, removing the SHA

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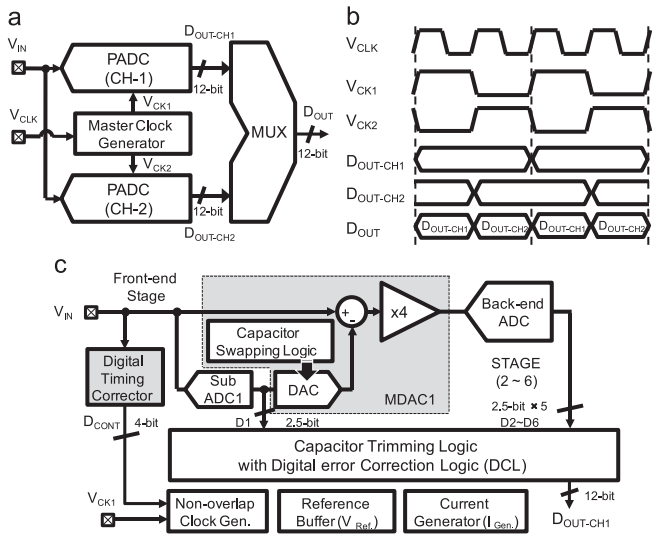

Fig. 1. Block diagrams: (a) proposed ADC architecture, (b) timing diagram, and (c) sub-channel CH-1.

Table 1
Digital output extraction with an 1-bit redundant error correction.

Stage	Digital Output												
Stage1	D1[3]	D1[2]	D1[1]										
Stage2			D2[3]	D2[2]	D2[1]								
Stage3					D3[3]	D3[2]	D3[1]						
Stage4							D4[3]	D4[2]	D4[1]				
Stage5									D5[3]	D5[2]	D5[1]		
Stage6											D6[3]	D6[2]	D6[1]
D_{OUT}	[12]	[11]	[10]	[09]	[08]	[07]	[06]	[05]	[04]	[03]	[02]	[01]	None Used

causes to occurrence of a sampling skew between the sub-ADC and MDAC1. In the proposed ADC, to prevent the sampling skew generation, 4-bit timing codes (D_{CONT}) are used. The timing codes control a digital timing corrector in Fig. 1(c) for providing compensated delay to the non-overlap clock generator. An amplifier sharing is adopted at the back-end stages [8]. The further detailed discussion will be taken in Sections 3 and 4.

At the front-end stage, to improve signal nonlinearities from capacitor mismatches at the multiplying digital-to-analog converter (MDAC), a periodic swapping of feedback capacitor is used, whereas the periodic swapping occurs to undesired offset from capacitor mismatch. To solve this, capacitor trimming scheme is suggested to compensate the offset at the first MDAC.

Each stage digital output is transferred to the digital error correction logic (DCL). As shown in Table 1, nonlinear errors from inter-stage residue amplifier and comparators offsets are corrected by overlapped 5-bit codes at the DCL, thus the raw 18-bit inputs are finally revised corrected 12-bit output with a non-used bit. In other worlds, the ADC adopted the DCL has offset budget less than 0.5 LSB of the resolution of the remaining stages.

A low-power implementation in the ADC design is an important issue in the deep submicron CMOS process, which uses a low-supply voltage. The high linearity and insensitive supply current should be assured in the low-supply since the threshold voltage of the transistor is still high even in low-supply and cascode circuits are hardly utilized. Therefore, optimized circuit design according to low-power consumption should be pursued in the sub-circuit design.

Bootstrap switches in the MDAC1 are used for ensuring a high linearity, which dominantly affects on the ADC dynamic range with a high speed input signal. Fig. 2(a) is the switch schematic with a bootstrap clock generator, which consists of the

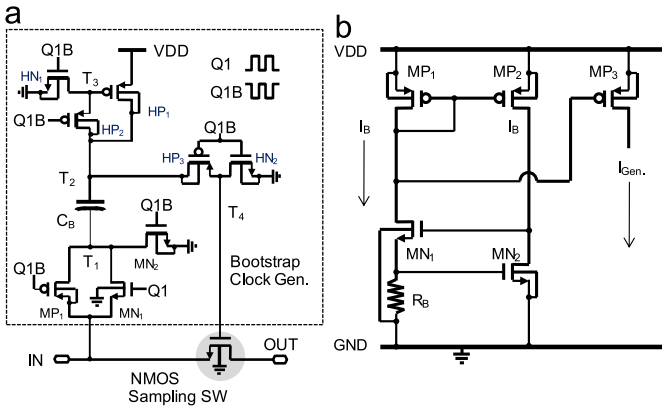

Fig. 2. Schematics of (a) bootstrap switch and (b) self-biased V_{TH} current source.

bootstrapping sampling capacitor C_B, normal switches (MN_{1-2} and MP_1), and high voltage switches (HN_{1-2} and HP_{1-3}). To mitigate the stress of the gate-oxide with above allowable voltage limits for a long-term reliability, high voltage transistors are used. As shown in Fig. 2(a), C_B is periodically charged up by clocking signal (Q1 and Q1B). In the steady-state, the charge of C_B is kept on the VDD. To turn on a sampling switch at high Q1, C_B is connected between the input (IN) and the transistor gate of the sampling switch. Since parasitic capacitors from the sampling switch leads to C_B charge loss, the gate voltage of the sampling switch does not get to the sum of the input signal and VDD, resulting the linearity degradation. To prevent this, a bootstrap switch is designed to be sufficiently linear.

To provide a constant supply current to overall ADC circuit, a self-biased V_{TH} current source is used as current generator (I_{Gen}) as shown in Fig. 2(b), instead of a big size band-gap reference circuit. With a big MN2 width, the bias current (I_{Gen}) is independent feature of supply variation.

3. The sampling skew correction

In the SHA-less ADC, the sampling skew (Δt) is inevitably increased by the intrinsic propagation delay mismatches between the two paths of the MDAC and sub-ADC. In sampling skew analysis at previous research [9], a maximally allowable sampling skew is derived as

$$Max(\Delta t) \le \frac{1}{2\pi f_{IN} 2^{N_{Sub\text{-}ADC}+1}}, \quad (1)$$

where $N_{Sub\text{-}ADC}$ is defined as the effective resolution of the sub-ADC and f_{IN} is the input frequency. At the ADC specifications of 200-MS/s and a 12-bit resolution, the maximum allowable Δt has to be guaranteed less than 200-ps from Eq. (1). Among the various sources of sampling skew, a pre-amplifier is major contributor as a dynamic sampling skew (DSS), and its variable delay time ($t_{Pre\text{-}Amp}$) [10] can be given as

$$t_{Pre-Amp} = \frac{1+g(f_{IN})}{2\pi \times f_{Pre\text{-}Amp}}, \quad (2)$$

where $f_{Pre\text{-}Amp}$ and f_{IN} are the -3 dB bandwidth of the pre-amplifier and input signal frequency, respectively, and g is a function with a proportionality of f_{IN}. Eq. (2) represents that the pre-amplifier delay time varies with f_{IN}, thereby the maximum tolerable sampling skew is achieved at the highest f_{IN} is injected.

With higher f_{IN}, $Max(\Delta t)$ is decreased and the sampling skew is required to be rejected more. The conventional layout scheme [5] has limitation in reducing the sampling skew of the high-speed

ADC, and the clocking technique [6] needs to be more accurate control circuits to compensate for the sampling skew.

A digital timing correction is suggested to reduce the DSS in high frequency input signals. Since the DSS is increased as input frequency is higher, an exact timing correction range should be predicted to reduce the DSS. Therefore, before the circuit design of the digital time corrector, a high-level simulation is required to find out a timing correction range of the DSS. For this simulation, the behavior model of the proposed ADC as shown in Fig. 1(c) is implemented with non-idealities. Fig. 3 shows the simulation results with swept sampling skew at three input signal frequencies (50, 78, and 100 MHz) at a sampling rate (200-MS/s). As simulation results, to assure the Nyquist operation, the maximum tolerable sampling skew range is achieved around 200-p, which value will be utilized to compensate an overall sampling skew degradation.

Fig. 4(a) and (b) shows a block detail of the digital timing corrector and its timing diagram, which explains operational

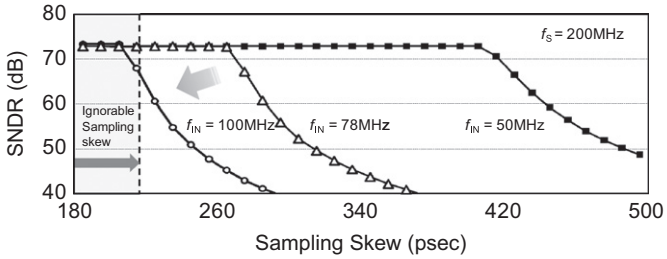

Fig. 3. MATLAB simulation results with increased sampling skew.

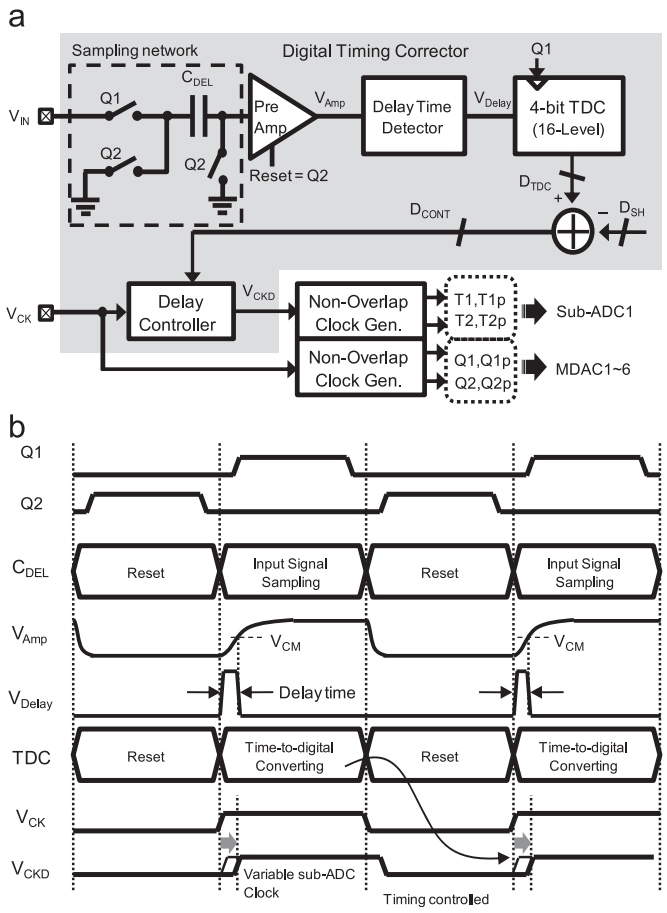

Fig. 4. (a) Block diagram of the digital timing corrector and (b) timing diagram.

principle. At first, a delay time detector measures the DSS generated in the dummy pre-amp at V_{Amp} in Fig. 4(a). The digital timing corrector transfers the measured DSS to time duration (V_{Delay}) based on a reference threshold voltage, and a 4-bit time-to-digital converter (TDC) changes V_{Delay} to 16-level different digital codes (D_{TDC}). These codes are revised to actual delay time data (D_{CONT}) by subtracting the delay generated in a sampling network (D_{SH}). The delay controller finally provides delay compensated clock signal (V_{CKD}) from the information of D_{CONT}. These delay correction is applied to the sub-ADC1s clock because its specification is looser than the MDAC1-6s.

These compensation mechanisms can be explained with the clock diagram in the qualitative manner as shown in Fig. 4(b). Q1 and Q2 signals make a delay time corrector to be operated an input signal or be reset, respectively. In the operation time (High Q1), V_{Amp} including the DSS is converted to a pulse waveform having a pulse-width. A 16-cascade inverter chain in the 4-bit TDC quantized with an accuracy of a 15-ps/1-LSB equally-implemented on the delay controller. The maximum allowable DSS is extended to 240 ps with the 16-cascade inverter chain. The output of 4-bit TDC is used to adjust V_{CK} delay time and the results are reflected at the next Q1 phase.

The proposed sampling skew correction is adopted in both two sub-channel ADCs to prevent spur generation from channel mismatch [11].

4. Capacitor swapped and trimmed MDAC

At the front-end stage of the proposed ADC, to reduce capacitor mismatches at the first MDAC, a periodic swapping of feedback capacitor is used. Fig. 5(a) shows the schematic of the MDAC1 in the sub-channel ADC. It consists of the merged-capacitor array [12], an op-amp, bootstrap switches, 4 switches (SW1-4), and an encoder and swapping logic. The clock signal Q1 and Q2 drive the MDAC1 for sampling and amplifying, respectively.

At the Q1 phase, the input signals (V_{INP} and V_{INN}) are sampled onto the capacitor array. The sub-ADC1 shown in Fig. 1(c) also samples the signal. With the quantized DAC output, the sampled signals are subtracted and extended to a residue output at the Q2 phase. The conventional capacitor swapping technique has disadvantages of circuit complexities in various switches implementation. Hence, in the proposed ADC, switch control signals (D_{SW1}-D_{SW4}) are swapped and applied to a MDAC switches (SW1-4) instead of the conventional mixing. The encoder and swapping logic in Fig. 5 provide the control signals to the MDAC switches for the capacitor swapping. Consequently, mismatches on the capacitors are suppressed in the proposed ADC output.

A circuit implementation of the MDAC switches can be further simplified in the proposed ADC. Fig. 5(b) shows a configuration of the MDAC switch. A left configuration in Fig. 5(b) represents a conventional triple-switch (TSW_S) architecture, which uses three voltage-leveled signals, excluding a feedback switch (SW_F). Whereas, in the proposed ADC, a double-switch (DST_S) architecture [13] is applied by removing a port of a common mode voltage (V_{CM}) and inserting a common mode switch (nSW). It leads to simplification of the switch composition and reduction of the layout area.

The capacitor swapping technique, however, accompanies harmonic offsets are raised by a periodic operation. To address the generation of the harmonic offset, the capacitor trimming scheme is suggested. Fig. 6 shows a block diagram, which describes a mechanism of the capacitor trimming for the CH-1.

The capacitor trimming block is composed with an address pointer and an offset register array, etc. The operation timing diagram is shown in Fig. 7. The address pointer assigns 4 swapping

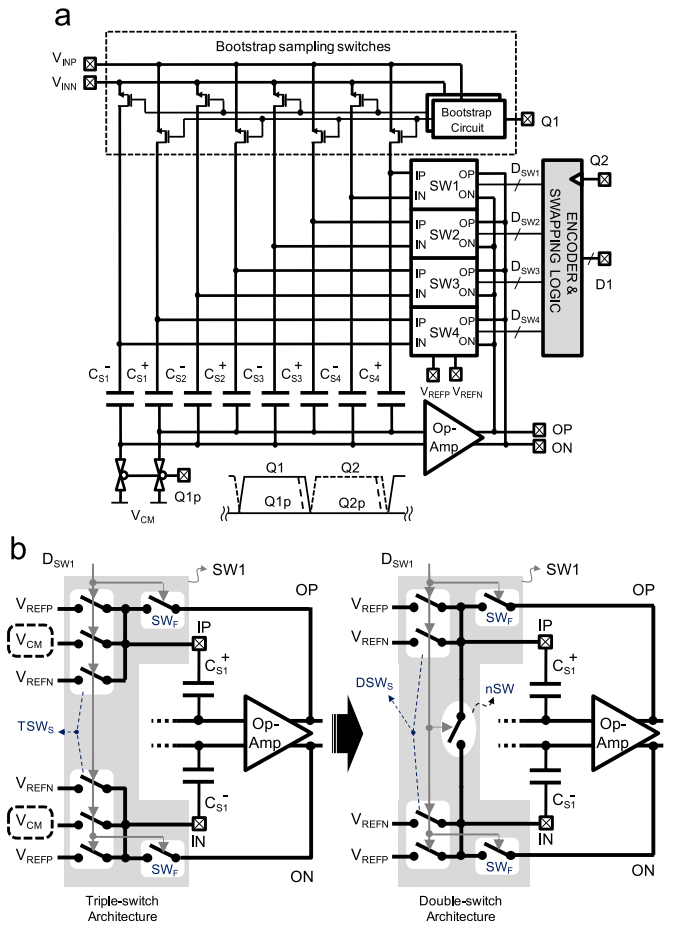

Fig. 5. Block diagram of (a) MDAC1 and (b) switch configurations of SW1.

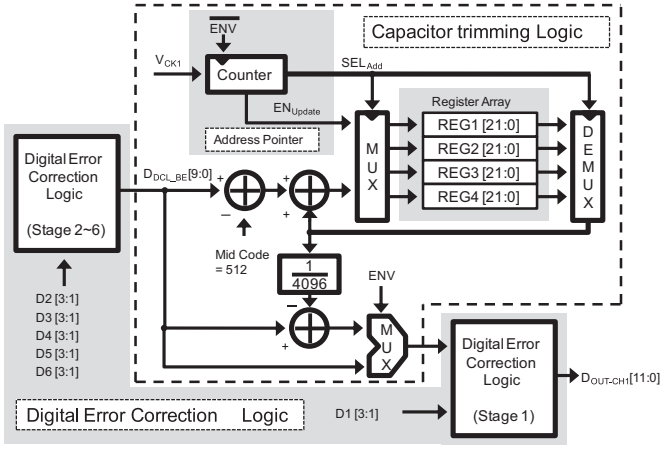

Fig. 6. Block diagram of the capacitor trimming logic.

compositions in each sub-channel ADC (CH-A and CH-B) to the designated resister with a counter output SEL_{Add} and then each register stores the offset states corresponding to the capacitor swapping compositions. After the offset states are accumulated by 4096 time and averaged by 1/4096, the offset estimation is completed. The estimated offsets in 4 registers (REG1–4) are subtracted from the back-end outputs (D_{DCL_BE}[9:0]) in corresponding register addresses (SEL_{Add}), respectively. The capacitor trimming operation at the high EN_{Update}, consequently, the original offset of the MDAC1 is removed by the predicted offset from the capacitor trimming at digital output signals ($D_{OUT\text{-}CH1}$[11:0]).

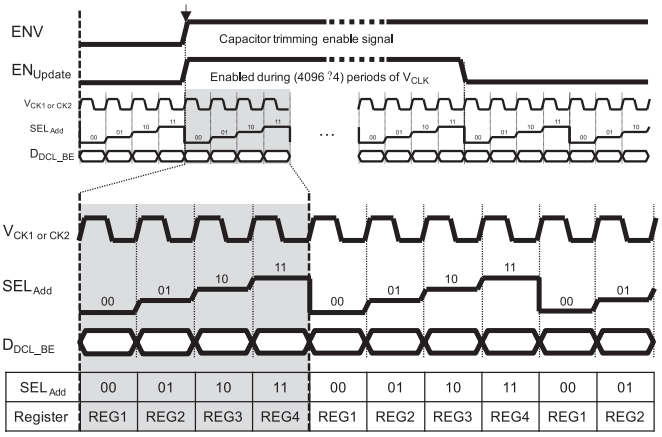

Fig. 7. Timing diagram of the capacitor trimming logic.

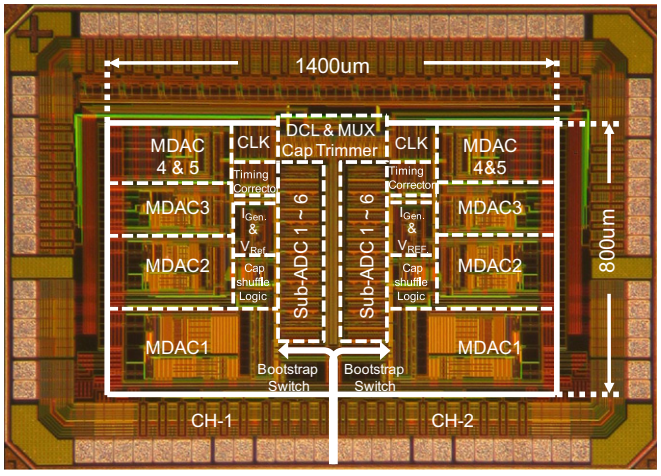

Fig. 8. Die photograph of the prototype ADC.

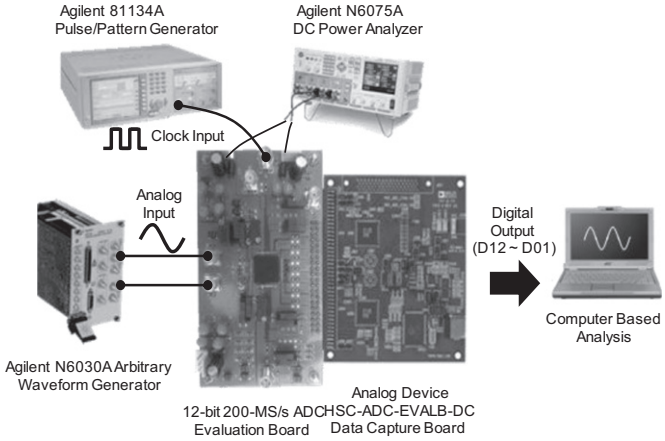

Fig. 9. Diagram of the measurement setup.

5. Experimental results and discussion

The proposed ADC is fabricated in a 65-nm 1P6M CMOS process with a metal-oxide-metal (MOM) capacitor. The die photograph of the proposed ADC is shown in Fig. 8. A total power consumption is about 112 mW (99.4 mW for the analog portion and 12.6 mW for the digital part) at a sampling rate of 200-MS/s with a 1.1 V supply.

As shown in Fig. 9, to measure the performance of the high-resolution and high-speed ADC, accurate input signal is provided

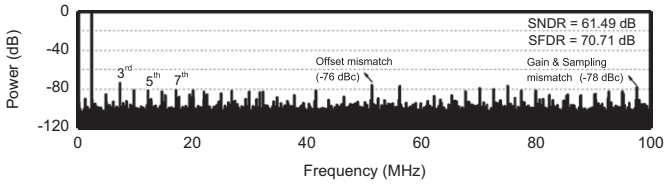

Fig. 10. Measured FFT plots at 2.4 MHz input and 200-MS/s data rate.

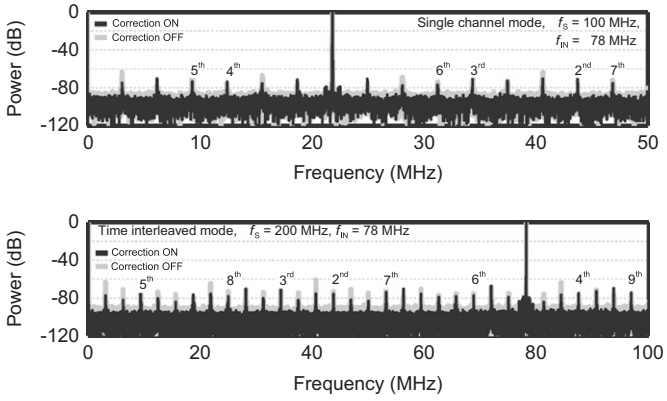

Fig. 11. Measured FFT plots before and after applying digital timing correction technique at 78 MHz input and 200-MS/s data rate.

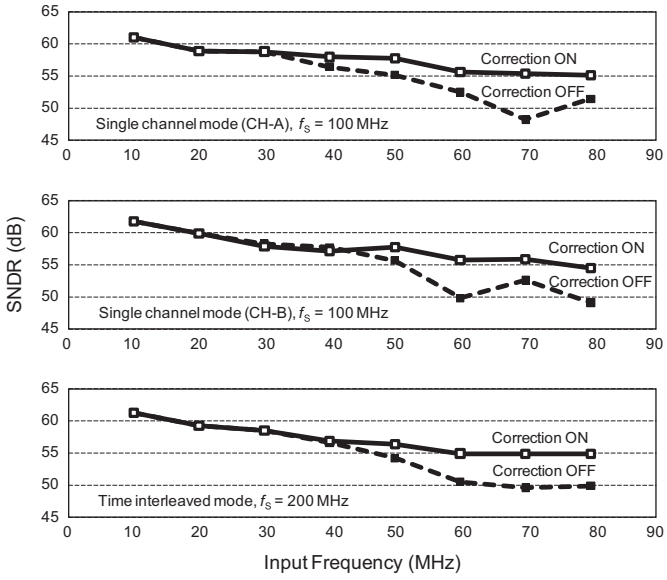

Fig. 12. Measured SNDR versus input frequency at 200-MS/s.

by an arbitrary-waveform-generator, Agilent N6030A (c.f., maximum output frequency is 78 MHz) in combination with an internal low-pass filter. A pulse-pattern-generator (Agilent 81134A) drives a low-jitter clock signal to the ADC. The digital outputs of the proposed ADC are captured by Analog Device HSC-ADC-EVALB evaluation board and observed in a PC monitor.

Figs. 10 and 11 show the measured dynamic performances of the proposed ADC. In Fig. 10, with an input frequency of 2.4 MHz, measured SNDR and SFDR were 61.49 dB and 70.71 dB, respectively. Dominant spurious tones due to channel mismatches from an offset and gain-plus-sampling are −76 dBc (at $f_S/4$) and −78 dBc (at $f_S/2-f_{IN}$), respectively [11]. In Fig. 11, the FFT spectrum is measured at on and off of the sampling skew

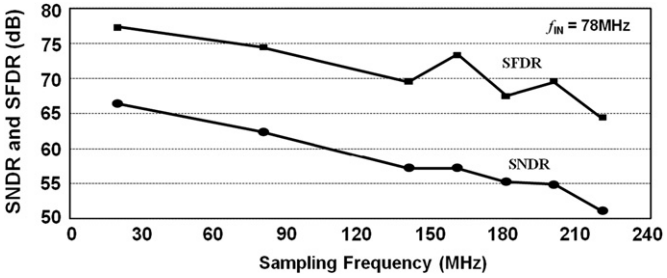

Fig. 13. Measured SNDR and SFDR versus sampling frequency at 78 MHz input frequency.

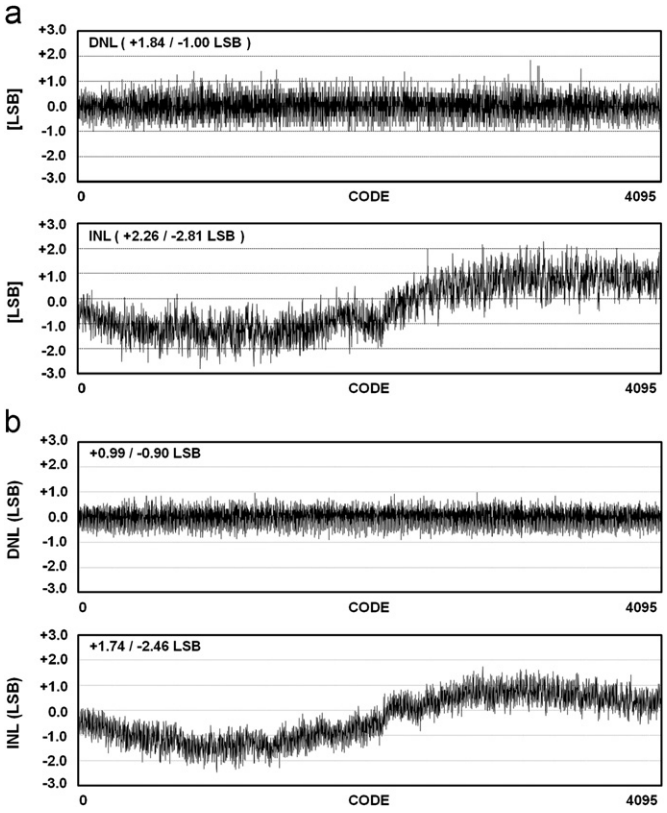

Fig. 14. Measured DNL and INL (a) before applying feedback capacitor swapping technique and (b) after applying the technique at 200-MS/s.

correction scheme for a 78 MHz input at 200-MS/s. The measured results with the correction scheme show the SNDR and SFDR of 54.86 dB and 64.12 dB, respectively. As shown in Fig. 11, the output spurs from the channel mismatch and SNR performance are enhanced by an adoption of the proposed correction schemes.

Fig. 12 summarizes the measured SNDR plots with an input frequency variation up to 78 MHz at on and off of the correction technique. At the higher input signal, the SNDR performances are prominently improved as shown in Fig. 12. At single channel and time-interleaved mode, the SNDR is observed the increased enhancement by 5 dB at the high-speed inputs. An ineffectiveness of the proposed sampling skew correction in the low input frequency (lower than 40 MHz in Fig. 12) was measured. Authors think that another dominant sources in the performance degradation at the low input may exist in unexpected mechanisms. Further researches seems to be needed in this issue.

Fig. 13 shows measured SNDR and SFDR for swept sampling frequencies of 78 MHz input. The ADC SNDR is above 54.86 dB until 200-MS/s.

Table 2
Performance summary and comparisons.

	[2]	[3]	This work
Technology	90-nm CMOS	65-nm CMOS	65-nm CMOS
Resolution	12-bit	11-bit	12-bit
Conversion rate	200-MS/s	200-MS/s	200-MS/s
Supply voltage	1.2 V	1.0 V	1.1 V
Input range	1.2 V_{pp}	1.0 V_{pp}	1.1 V_{pp}
DNL	+0.91/−0.76 LSB	+0.45/−0.53 LSB	+0.99/−0.90 LSB
INL	+1.55/−1.90 LSB	+0.87/−0.67 LSB	+1.74/−2.46 LSB
SNDR	61.60 dB @ f_{IN}=3.5 MHz 59.40 dB @ f_{IN}=91 MHz	62.2 dB @ f_{IN}=4.0 MHz 59.9 dB @ f_{IN}=60 MHz	61.49 dB @ f_{IN}=2.4 MHz 54.86 dB @ f_{IN}=78 MHz
Power consumption	186 mW (low bias mode)	180 mW	112 mW (Analog=99.4 mW) (Digital=12.6 mW)
FoM	0.96 pJ/conv. @ f_{IN}=3.5 MHz 1.22 pJ/conv. @ f_{IN}=91 MHz	0.85 pJ/conv. @ f_{IN}=4.0 MHz 0.93 pJ/conv. @ f_{IN}=60 MHz	0.58 pJ/conv. @ f_{IN}=2.4 MHz 1.24 pJ/conv. @ f_{IN}=78 MHz
Active area	1.36 mm^2 (800 μm × 1700 μm)	1.1 mm^2	1.12 mm^2 (800 μm × 1400 μm)

Fig. 14 shows the measured nonlinearity of the proposed ADC with 12-bit accuracy at 200-MS/s. The proposed ADC is measured with the capacitor swapping and trimming, and the conventional ADC without the techniques is also measured for the performance comparison. The measured DNL and INL in the conventional ADC are obtained as +1.84/−1.00 LSB and +2.26/−2.81 LSB, respectively (Fig. 14(a)). With the proposed technique, the measured DNL and INL are measured as +0.99/−0.90 LSB and +1.74/−2.46 LSB, respectively. The proposed technique enhances the DNL by 33.4% and the INL by 17.2%.

Table 2 is the performance comparison with the ADCs of similar performances, previously reported (200-MS/s sampling rate and around 12-bit resolution). For a fair comparison, the figure of merit (FoM)

$$\mathrm{FoM} = \frac{P}{2^{ENOB} \times f_S}, \tag{3}$$

is used, where P is the power dissipation, *ENOB* is the measured effective number of bits for an input frequency f_{IN} and sampling frequency f_S. As shown in Table 2, the power consumption is the lowest among the ADC and the FoM is 0.58 pJ and 1.24 pJ/conversion-step at 2.4 MHz and 78 MHz input signal, respectively. Therefore, the proposed ADC is useful in terms of a power consumption and high accuracy performance in a high conversion rate.

6. Conclusion

In this paper, a 12-bit dual channel pipelined ADC has been proposed. According to the proposed digital timing correction technique, the channel mismatch effect presented by harmonics on the frequency domain are suppressed below −76 dBc at a given 2.4 MHz input and are restrained below −64 dBc at a 78 MH input frequency. Moreover, the nonlinearities from capacitor mismatches are enhanced by the capacitor swapping technique and the result is confirmed by the measured INL and DNL. The prototype realized in the 65-nm CMOS technology achieved a peak SNDR of 61.49 dB with the FoM of 0.58 pJ/conversion-step at a 200 MHz sampling clock and 2.4 MHz input frequency.

Acknowledgements

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