A 300 kHz, 63 kW/L ZVT DC–DC Converter for 800-V Fuel Cell Electric Vehicles

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Abstract—In this article, one of the very first 800-V fuel cell DC–DC converter (FDC) is developed for the next-generation fuel cell electric vehicles. The higher boost gain ratio and switching loss associated with increasing dc-link voltage, along with gradually increasing power density and efficiency demanded in the next-generation EV power converters, make the conventional boost converter not suitable for 800-V FDC. This article proposes a new design approach in which a zero voltage transition (ZVT) high step-up dual floating output boost converter (DFOBC) is introduced. Due to higher voltage gain, the operating duty cycle of DFOBC is reduced and lies in the vicinity of $D = 0.5$, which reduces filter size. The ZVT cells greatly reduce switching losses at 300 kHz, which enables using only a single discrete SiC MOSFET for the main switch of 25-kW module, contributing to volume and cost reduction. Moreover, the proposed converter successfully demonstrates the possibility of using planar core and printed circuit board (PCB) windings at 100-kW power level, which is rarely seen in previous works. Finally, a 25-kW prototype of the proposed ZVT DFOBC is built and test. The power density of 63 kW/L excluding heatsink is achieved. The peak and full-load efficiency are measured to be 99.0% and 97.7%, respectively.

Index Terms—800 V electric vehicles, coupled inductor, fuel cell electric vehicles (FCEV), PCB winding, planar core, switching loss, ZVT cell.

I. INTRODUCTION

FUEL Cell Electric Vehicles (FCEVs) become an attractive option for eco-friendly vehicles due to: 1) zero emissions; 2) energy diversification; 3) short refueling time for long cruising range; 4) large power supply for household or emergencies; [1]–[8]. The world's first mass-produced FCEV is Hyundai Tucson in 2013, followed by Toyota Mirai in 2015.

In the FCEVs, as shown in Fig. 1, an FC stack is the main source that powered the load, and a propulsion battery is used
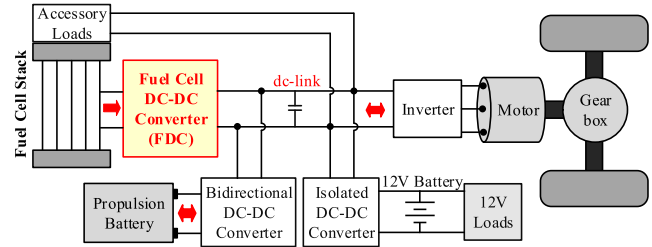
Fig. 1. Block diagram of the FCEVs.

to absorb the regenerative energy and operate the FC stack in its high-efficiency region by using a power management strategy, which increases the lifetime of the stack and reduces the total fuel consumption of the vehicle [1], [4], [5]. With this configuration, FC DC–DC converter (FDC) is a key component of the FCEV since it processes the main power and boosts the low and nonregulated FC voltage of 200–400 V, in general, to the desired level of dc-link voltage which varies from 500 to 650 V as so far reported.

Recently, along with the development of 800-V system for battery electric vehicles (BEVs) [9], [10], increasing the dc-link voltage of the FCEVs to 800 V is considered by manufacturers. Because the benefits of a higher dc-link voltage system will be inherited for FCEVs, such as lighter vehicle weight, higher efficiency, higher motor power, and wider speed range. In addition, other components such as inverters, motors, or isolated dc–dc converters that have been manufactured for 800-V BEVs can be utilized for 800-V FCEVs. However, increasing dc-link voltage makes the design of FDC more challenging due to the higher voltage gain ratio, switching losses, and cost. In response to these concerns, this research focuses on the design of FDC for the 800-V FCEVs, which has not been investigated in the previous literature.

Several designs of FDC have been presented in the previous works [3]–[5], [11]. The FDC of Toyota Mirai [4] uses a four-phase interleaved boost converter to process a high power of 114 kW, and its maximum dc-link voltage is about 650 V. A phase shedding (PS) control is used in this four-phase interleaved structure to improve the light load efficiency, which is beneficial in vehicular applications. The switching frequency is randomly changed over time to reduce the noise and vibration. However, it is expected to be lower than 20 kHz since the converter adopts silicon IGBT power modules and operates with hard switching. The individual inductor used in each phase is designed with a

bulky core and solid wire. The reported volume of Toyota FDC is 13 L equating to a power density of 8.8 kW/L.

The FDC in [11] utilizes a six-phase interleaved boost converter to process power of 100 kW, and the dc-link voltage is about 400 V. To reduce the volume of passive components, the switching frequency in this converter is set to 150 kHz. The high switching frequency is realized by a customized power module which consists of eight parallel Si super-junction MOSFETs and twelve SiC-Schottky diodes in each phase. Since multi-MOSFETs are connected in parallel, the conduction loss is significantly reduced. Therefore, high efficiency of 98% is achieved at the full-load condition. A PM core and solid wire are used for the inductor in each phase. In spite of using a high frequency of 150 kHz, the power density achieved is 6.2 kW/L.

In Honda FCV [5], a 100-kW FDC is designed with two modules of a two-phase interleaved boost converter, and the dc-link voltage is set to 500 V. In each module, an inverse coupled inductor is used to reduce the magnetic volume, which is designed by a gapless core and solid wire. In addition, a full SiC power module is used for the switch and diode, and the PS control is also adopted. As reported by Honda, the total converter volume is reduced by 40% compared to the predecessor, yielding a power density of 6.3 kW/L.

From the brief literature review mentioned above, the previous works on FDC are usually based on the following approaches.

1) The hard switching multiphases interleaved boost converter is generally used, and research articles focus mainly on reducing the volume of the passive components by using the coupled inductor or increasing switching frequency with SiC devices.

2) The bulky power module type is used for the switch and diode since it has high current rating, low thermal conductivity, and conduction loss.

3) The high-power inductor is designed using a bulky core and solid wire or Litz wire.

The previous FDCs confirmed the power density below 10 kW/L. However, as the dc-link voltage increases along with the gradually increasing power density and efficiency demand for the next generation EV power converters [12], a question arises whether the previous design approaches are still a suitable option or not for the 800-V FDC.

Other dc–dc converters for EV applications have been reported with high power density [13]–[15]. Mitsubishi introduces a 65 kW, interleaved boost converter in [13]. The input and output voltage are reported at 350 and 600 V, respectively. By replacing the IGBT and free-wheeling diode with the SiC MOSFET and the Schottky barrier diode, the switching frequency could be increased from 20 to 50 kHz, achieving a high power density of 26.5 kW/L excluding heatsink, which is a 71% reduction compared to the predecessor. In [14], an 80 kW bidirectional dc–dc converter is built to interface between battery and dc-link using the 1200 V–300 A SiC power module MOSFET. The battery voltage varies from 300 to 380 V, and the dc-link voltage is set to 750 V. By applying a multiobjective optimization method, this converter achieves a high power density of 31.4 kW/L, including heatsink, at the switching frequency of about 115 kHz. Waffler *et al.* [15] introduce a bidirectional cascaded buck–boost converter with a multiobjective optimization algorithm. The
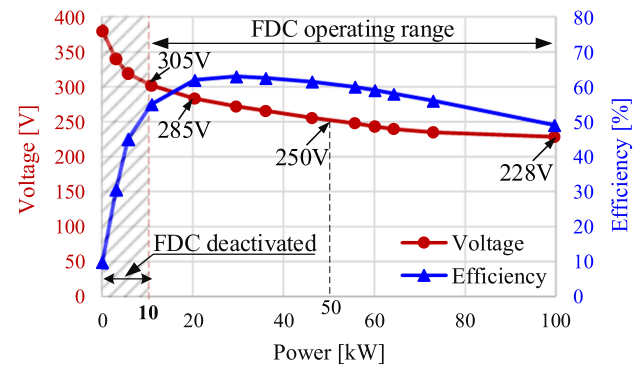

Fig. 2.   Output voltage and efficiency of 100-kW FC stack.

input and output voltages vary from 150 to 450 V, and the peak power is 70 kW occurred at 280 V input. Authors clamp that power density of 48 kW/L could be realized at 70 kW and 150 kHz. However, only a 12-kW prototype operated at 100 kHz is shown with a power density of 30 kW/L, including heatsink.

Even though the aforementioned EV power converters achieve impressive power density [13]–[15], the maximum power of which occurs at the medium or high input voltage, leading to lower inductor current and losses compared to that of the FDC. In addition, the boost gain ratio and power rating of these converters are also smaller than that of 800-V FDC. It is noted that FDC is usually rated above 100-kW power level, and its maximum power occurs at the minimum FC voltage leading to current rating and losses are worst. For this reason, the FDC design is more challenging, and FDC's power density is usually lower than dc–dc converters in other applications, even with the same power level.

This article proposes a new approach for FDC design to achieve high power density and efficiency targets. Four modules of the soft-switching high step-up converter are introduced to process 100-kW power from the FC stack. Due to the elimination of the switching loss by the ZVT cell, the proposed converter is able to operate at 300 kHz with only one discrete SiC MOSFET TO-247 package per phase. Moreover, due to the high step-up ratio, the proposed converter's operating duty cycle lies in the vicinity of 0.5, which reduces the required inductance and capacitance values of the input and output filters. The selection of a suitable converter with a lower current ripple and high switching operation allows using planar core and PCB winding for the main inductor. It is shown that the proposed converter has a smaller volume, lower loss, and cost compared to the so far reported FDC in the literature. A 25-kW prototype of one module of the proposed 800-V FDC operated at 300 kHz is built and tested to verify the theoretical analysis.

II. TECHNICAL TARGETS AND PROPOSED DESIGN APPROACHES

A. Specifications and Technical Targets

The polarization curve and efficiency curve of a 100-kW FC stack used in this project are shown in Fig. 2. It can be seen from the shaded area of Fig. 2 that a common issue of the FC stack is low efficiency at the light load, which results in considerable fuel

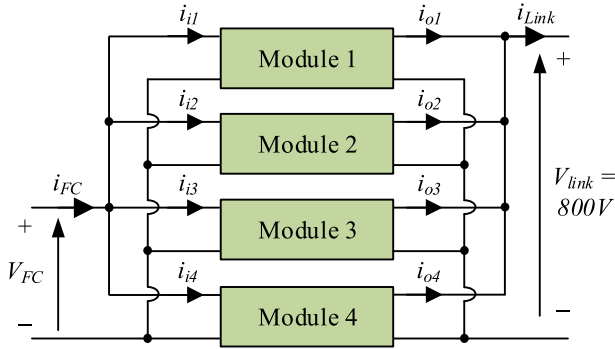| Parameters	Values
Power P_o	100 kW
Dc-link voltage	800 V
Input voltage V_{FC}	228 V – 305V
Maximum stack current $I_{FC,max}$	439A @ 228V
Efficiency at full load	> 97 %
Efficiency at 20% load (V_{FC} = 290V, P_{FC} = 20kW)	> 98 %
Power density excluding heatsink	> 50 kW/L
Maximum height excluding heatsink	28mm

Fig. 4. Possible topology for each module using the CIBC with coupled inductor, as being used in new Honda FCV [5].

Fig. 3. Proposed structure for 100-kW FDC.

Fig. 5. Normalized input current ripple of CIBC and DFOBC and their operating duty cycle ranges.

consumption. Therefore, in FCEV applications, FDC is usually deactivated at the low-load driving condition, and the vehicle is powered only by the battery [1], [16]. As a result, the considered fuel cell voltage range in this article is from 228 to 305 V even though the output voltage of the FC stack goes up to 380 V at a very low power level. With the given FC stack, the main design specifications and technical targets of the FDC in this project are given in Table I.

B. Proposed Converter

The interleaving converter is generally adopted in the FDC designs to deal with the high current rating of the FC stack. For this structure, one or several modules can be disabled at the light-load condition to reduce both magnetic and switching losses which lead to higher efficiency, so-called PS control [4], [5], [17], [18]. Moreover, the reliability of the converter is also increased in such a way that if one or more of the modules fails in some way, the converter is able to keep operating under derating mode with other modules until the vehicle reaches the repairment store, which is critical in vehicular applications. In this project, four modules connected in parallel are selected, as shown in Fig. 3. It is noted that the number of modules with a power of 2 (2^N where N is an integer) should be selected for PS control to avoid online changing the phase angles of the carrier signals according to the number of operating modules. This article discusses the first phase of the project that focuses on the design of each individual 25 kW module to achieve the highest possible power density by increasing the switching frequency while maintaining an acceptable temperature rise and efficiency.
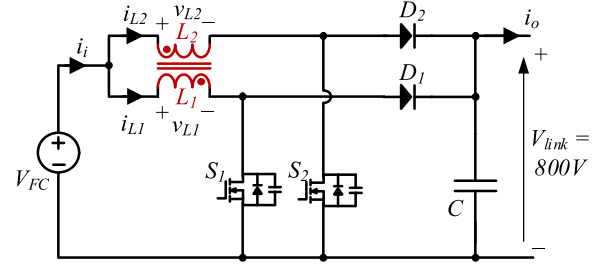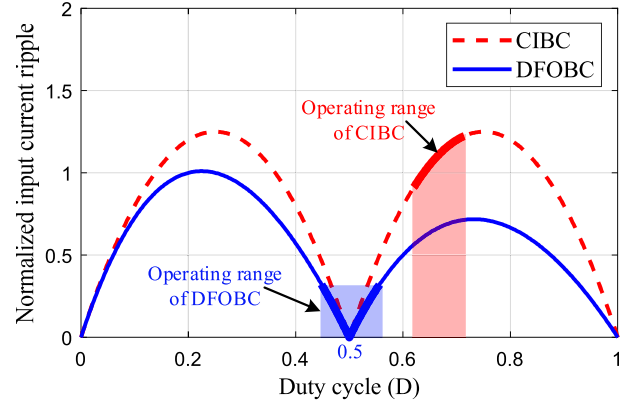
Now, selecting a suitable step-up converter for each module is an important task. The conventional interleaved boost converter (CIBC), which has been widely used in the previous design of the FDC, could be considered, as shown in Fig. 4. In this configuration, the inverse coupled inductor is adopted to reduce the magnetic volume and loss, as demonstrated in recent years [19]–[24]. However, due to the high dc-link voltage of 800 V, the operating duty cycle of the CIBC lies in the vicinity of $D = 0.7$, which makes the ripple reduction of the two-phase interleaving ineffective, leading to large inductor and capacitor volume, as seen in Fig. 5. Moreover, the CIBC operates with hard switching condition which limits the switching frequency of the converter leading to lower power density and efficiency.

In response to these concerns, the soft switching dual floating output boost converter (DFOBC) [25]–[27], as shown in Fig. 6, is introduced for 800-V FDC design in this article. Due to higher voltage gain, the operating duty cycle of DFOBC lies in the vicinity of $D = 0.5$, which maximizes the effect of ripple reduction of the two-phase interleaved converters, thereby significantly reducing the inductor and capacitor volume. Two ZVT cells are employed to provide the soft-switching condition for the main switches and main diodes of the DFOBC. Since the switching loss is reduced, the converter is able to operate at a higher switching frequency under the same cooling system. This proposed soft-switching approach not only reduces the passive component volume but increases the light load efficiency of the converter, which is critical in automotive applications [28]. Once ZVT cells are employed in the 800-V FDC, the DFOBC

TABLE II
APPLICABILITY OF THE ZVT CELLS TO DFOBC AND CIBC USED FOR 800 V FDC

| Features	[30] (This work)	[31]	[32]	[33]
Circuit diagram				
Main switch turns ON	ZVS	ZVS	ZVS	ZVS
Main switch turns OFF	ZVS	ZVS	Near ZVS	Hard switching
Snubber switch turns ON	ZCS	ZCS	ZCS	ZCS
Snubber switch turns OFF	ZVS	ZVS	ZVS	ZVS
Voltage rating of snubber switch S_s	V_o	$V_o + V_{Cs}$	V_o	V_o
Voltage rating of blocking diode D_{s1}	$2V_o$	V_o	V_o	V_o
Component count	Low	Medium	Low	Medium
Applicable converters for 800V FDC	Only DFOBC	Only DFOBC	CIBC DFOBC	CIBC DFOBC
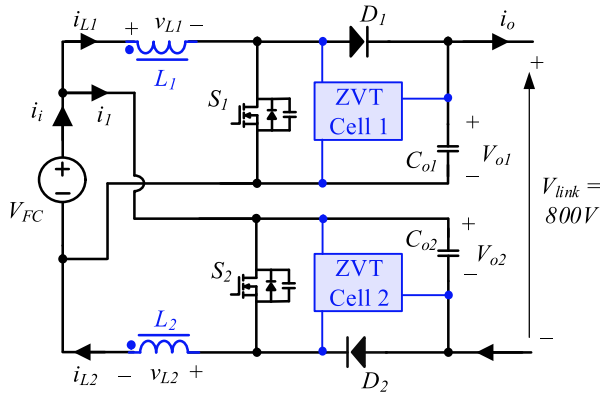
Fig. 6. Proposed designed approach for each module based on the DFOBC and ZVT cell.

with lower voltage stress imposed on the devices shows other advantages over the CIBC such as higher flexibility to the ZVT cell selection and smaller the demand energy to discharge C_{oss} of the main switch, which will be detailed in the following section.

In the next generation of FCEV, automotive companies want to extend the driving range to above 800 km while realizing a more spacious cabin for more passengers. In order to do that, the volume of the hydrogen tank and propulsion battery is increased, while the volume of the power electronics component must be minimized. In this project, the car layout has already been designed in which all the power converters and the FC stack share a cramped space under the car's front hood. Hence, only 45 mm height, including heatsink and house, is available for the FDC. Therefore, the converter with a maximum height of 28 mm, excluding the heatsink, is given as a project constraint. This makes the PCB structure and coupled inductor optimization essential to achieve high power density and low-profile targets. Notice that low-profile power converters with high power density are also a key solution to realize an EV skateboard chassis architecture, a future trend of EV manufacturing [12], [29].

Since the coupled inductor has the biggest volume in the built-up FDC, special care has been taken to optimize the volume. For low profile, the planar core inductor with PCB windings is introduced. Moreover, the use of PCB winding contributes to the reduction of manufacturing time and cost since the complex wire wrap process is eliminated. In addition to inductor volume reduction, the multiboard assembly structure is also introduced to reduce the total converter volume as well.

III. ZVT CELL SELECTION AND REALIZATION OF 300-kHz, 25-kW CONVERTER USING DISCRETE TYPE TO-247 PACKAGE SIC MOSFET

A. ZVT Cell Selection

Basically, the ZVT cell provides complete zero voltage switching (ZVS) turn-ON for the main switch of the converter. However, its turn-OFF performance is usually a tradeoff between the ZVS and extra voltage stress imposed on the auxiliary components. As an example, four represented ZVT cells [30]–[33] are shown in Table II. It can be seen that the main switch in [30] and [31] turns OFF with the complete ZVS; however, the blocking diode in [30] and the snubber switch in [31] have extra voltage stress. On the other hand, the main switches in [32] and [33] do not achieve complete ZVS turn-OFF, but snubber components have no extra voltage stress. Assuming that the maximum voltage rating can be chosen for the snubber diode is 1200 V, the DFOBC is able to utilize all the ZVT cells since its output capacitor voltage is low that enables it to have the extra voltage stress. In the case of CIBC, the ZVT cell with extra voltage stress, as [30] and [31], cannot be used since the maximum voltage of the snubber devices could reach 1600 V for 800 V output. Therefore, the DFOBC shows higher flexibility in the ZVT cell selection compared to the CIBC in the 800-V FDC design.

In this article, to maximize the main switch's current conductivity, the fully soft switched ZVT cell in [30] is employed for the DFOBC to eliminate the switching loss at both turning ON and OFF. However, the original ZVT cell presented in [30] have been
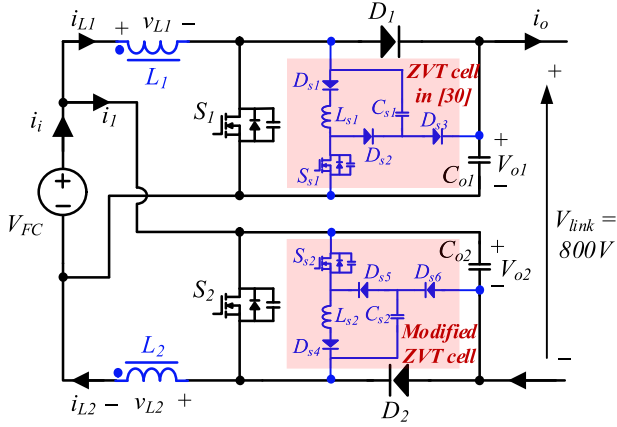
Fig. 7. Proposed converter with selected ZVT cell in [30] and its modified version for a module of 25 kW FDC.
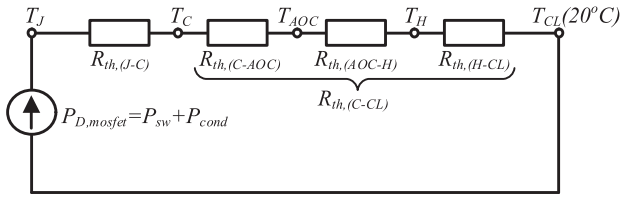

Fig. 8. Equivalent thermal circuit of the MOSFET and cooling system.

proposed for only boost converters, thus only can be applied for the upper leg of the DFOBC; therefore, another modified ZVT cell based on [30] is introduced to adapt to the lower leg of the DFOBC, as seen in Fig. 7. In principle, the upper and lower ZVT cells' operation and design procedures are identical, and only the current direction is reversed. The design procedure for the ZVT has already been detailed in [30] and will not be presented in this article.

B. Realization of 300-kHz, 25-kW Converter Using Discrete TO-247 Package SIC MOSFET

In power converter design, the total power losses of a MOSFET including switching loss and conduction loss must be kept lower than the maximum allowable power dissipation to ensure that the temperature rise of the MOSFET does not exceed a specified value under full load condition, which can be expressed by

$$P_{\text{cond}} + P_{\text{sw}} \leq P_{D,\max}(\Delta T) = \frac{\Delta T}{R_{\text{th}(J-C)} + R_{\text{th}(C-CL)}} \tag{1}$$

where ΔT is the allowable temperature rise of the MOSFET, which is a difference between junction and coolant temperatures (T_J-T_{CL}); $R_{\text{th}(J-C)}$ is a junction-to-case thermal resistance which is given in the MOSFET datasheet; $R_{\text{th}(C-CL)}$ is a total case-to-coolant thermal resistance which depends on the cooling system; P_{cond} and P_{sw} are the conduction and switching losses of the MOSFET, respectively; $P_{D,\max}(\Delta T)$ is the maximum allowable power dissipation in one MOSFET with the given ΔT. The calculation of P_{sw} and P_{cond} is based on [34].

The equivalent thermal circuit of the MOSFET and cooling system is shown in Fig. 8. An automotive-qualified SiC MOSFET

TABLE III
COOLING SYSTEM SPECIFICATIONS

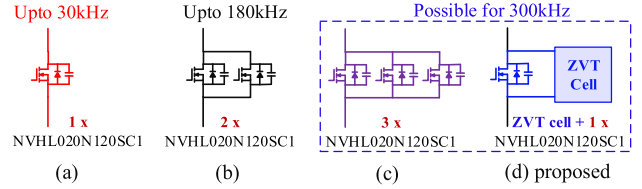| Items	Values
Junction-to-Case, $R_{th(J\text{-}C)}$	0.28 (°C/W)
Case-to-AOC, $R_{th(C\text{-}AOC)}$	0.26 (°C/W)
AOC-to-Heatsink, $R_{th(AOC\text{-}H)}$	0.08 (°C/W)
Heatsink-to-Coolant, $R_{th(H\text{-}CL)}$	0.14 (°C/W)
Coolant temperature	20 (°C)
Maximum temperature rise ΔT	80 (°C)

Fig. 9. Four cases of main switch structure: (a) one MOSFET per phase without ZVT cell; (b) two MOSFETS per phase without ZVT cell; (c) three MOSFETS per phase without ZVT cell; (d) one MOSFET per phase with ZVT cell.

NVHL020N120SC1 from ON semiconductor with $R_{ds,\text{on}} = 28$ mΩ is selected for the main switch of the DFOBC, and a low thermal conductivity insulator aluminum oxide ceramic (AOC) is used as a thermal interface material (TIM) between the switch and heatsink. The specifications of the cooling system are shown in Table III.

The experiment is conducted with the coolant temperature T_{CL} of 20 °C. The maximum temperature rise of the SiC MOSFET given by the project is 80 °C. It is noted that even though the selected SiC devices have the highest operating junction temperature of 175 °C, the engine room temperature inside the car could reach the maximum of 60 °C; therefore, only 80 °C is allowed for the temperature rise considering the margin. The total case-to-coolant thermal resistance of $R_{\text{th}(c\text{-}a)} = 0.48$ °C/W determined based on Table III. Therefore, the maximum allowable power dissipation of the selected SiC MOSFET is obtained of $P_{D,\max}(80\ °C) = 105.3$ W.

To clarify the advantages of using ZVT cell in high-power and high switching frequency converter designs, the loss and cost analysis of the main switch of the DFOBC in 800-V FDC is presented. Four cases of the main switch structure with and without ZVT cell are shown in Fig. 9. The power losses, including conduction and switching losses of one MOSFET in each case, are calculated at the full load condition of $P_o = 25$ kW and $V_i = 228$ V. After that, the results of which are compared to the $P_{D,\max}(80\ °C)$ to evaluate the possible switching frequency for each case, as shown in Fig. 10. It is noted that in the case of using ZVT cell, 10% of the switching loss is assumed to remain in the main switch for the margin even though there is theoretically no switching loss due to the complete ZVS turning ON and OFF.

As seen in Fig. 10, for hard switching operation, the converter can only operate up to 30 kHz in the case of Fig. 9(a) with a single discrete SiC MOSFET per phase due to high conduction loss. Even though two MOSFETs are connected in parallel to reduce the conduction loss by four times, as in the case of Fig. 9(b),
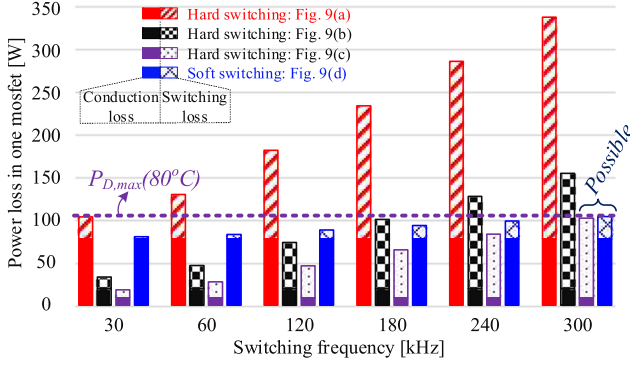
Fig. 10. Power losses analysis in one MOSFET with four different cases of main switch structure, calculated for the 25 kW DFOBC with input voltage of 228 V. The discrete type SiC MOSFET NVHL020N120SC1 is used for all the cases.

Fig. 11. Loss and cost comparisons between two possibilities of the 300-kHz switching frequency: (a) Loss; (b) Cost (the cost is based on digikey.com in November 2020).
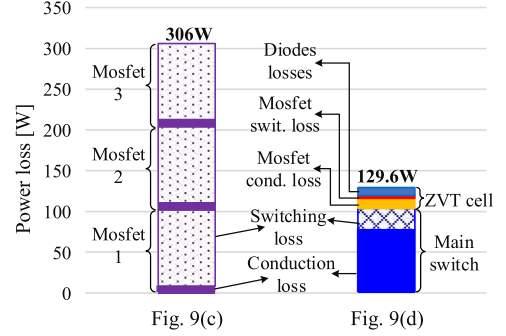
the switching frequency is still limited to 180 kHz. Based on the analysis in Fig. 10, the highest possible switching frequency of the proposed converter is 300 kHz. Two possible strategies to achieve that high switching frequency in the 25-kW 800-V FDC design are the following. First, operating the converter under hard switching condition with three discrete SiC MOSFETS connected in parallel per phase, as in the case of Fig. 9(c); second, operating the converter under soft-switching condition with a single discrete SiC MOSFET and a ZVT cell per phase, as in case of Fig. 9(d).

Even though the power losses of one MOSFET in the case of Fig. 9(c) is similar to that of Fig. 9(d), the total power losses of the main switch structure with three hard-switching MOSFETS of Fig. 9(c) is significantly higher than that of Fig. 9(d), as seen in Fig. 11(a). In addition, the total component costs in the case of Fig. 9(c) is about 16.9% higher than that of Fig. 9(d) due to the cost of high power MOSFETS, as shown in Fig. 11(b) (cost was based on digikey.com in November 2020). As a result, the proposed soft-switching strategy in Fig. 9(d) is more beneficial than the conventional hard-switching design in both efficiency and cost. Moreover, the required energy for the gate driver in Fig. 9(c) with three high-power MOSFETs is much higher than that of the proposed method which only includes one high-power MOSFET for the main switch and one low-power MOSFET for the ZVT cell.

IV. INVERSE COUPLED INDUCTOR DESIGN WITH PROPOSED MODIFIED E CORE AND PCB WINDINGS

This section provides an inverse coupled inductor design procedure using planar core and PCB winding to achieve high power density and low profile target. The mathematic equations of the inversed coupled inductor are obtained by a similar method in [18], thus will not be presented in this article.

In this first phase of the project, maximizing switching frequency to achieve the highest possible power density under an acceptable temperature rise is the first priority. Therefore, the switching frequency of 300 kHz is selected considering the maximum main switch temperature of the proposed converter, as shown in Fig. 10.
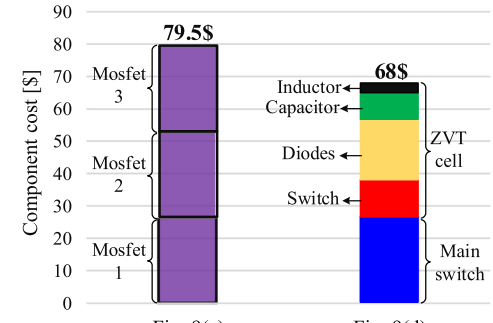
A. Coupling Coefficient

Developing a precise formula to calculate the coupling coefficient k is very complicated and can be applied to only a specific core shape and winding structure. Moreover, the leakage inductance value is not a critical factor in the nonisolated power converter's design, as it is in the isolated converter. Therefore, this article introduces a suitable range of coupling coefficient k for the inverse coupled inductor considering the current ripple and core loss, which is missing in the literature. Since the precise calculation method of k is eliminated, the inverse coupled inductor's design procedure is much more straightforward.

The winding and input current ripples of the inverse coupled inductor used in the DFOBC can be expressed as

$$\begin{cases} \Delta i_L = \frac{V_{\text{Link}} \cdot (1 - D - D \cdot k) \cdot D}{L \cdot (1 - k^2) \cdot (1 + D) \cdot f_s} & \text{when } D \le 0.5 \\ \Delta i_L = \frac{-V_{\text{Link}} \cdot (k - D - D \cdot k) \cdot (1 - D)}{L \cdot (1 - k^2) \cdot (1 + D) \cdot f_s} & \text{when } D > 0.5 \end{cases} \quad (2)$$

$$\begin{cases} \Delta i_i = \frac{V_{\text{Link}} \cdot (1 - 2 \cdot D) \cdot D}{L \cdot (1 - k) \cdot (1 + D) \cdot f_s} & \text{when } D \le 0.5 \\ \Delta i_i = \frac{V_{\text{Link}} \cdot (2 \cdot D - 1) \cdot (1 - D)}{L \cdot (1 - k) \cdot (1 + D) \cdot f_s} & \text{when } D > 0.5. \end{cases} \quad (3)$$

From (2) and (3), the normalized winding and input current ripples as a function of coupling coefficient k are drawn and shown in Fig. 13. The current ripples drastically increase when k is higher than 0.96, making the converter very sensitive with k tolerance. Therefore, a coupling coefficient smaller than 0.96 is recommended, thereby avoiding the use of an auxiliary inductor to limit the current ripples [20], [21]. Also, the small value of k
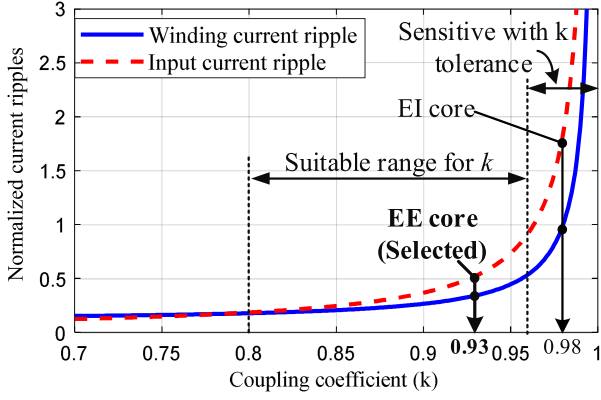
Fig. 12. Normalized winding and input current ripples of the inverse coupled inductor with $\frac{V_o}{L \cdot f_s} = 1$ and $D = 0.448$.

Fig. 13. Required N·ac of the inverse coupled inductor, calculated at 300 kHz, $k = 0.93$, $B_{\max} = 150$ mT, with $L = 28\ \mu$H.

leads to not only higher magnetizing current ripple, increasing the core loss [21], but high leakage flux, causing errors in other electronic devices in the circuit [35]. Therefore, the suitable range of k is selected in between 0.8 and 0.96, as shown in Fig. 12.

Even though k can be flexibly selected from the range mentioned above, it is not always practically achieved k within this range without using the extra magnetic shield. As an example, two well-known cores, EE and EI cores, have been evaluated in this project, and the results show that the use of EE core can achieve a lower coupling coefficient than EI core for the same PCB windings structure and the number of turns. The main reason for this can be explained as follows: in the case of EE core, two windings of the coupled inductor are placed in two separated E core with an air gap in between, the leakage flux of two windings is, therefore, high due to the air-gap, leading to low coupling coefficient. However, in the case of EI core, two windings are placed in the same E core without air gap between the windings, thus lower leakage flux and higher coupling coefficient. Obtaining from the experimental results, EE core with the coupling coefficient $k = 0.93$ is chosen, as shown in Fig. 12.

B. Self-Inductance

The self-inductance in this project is designed to ensure that the input current ripple is kept lower than 10% of its maximum value of 439 A, as given in Table I. The worst case of input current ripple is considered when the converter operates with a single module, which confirms duty cycle $D = 0.448$ in the case of using DFOBC, as seen in Fig. 6. Therefore, the required self-inductance is obtained based on (3) by $L = 28\ \mu$H.

C. Number of Turns and Cross-Sectional Area of the Core

The maximum operating magnetic flux density of the core is expressed by

$$B_{\max} = \frac{L \cdot I_{M,\text{peak}}}{N \cdot A_c} \qquad (4)$$

where N is the number of turns; A_c is the cross-sectional area of the core; $i_{M,\text{peak}}$ is the peak value of the magnetizing current
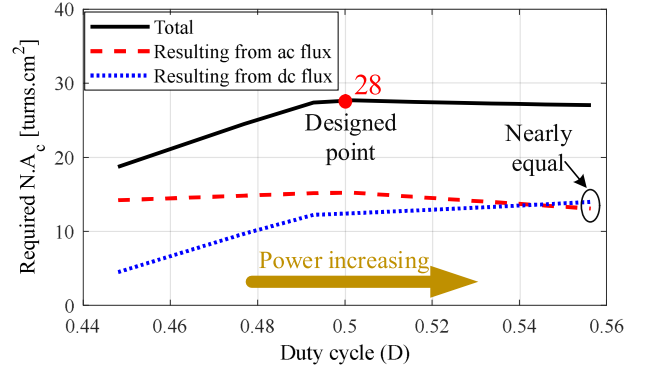
which can be calculated as

$$\begin{cases} i_{M,\text{peak}} = \frac{(1-k) \cdot P_{\text{FC}}}{V_{\text{Link}} \cdot (1-D)} + \frac{V_{\text{Link}} \cdot D}{2 \cdot L \cdot f_s \cdot (1+D) \cdot (1+k)} & \text{when } D \leq 0.5 \\[2mm] i_{\text{peak}} = \frac{(1-k) \cdot P_{\text{FC}}}{V_{\text{Link}} \cdot (1-D)} + \frac{V_{\text{Link}} \cdot (1-D)}{2 \cdot L \cdot f_s \cdot (1+D) \cdot (1+k)} & \text{when } D > 0.5. \end{cases} \qquad (5)$$

The first term on the right side of (5) represents the dc magnetizing current, which is a power-dependent factor. The second term on the right side of (5) represents the ac magnetizing current, which has a significant impact on the inductor's core loss.

From (4) and (5), a product of N and A_c is obtained

$$\begin{cases} N \cdot A_c = \frac{L \cdot (1-k) \cdot P_{\text{FC}}}{B_{\max} \cdot V_{\text{Link}} \cdot (1-D)} + \frac{V_{\text{Link}} \cdot D}{2 \cdot B_{\max} \cdot f_s \cdot (1+D) \cdot (1+k)} \\ \qquad \text{when } D < 0.5 \\[2mm] N \cdot A_c = \frac{L \cdot (1-k) \cdot P_{\text{FC}}}{B_{\max} \cdot V_{\text{Link}} \cdot (1-D)} + \frac{V_{\text{Link}} \cdot (1-D)}{2 \cdot B_{\max} \cdot f_s \cdot (1+D) \cdot (1+k)} \\ \qquad \text{when } D < 0.5. \end{cases} \qquad (6)$$

For 300-kHz switching frequency, soft ferrite material ML95S is chosen as it has low and stable core loss density in a wide range of operating temperatures. The $B_{\max}$ is set to 35%B_{sat} of 150 mT considering both ac and dc flux. It is noted that dc flux does not significantly impact the core loss. Therefore, only ac flux density is considered in the core loss density calculation. Assuming that when the FC power is higher than 25 kW, the power of each module P_{FC} in (6) is maintained at the maximum value of 25 kW, the required $N \cdot A_c$ of the inverse coupled inductor as a function of duty cycle is shown in Fig. 13. The designed value of $N \cdot A_c$ is set to be 28 turn·cm^2 which is used to optimize the number of turns N and cross-sectional area A_c of the customized core in the later section.

D. Proposed Modified E Core

In the conventional E core, the width of the outer leg b is equal to that of the center leg, leading to a large dead area and high profile. This issue is worse in the case of using PCB winding in high power applications since the PCB trace width w_t is large and the height of window e is very small compared to the core thickness c ($e << c$), as shown in Fig. 14(a). Therefore, a modified E core is proposed in this article, in which the thick and short outer leg of the conventional E core is modified to be thinner and longer in the proposed E core ($b_m > b$ and $c_m < c$), as seen in Fig. 14(b).
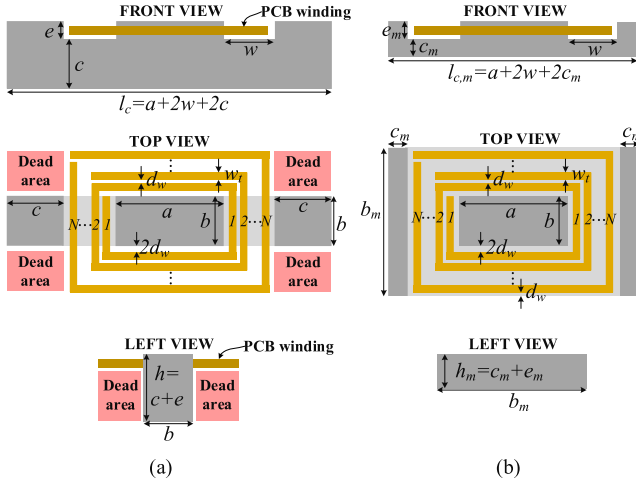
Fig. 14. Different between two core structures with PCB winding: (a) conventional E core; (b) proposed modified E core.

TABLE IV
DESIGN CONSTRAINTS FOR INVERSE COUPLED INDUCTOR WITH PLANAR CORE AND PCB WINDING

Item	Values
Maximum EE core height	26mm
Maximum core length l_{c,m_max}	100mm
Minimum core thickness c_{m_min}	5mm
Number of layers in one PCB	6 layers
PCB height h_{pcb}	2.2mm
copper thickness h_{copper}	3oz (0.105mm)
Current density of the winding J	20 A/mm^2

As a result, dead areas are eliminated. The proposed modified E core has a lower profile and shorter length since the thickness of the outer leg significantly contributes to these dimensions ($h_m < h$ and $l_{c,m} < l_c$). This is very beneficial in high power inductor design in which the availability of a large-dimension core is basically limited by manufacturers. Moreover, due to the larger bottom plate area, the thermal resistances from PCB winding-to-core and from core-to-heatsink are smaller, leading to the lower operating temperature. Note that the outer leg's cross-sectional area in the conventional E core and the proposed E core are identical

$$b \cdot c = b_m \cdot c_m. \tag{7}$$

E. Optimization Number of Turns Based on the Dimensions Limit of the Customized Core

With the proposed core structure and the required value of $N \cdot A_c$ above, this section discusses the selection of the number of turns for each winding. Since the proposed modified EE core is customized, its dimensions are restricted by the project specifications, manufacturer capability, and mechanical stability. Moreover, due to cost reason, the number of layers of the PCB winding is also limited by the project. A summary of the project constraints of the inductor design is given in Table IV.

Each winding of the coupled inductor conducts a high current of 73 A at the full-load condition. To reduce the PCB winding

footprint, each winding is made of two 3oz six-layer PCBs connected in parallel since the current density of the winding J is limited by 20 A/mm^2. In each six-layer PCB, four layers are used to create the turns, while the other two layers are used to deliver current from inside to outside of the windings. As a result, the PCB trace width in each layer w_t is about 4.35 mm. Other power electronics components are compactedly arranged in a power board with a length of 105 mm. Therefore, the ideal length of the coupled inductor is to be equal to that of the power board so that the whole converter can be placed in a rectangular volume without a dead area. However, the core length $l_{c,m}$ is designed at 100 mm which is limited by the project. Based on the maximum converter height given in Table I, the maximum height of the EE core is set to 26 mm considering the margin for the TIM placed between the core and the heatsink. The thickness of the TIM h_{TIM} is about 1 mm. Based on Table IV and Fig. 14(b), the volume and height of the inductor can be expressed by

$$\text{Inductor volume} = 10^{-6} \cdot l_{c,m\_\max} \cdot b_m \cdot (2 \cdot (e + c_m)) \tag{8}$$

$$\text{Inductor height} = 2 \cdot (e + c_m) \tag{9}$$

$$w = N \cdot w_t + (N + 3) \cdot d_w \tag{10}$$

$$w_t = \frac{I_{\text{rms,max}}}{8 \cdot J \cdot h_{\text{copper}}} \tag{11}$$

$$b_m = \frac{N \cdot A_c}{N \cdot \frac{-B + \sqrt{B^2 - A \cdot C}}{2 \cdot A}} + 2 \cdot (w - d_w) \tag{12}$$

$$c_m = \frac{0.6 \cdot N \cdot A_c}{N \cdot b_m} \tag{13}$$

$$e = 2 \cdot h_{\text{pcb}} + 2 \cdot h_{\text{TIM}} + \frac{h_{\text{cooling\_plate}}}{2} \tag{14}$$

$$A = 2 \cdot (w - d_w) \tag{15}$$

$$B = 2.2 \cdot \frac{N \cdot A_c}{N} + (4 \cdot w - 2 \cdot l_{c,m\_\max}) \cdot (w - d_w) \tag{16}$$

$$C = (2 \cdot w - l_{c,m\_\max}) \cdot \frac{N \cdot A_c}{N}. \tag{17}$$

Based on (8)–(17), the volume and height of the coupled inductor as a function of the number of turns are shown in Fig. 15. For the same $N \cdot A_c = 28$ turns·cm^2, the lower number of turns results in a larger cross-sectional area, which leads to a higher core profile and larger volume. On the other hand, a high number of turns leads to high conduction loss of the winding. Therefore, in this article, $N = 5$ is selected, as seen in Fig. 15.

Multivias are placed in each turn to connect the windings in the different layers. These vias have two purposes: first, balance the current between layers; second, transfer the heat from the middle layers to the outside. A small air gap of about 0.5 mm is set to achieve the designed self-inductance value of $L = 28 \ \mu\text{H}$. Details of the five-turn PCB winding modified EE core inverse coupled inductor are shown in Fig. 16. The 3D FEA simulation results of the proposed planar core and PCB winding at full load are shown in Fig. 17. The simulated $B_{\max}$ is around 150 mT
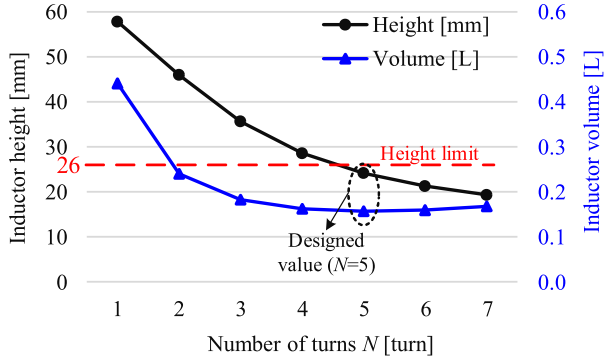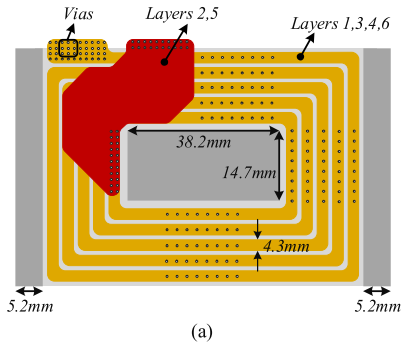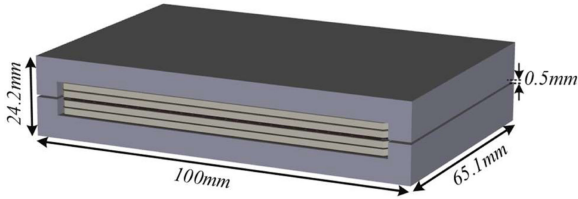
Fig. 15. Volume and height of the inverse coupled inductor as a function of number of turns N.

(a)

(b)

Fig. 16. Proposed planar inverse coupled inductor: (a) front-view of the five-turn PCB winding and the proposed E core parameters; (b) 3-D view.

(a)

(b)

Fig. 17. FEA simulation result of the planar inductor: (a) current distribution; (b) flux distribution.

which is similar to the designed value. However, the current density of the winding is a bit higher than 20 A/mm² because of the high-frequency effect.
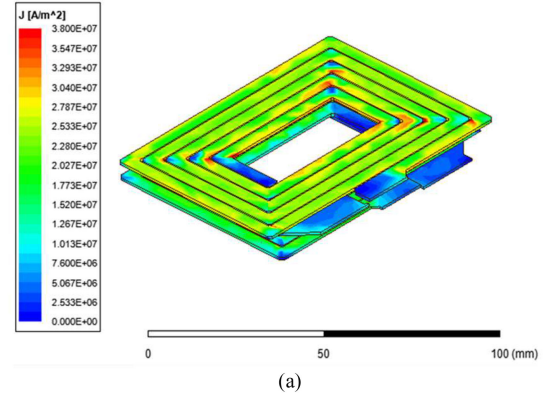
F. Inductor Loss Analysis

Based on the above design procedure, the inductor loss as a difference of switching frequency and number of turns will be estimated and discussed. Core loss is calculated as
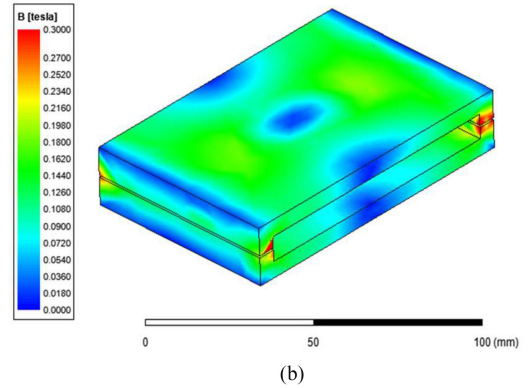
$$P_{cv} = k \cdot B_{\max}^{\alpha} \cdot f^{\beta} \tag{18}$$

$$P_{\text{core\_loss}} = P_{cv} \cdot V_{\text{core}} \tag{19}$$

where P_{cv} is the core loss density (kW/m³ or W/L); k, α, and β are temperature-dependent parameters given in [36]; f is the switching frequency in case of the coupled inductor. In this article, the contribution of ac and dc flux at the full load condition

is nearly equal, as shown in Fig. 13. Thus, $B_{\text{ac,max}}$ is about half of $B_{\max}$ for the core loss calculation, $B_{\text{ac,max}} \approx 0.75$ mT.

The winding conduction loss is calculated as

$$R_{\text{PCBwinding}} = \frac{\rho \cdot L_{\text{PCBwinding}}}{A_{\text{winding}}} \quad [\Omega] \tag{20}$$

$$P_{\text{winding}} = 2 \cdot R_{\text{PCBwinding}} \cdot I_{\text{rms,full\_load}}^{2} \quad [W] \tag{21}$$

where $\rho = 0.0171 \, [\frac{\Omega \cdot \text{mm}^2}{\text{m}}]$ is the resistivity of copper, A_{winding} [mm²] is the effective cross-sectional area of a winding, and $L_{\text{PCBwinding}}$ [m] is the length of a winding.

From (18)–(21) and the design procedure above, the inductor loss and volume as a function of switching frequency are calculated and draw in Fig. 18.

As shown Fig. 18, the inductor achieves minimum loss at 150 kHz. However, the difference of inductor loss between 150 and 300 kHz is not significant, which is less than 10 W. Therefore, the inductor is designed at 300 kHz for volume reduction since the core and winding temperatures are still under acceptable level, as shown in the following section.

Fig. 19 shows the inductor loss as a function of number of turns. It can be seen in Fig. 19 that minimum inductor loss is at three turns, but five-turn winding is selected because of the height limit. The use of higher than five turns is not efficient due to higher loss.
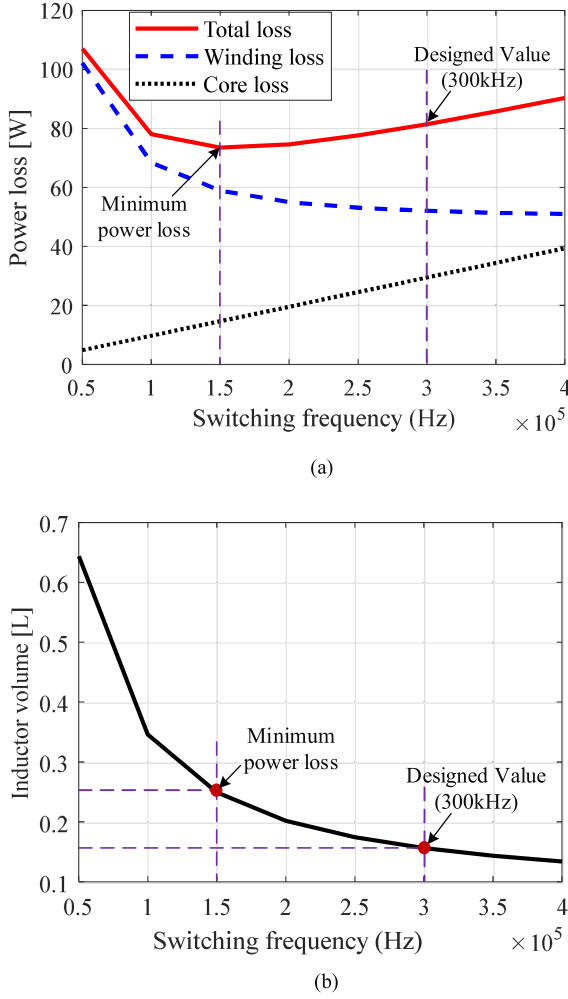
(a)

(b)

Fig. 18. Power loss and volume of the inverse coupled inductor at full load as a function of switching frequency: (a) power loss; (b) volume.
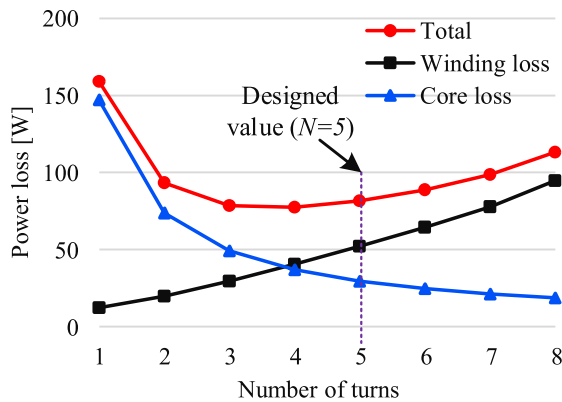

Fig. 19. Power loss of the inverse coupled inductor at full load as a function of number of turns N.

V. Experimental Prototype and Results

A. ZVT Cell Design

ZVT cell in this article is designed to help the main switches achieve soft switching in the whole operating range of FDC,

which is from 10 kW (305 V) to full load (228V), as shown in Fig. 2.

For snubber inductor, the minimum energy of snubber inductor demanded to discharge C_{oss} of the main switch at the light load of 10 kW is calculated as

$$\frac{1}{2} \cdot L_{s1} \cdot I_{L1,@10kW}^2 \geq \frac{1}{2} \cdot C_{oss,S1} \cdot V_{C1,@10kW}^2 \qquad (22)$$

$$\Rightarrow L_{s1} \geq C_{oss,S1} \cdot \frac{V_{C1,@10kW}^2}{I_{L1,on@10kW}^2} = 0.1 \; \mu H. \qquad (23)$$

On the other hand, the snubber inductance value should be small enough to rise from zero to the winding inductor current at full load, and discharge the C_{oss} energy within its operating interval t_{Ss}, which can be expressed as [32]

$$L_{s1}$$

$$\leq \left(\frac{-\frac{\pi}{2} \cdot \sqrt{C_{oss,S1}} + \sqrt{\frac{\pi^2}{4} \cdot C_{oss,S1} + 4 \cdot \frac{I_{L1,on@25kW}}{V_{C1@25kW}} \cdot t_{Ss}}}{2 \cdot \frac{I_{L1,on@25kW}}{V_{C1@25kW}}} \right)^2$$

$$\Rightarrow L_{s1} \leq 1.3 \; \mu H \qquad (24)$$

where t_{Ss} is set to be 5% of a switching period. From (23) and (24), the snubber inductance value is restricted by $0.1 \; \mu H \leq L_s \leq 1.3 \; \mu H$. It can be seen that the required inductance value of the snubber inductors to provide ZVS turn-ON for the main switch is very small. This is because the DFOBC has low voltage imposed on the main switch leading to smaller the required ZVT energy. This enables to use a three-turn air-core inductor in each snubber circuit for lower volume and cost. Finally, the snubber inductance value of 0.7 μH is used, achieving from three turns air core inductor.

The snubber capacitor is designed to ensure that it can be charged to output capacitor voltage by the transferred energy of the snubber inductor, which is expressed as

$$C_{s1} \leq \frac{L_{s1} \cdot I_{Ls1,pk@25kW}^2}{V_{C1,@25kW}^2} = 11.7 \; nF. \qquad (25)$$

Therefore, in this article, $C_s = 3 \; \mu$F is selected considering the current rating, which includes 30 ceramic capacitors connected in parallel.

B. Experimental Prototype Concept for High Power Density FDC

To verify the theoretical analysis and design procedure above, a 25 kW, 300 kHz laboratory prototype of DFOBC with inverse coupled inductor and ZVT cells, as shown in Fig. 7, is built and tested. As requested by the project, the selected components must be qualified for automotive applications. A summary of the component ratings and selected devices for the experimental prototype is shown in Table V.

For high power density, the multiboard assembly structure is used, and the concept of the experimental prototype is shown in Fig. 20. All the semiconductor devices are placed between a power board and heatsink. To reduce the footprint for the power board, current sensors are directly placed on the PCB windings

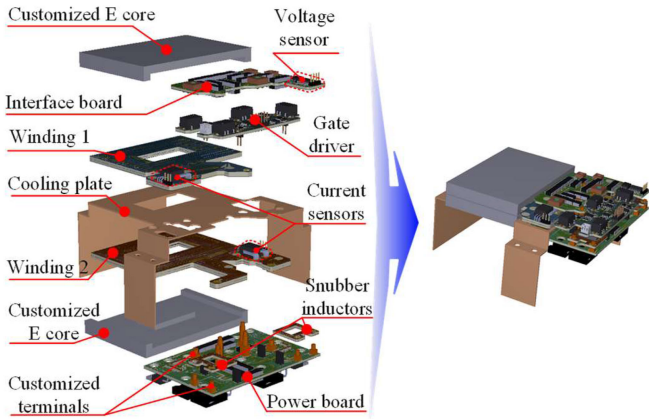| Components	Ratings	Selected devices
Main switch (S_1, S_2)	551V, 54A$_{rms}$	NVHL020N120SC1 (ON Semiconductor) 1200V, 73A@100ºC, $R_{ds,on}$ = 28mΩ, C_{oss} = 300pF@514V
Main diode (D_1, D_2)	551V, 30A$_{avg}$	STPSC20H12-Y (ST), 2 diodes per phase 1200V, 20A@155ºC, V_F = 1.5V
Inverse coupled inductor	L = 28µH 92.3A$_{pk}$ 75 A$_{rms}$	B_{max} = 0.15T, N = 5 turns, k = 0.93 2 x (6-layer 3oz PCB winding) per phase
Output capacitor (C_{o1}, C_{o2})	551V, 36 A$_{rms}$ 4µF	C2220C104KDRACAUTO (KEMET) 1000V, 0.1µF (40 cap. per phase)
Snubber switch (S_{s1}, S_{s2})	551V, 10.6A$_{rms}$	NVHL080N120SC1 (ON Seniconductor) 1200V, 22A@100ºC, $R_{ds,on}$ = 110mΩ, C_{oss} = 90pF@514V
Snubber diode	$D_{s1,4}$ 980V, 3.8 A$_{avg}$	STPSC10H12-Y (ST) 1200V, 10A@155ºC, V_F = 1.5V
	$D_{s2,5}$ 551V, 1.3 A$_{avg}$	
	$D_{s3,6}$ 551V, 1.3 A$_{avg}$	
Snubber inductor (L_{s1}, L_{s2})	I_{rms} = 13.3A L_s = 0.7µH	N = 3 turns, air core 2 x (6-layer 3oz PCB winding) per phase
Snubber capacitor (C_{s1}, C_{s2})	551V, 8A$_{rms}$ 3 nF	C1206C151JDGACAUTO (KEMET) 1000V, 0.15nF (20 cap. per phase)

Fig. 20.   Concept of high-power density soft-switching DFOBC.
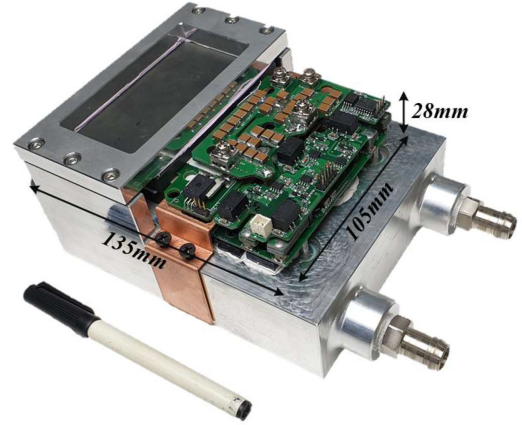

Fig. 21.   Proposed 300 kHz, 63 kW/L ZVT DFOBC prototype.

C. Results and Discussions

The experiment is implemented by DSP TMS320F28377 under the room and coolant temperatures of 24 and 20 °C, respectively. An oscilloscope YOKOGAWA DLM4058 is used to measure the voltage and current waveforms, and the converter efficiency is measured by a digital power meter YOKOGAWA WT3000. Since the 25-kW FC stack is not available in our laboratory, the converter is powered by ITECH IT6036C-500-180, and the resistive load is used at the output.

Fig. 22 shows the experimental results at 300 kHz under full load condition of V_i = 228 V, V_o = 800 V, P_o = 25 kW. Fig. 22(a) shows the gating signal and drain–source voltages of the main switches. The ZVS is achieved at both turning ON and OFF. The input inductor currents and output capacitor voltages are shown in Fig. 22(b). The ripple of the input current is larger than that of the winding currents, which is a characteristic of the inverse coupled inductor. Since PCB windings are used, their parasitic capacitors and leakage inductor create a resonant circuit and cause ringing in the winding currents of each phase. However, the ringing current is mostly canceled out at the input side due to 180º phase shift of the currents in two phases, as shown in Fig. 22(b). There are two kinds of parasitic capacitors in the PCB windings of the coupled inductor, which are the capacitor in each winding ($C_{\mathrm{pcb},11}$ and $C_{\mathrm{pcb},22}$), and the capacitor between two windings ($C_{\mathrm{pcb},12}$ and $C_{\mathrm{pcb},21}$), as shown in Fig. 23(a). These capacitors resonate with the leakage inductor, causing the ringing in the winding current. The equivalent resonant circuit of the parasitic capacitors and leakage inductor is shown in Fig. 23(b). The leakage inductance is calculated by $L_k = (1 - k)L = 1.96\ \mu H$. The period of ringing current obtains in Fig. 23(b) is about $T_{r,pcb}$ = 100 ns. Therefore, the equivalent parasitic capacitor $C_{\mathrm{pcb},eq}$ in the PCB winding can be estimated by

$$C_{\mathrm{pcb,eq}} = \frac{T_{r,\mathrm{pcb}}^2}{4 \cdot \pi^2 \cdot L_k} = 129 \text{ pF}. \qquad (26)$$

The voltage stress applied to the main switches during the turn-OFF interval is equal to the output capacitor voltages of 514 V, which is lower than the output voltage, as shown in

which are connected to the power board via customized terminals. In high switching frequency applications, PCB windings are usually the hottest part due to high ac resistance. Therefore, a copper cooling plate is introduced to deliver the heat generated in PCB winding to the heatsink, which reduces the PCB windings' temperature by 27 °C at the full-load condition. The output capacitors are placed in two parts, the first part is on the main power board, and the second part is on the power interface board which consists of the input and output terminals and the voltage sensor. The snubber inductors are placed on two sides of the main power board.

The final prototype of the 300 kHz, 25 kW soft-switching DFOBC with liquid coolant heatsink is shown in Fig. 21, yielding the power density of 63 kW/L excluding heatsink.
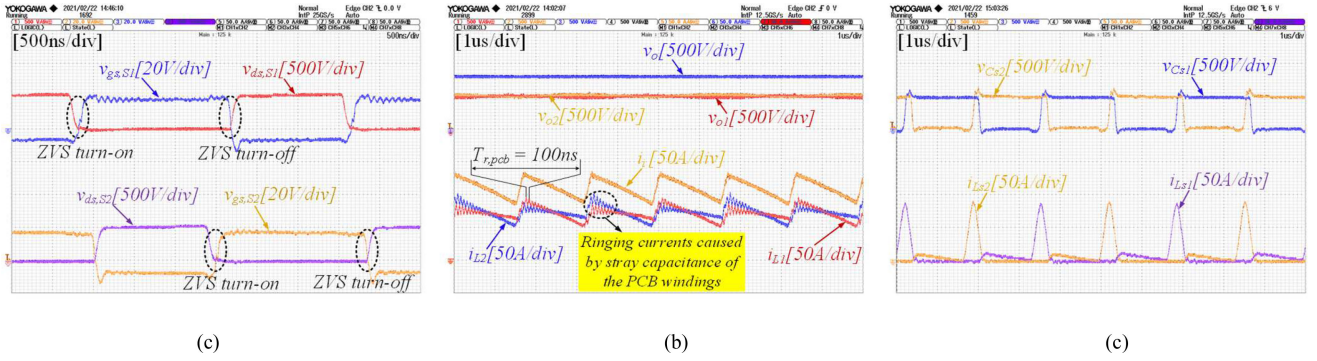
Fig. 22. Experimental results at $V_i = 228$ V, $V_o = 800$ V, $P_o = 25$ kW, and $f_s = 300$ kHz: (a) soft switching of the main switches; (b) input inductor currents and output capacitor voltages; (c) snubber inductor currents and voltages.
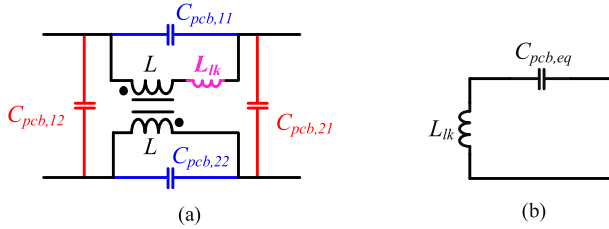

Fig. 23. Parasitic capacitors of the coupled inductor and equivalent of the resonant circuit: (a) parasitic capacitors; (b) equivalent resonant circuit.
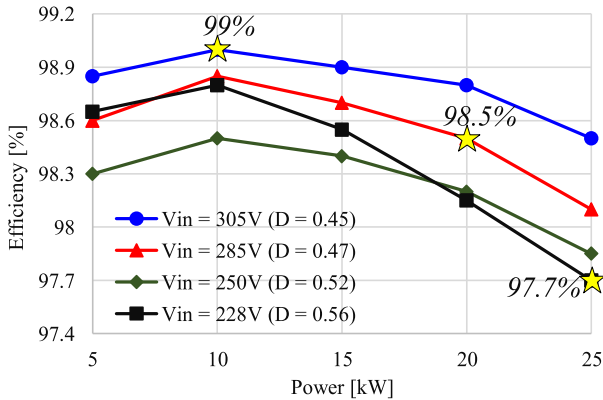

Fig. 25. Loss breakdown at $V_i = 228$ V, $V_o = 800$ V, $P_o = 25$ kW, and $f_s = 300$ kHz. Total loss = 575 W.

Fig. 24. Measured efficiency of the proposed soft-switching DFOBC with inverse coupled inductor at 300 kHz.
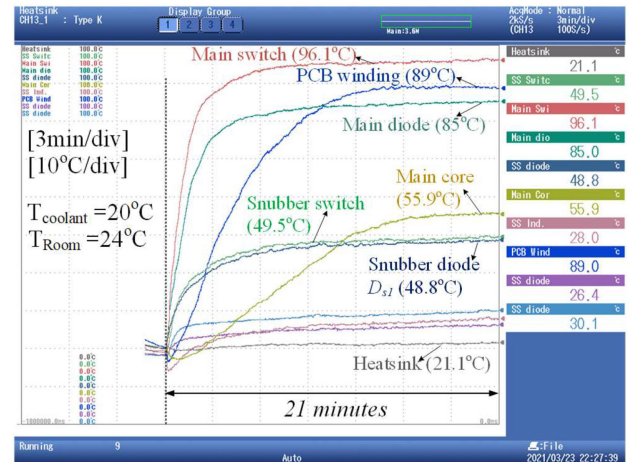
Fig. 26. Thermal test of the proposed converter at $V_i = 228$ V, $V_o = 800$ V, $P_o = 25$ kW, and $f_s = 300$ kHz.

Fig. 22(a) and (b). The snubber inductor currents and snubber capacitor voltage are shown in Fig. 22(c).

The measured efficiencies of the converter with loads and input voltages variation show in Fig. 24. The efficiencies stay above 97.5% in the whole operating range. The converter efficiency measured at 20 kW, 285 V input is about 98.5% which is higher than the project target. The peak and full-load efficiency confirm to 99% and 97.7%, respectively.

It can be seen from Fig. 24 that the converter achieves higher light-load efficiency when operation away from $D = 0.5$. This is because the core loss of the inverse coupled inductor is higher as closer to $D = 0.5$, and the core loss is dominant over the conduction loss at the light load condition. On the other hand, the full-load efficiency is higher as higher input voltage since conduction loss is dominant over the core loss

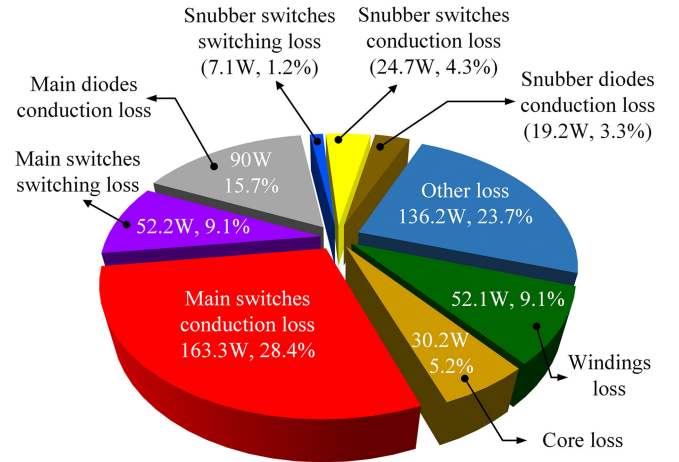at the full-load condition. It is clearly shown in Fig. 24 that efficiency is significantly reduced as the input voltage reduces at the same power rating of 25 kW. This is the main reason making the design of FDC more challenging than dc–dc converter in other applications.

Loss breakdown of the converter at full load condition is shown in Fig. 25. The conduction loss of the main switch is the most dominant loss, while the switching loss is low even at 300 kHz due to soft switching operation. The ZVT cell losses contribute a small portion of the total converter losses.

The device temperatures measured by YOKOGAWA DL850 at full load condition are shown in Fig. 26. The main switch is the hottest component with the full-load temperature of around 96.1 °C, which is close to the thermal analysis. The PCB winding and core of the coupled inductor saturate at 89 and 55.9 °C, respectively. Other components also confirm temperatures under an acceptable level.

VI. CONCLUSION

In this article, the 800-V FDC with a high power density of 63 kW/L is developed by applying the switching frequency of 300 kHz. For 800-V dc link, the DFOBC is selected as the most suitable topology because its duty cycle lies in the vicinity of $D = 0.5$, which minimizes the required inductance and capacitance values of the input and output filters. The ZVT cell and its proposed modified version are adopted to eliminate the switching losses of the converter, which realizes the high switching frequency operation. As a result, planar core and PCB winding can be used for the main inductor of the 25 kW, 800 V DFOBC, leading to volume reduction.

Cost and loss comparisons between the hard and soft switching strategies at 300 kHz are given. The modified E core with a lower profile and smaller volume compared to that of the conventional E core is proposed. The inverse coupled inductor design procedure with the optimization of the number of turns and cross-sectional area based on the project constraints is introduced to achieve low-profile and small volume targets. Also, a copper cooling plate is introduced to reduce the PCB windings' temperature.

Finally, a 25-kW prototype of one module of the proposed soft-switching DFOBC operated at 300 kHz is built and tested. The experimental prototype achieves both power density and efficiency targets.

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