High Gain Soft-Switching Bidirectional DC–DC Converter for Eco-Friendly Vehicles

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***Abstract*—This paper proposes a nonisolated soft-switching bidirectional dc–dc converter suitable for high step-up and step-down applications. The proposed converter can achieve zero voltage switching turn on of all switches and zero-current-switching turn off of some switches in continuous conduction mode in both forward and reverse modes. An optimized switching strategy is presented to minimize switch current rating and achieve soft switching in wider range. An intermediate switching pattern is introduced to carry out seamless mode change. Experimental results from a 5-kW prototype are provided to validate the proposed concept.**

***Index Terms*—Bidirectional dc–dc converter (BDC), continuous conduction mode (CCM), high step-up, high voltage gain, nonisolated, soft switched.**

I. Introduction

THE advantages of using a bidirectional dc–dc converter (BDC) in hybrid electric vehicles (HEVs) are efficient charge of regenerative energy as well as voltage boost and regulation for efficient operation of inverters and motors. The conventional half-bridge topology [1], [17] has been used as a BDC for HEV due to simple structure. The multiphase interleaved technique [2] can be employed to decrease the volume of passive component. However, the switch voltage rating of the converter based on half-bridge topology is the same as the output voltage. The three-level converter in [3] has lower switch voltage stress (half compared to the half-bridge topology) and smaller passive components even though the component count increases.

In HEV, the input voltage of the inverter has a tendency to increase in order to use high-speed high-power motor and improve the efficiency and power density of the inverter. For example, the input voltage has increased from 500 to 650 V in fourth-generation PCU of Toyota Prius HEV, where a Ni-MH battery of nominal voltage of 201.6 V has been installed [4]. In the meantime, the battery voltage is preferred to be low since parallel strings of storage batteries not only enhance the redundancy of the back-up system, but also alleviate the problems associated with charge imbalance compared to series strings [5]. Therefore, high efficiency BDC with high voltage gain is preferred in the aforementioned systems. If the conventional half-bridge topology is used for high voltage gain, the boost diode must sustain a short pulse current with high amplitude, resulting in severe reverse recovery [1], [6] as well as high EMI problems. Using an extreme duty cycle may also lead to poor dynamic responses to line and load variations. These make the conventional half-bridge topology inefficient in the applications where high voltage gain is required.

Also, high-frequency operation is required to achieve high power density, improve dynamic characteristic, and reduce acoustic noise. The switching frequency of the hard switching BDC is limited due to switching losses and EMI problem [7]. In order to increase switching frequency of the BDC, several soft-switching techniques have been applied to the half-bridge topology that could achieve zero voltage switching (ZVS) or zero-current-switching (ZCS) of main switches using an auxiliary circuit in both forward and reverse modes of operation [8], [9], [20]. The converter in [8] integrates an active clamp circuit into the half-bridge topology to achieve soft-switching in CCM operation. The converter in [9] is based on a cascaded buck-boost structure with active snubber circuits in order to achieve zero-voltage and zero-current transition, showing high efficiency despite of its circuit complexity. The converter is capable of being operated with boost and buck operations in both forward and reverse modes. However, they are not suitable for application where high-voltage conversion ratio in both boost and buck operations is required.

BDCs based on coupled or tapped inductors [10]–[13], [21] can provide high output voltage without extreme duty cycle and yet reduce the switch voltage stress. In these coupled inductor converters, in general, the effort to overcome the problem associated with a leakage inductor of the coupling inductor is nontrivial, and the capacity of the magnetic core should substantially be increased as the required output power is increased. Therefore, these topologies incorporating the coupling inductor are not suitable for high-power applications. Also, the input current ripple is considerable due to the operation of coupling inductor.

The BDC using switched-capacitor converter cells could have more modular structure and higher power handling capability, but the required number of switches becomes high [14]–[16]. They are hard-switched, and high current pulse occurs since two capacitors with different voltages are connected in parallel at each switching instant. A major drawback of the switched-capacitor-based converter is that ESR drop of the active and passive devices is considerable due to high number of series connected devices in the current path, resulting in reduced output voltage. This may restrict the power level to which the switched-capacitor converter can be applied. So far, the nonisolated BDC

Manuscript received December 21, 2012; revised April 28, 2013; accepted June 10, 2013. Date of current version October 15, 2013. This work was supported in part by Seoul National University of Science and Technology and by a National Research Foundation of Korea (NRF) grant funded by the Korea Government (MEST) (No. 2012-000545). Recommended for publication by Associate Editor M. Ferdowsi.

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Digital Object Identifier 10.1109/TPEL.2013.2271328

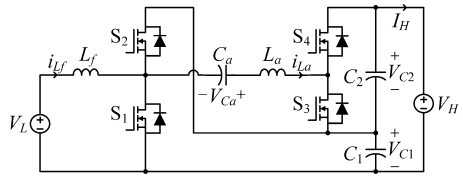

Fig. 1. Proposed high step-up soft-switched bidirectional dc–dc converter.

with high-voltage gain that can be applied to high power level has rarely been proposed.

In this paper, a new nonisolated BDC for high step-up/step-down and high-power applications is proposed. The optimized PWM switching technique for boost and buck operations and smooth mode transition is also presented. The proposed converter has the following advantages:

1) high voltage gains for both boost and buck operations;
2) reduced (nearly half) voltage stresses of switches;
3) ZVS turn on and ZCS turn off of switches in CCM operation;
4) reduced energy volumes of passive components;
5) seamless mode transition.

II. Proposed Converter

Fig. 1 shows the circuit diagram of the proposed BDC. The proposed converter consists of a general half-bridge converter as the main circuit and an auxiliary circuit that includes the capacitor C_a, inductor L_a, and two high-voltage side (HVS) switches S_3 and S_4. The goal of control, in this paper, is assumed to regulate the HVS voltage V_H, while allowing bidirectional power flow according to the direction of inductor current I_{Lf}.

A. Operating Principle

Assume that capacitances C_1, C_2, and C_a are large enough so that voltages V_{C1}, V_{C2}, and V_{Ca} across them are constant during the switching period T_S.

1) Boost Operation (Forward Mode): Figs. 2 and 3 show key waveforms and operation states of the boost operation, respectively. In this mode, low-voltage side (LVS) switches S_1 and S_2 are operated with asymmetrical complementary switching with duty cycles of D and $1-D$, respectively, as shown in Fig. 2. In the mean time, HVS switches S_3 and S_4 are turned ON with delay times of t_{d3} and t_{d4}, respectively. The operation of the proposed converter can be divided into five modes, as shown in Fig. 3.

Mode I [t_0–t_1]: This mode begins with turning OFF of S_2 and S_4. Then, the body diodes of S_1 and S_4 are turned ON. The gating signal for S_1 is applied with appropriate dead-time during this mode, and then S_1 could be turned ON under ZVS condition. Inductor currents i_{Lf} and i_{La} start to increase and decrease, respectively, with the slopes determined by the following equations:

$$\frac{di_{Lf}}{dt} = \frac{V_L}{L_f} \tag{1}$$

$$\frac{di_{La}}{dt} = \frac{V_{Ca} - V_{C1} - V_{C2}}{L_a}. \tag{2}$$

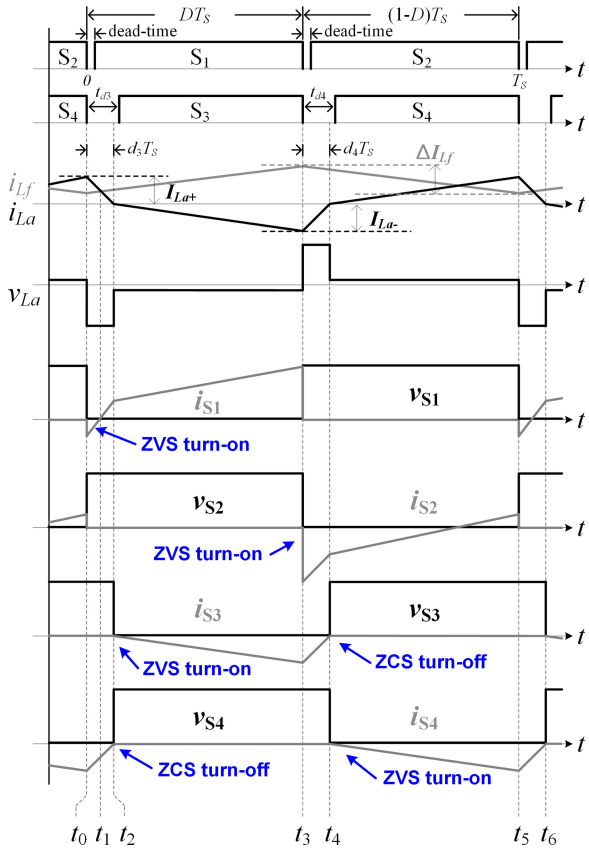

Fig. 2. Key waveforms of the proposed converter (boost operation).

Mode II [t_1–t_2]: When the increasing current i_{Lf} becomes greater than the decreasing current i_{La}, current flowing through S_1 is reversed, and the main channel of S_1 conducts. This mode ends when the decreasing current i_{La} reaches 0 A. Note that switch S_4 is also turned OFF under ZCS condition.

Mode III [t_2–t_3]: At t_2 current i_{La} is reversed and the body diode of S_3 is turned ON. For synchronous rectification the gating signal for S_3 can be applied after t_2. Note that S_3 is turned ON under ZVS condition. Inductor current i_{La} linearly increases with the slope determined by the following equation:

$$\frac{di_{La}}{dt} = \frac{V_{Ca} - V_{C1}}{L_a}. \tag{3}$$

Both inductor currents i_{Lf} and i_{La} flow through switch S_1.

Mode IV [t_3–t_4]: At t_3 switches S_1 and S_3 are turned OFF, and then body diodes of S_2 and S_3 are turned ON. Both inductor currents i_{Lf} and i_{La} start to decrease with the slopes determined by the following equations:

$$\frac{di_{Lf}}{dt} = \frac{V_L - V_{C1}}{L_f} \tag{4}$$

$$\frac{di_{La}}{dt} = \frac{V_{Ca}}{L_a}. \tag{5}$$

The gating signal for S_2 is applied with appropriate dead-time during this mode, and then S_2 could be turned ON under ZVS condition. This mode ends when the decreasing current i_{La}

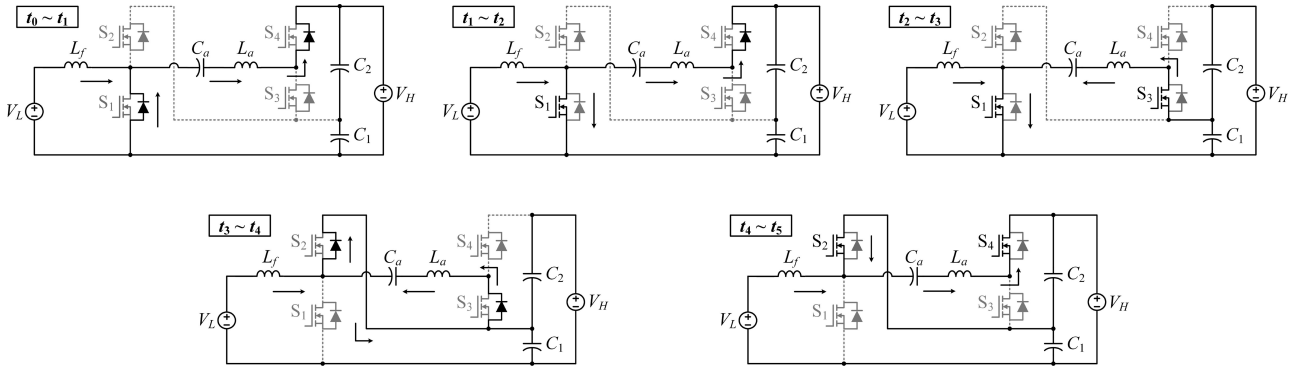

Fig. 3. Operation states of the proposed converter (boost operation).

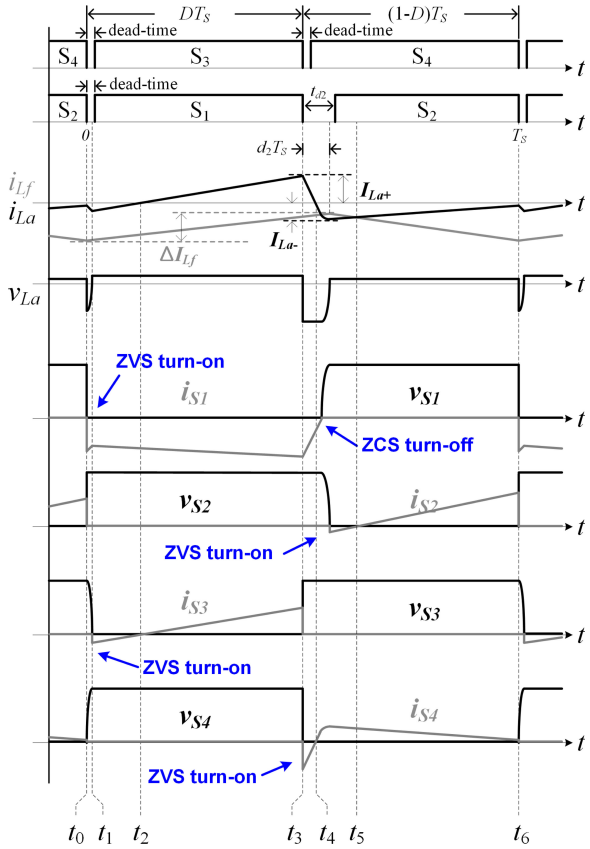

Fig. 4. Key waveforms of the proposed converter (buck operation).

reaches 0 A. Note that switch S_3 is also turned OFF under ZCS condition.

Mode V [t_4–t_5]: This mode begins when current i_{La} is reversed and the body diode of S_4 is turned ON. For synchronous rectification, the gating signal for S_4 can be applied after t_4. Note that S_4 is turned ON under ZVS condition. Inductor current i_{La} linearly increases with the slope determined by the following equation:

$$\frac{di_{La}}{dt} = \frac{V_{Ca} - V_{C2}}{L_a}. \tag{6}$$

This is the end of one complete cycle.

2) Buck Operation (Reverse Mode): Figs. 4 and 5 show key waveforms and operation states of the buck operation, respectively. In this mode, HVS switches S_3 and S_4 are operated with asymmetrical complementary switching with duty cycles of D and $1-D$, respectively, as shown in Fig. 4. In the mean time, LVS switch S_2 is turned ON with delay time of t_{d2}. The operation of the proposed converter can be divided into six modes, as shown in Fig. 5.

Mode I [t_0–t_1]: This mode begins with turning OFF of switches S_2 and S_4. Then, the body diodes of S_1 and S_3 are turned ON after the parasitic capacitors of S_3 and S_4 are completely discharged. Inductor current i_{Lf} starts to decrease with the slope determined by (1).

Mode II [t_1–t_2]: At t_1 inductor current i_{La} starts to decrease with the slope determined by (3). After appropriate dead-time switches S_1 and S_3 are turned ON. The gate signal for S_3 should be applied before reversal of current i_{La} for ZVS turn ON. Note S_1 is turned ON without any delay for synchronous rectification. This mode ends when the decreasing current i_{La} reaches 0 A.

Mode III [t_2–t_3]: At t_2 inductor current i_{La} is reversed and starts increasing with slope determined by (3). From (3), the positive peak value of i_{La} can be obtained as follows:

$$I_{La+} = \frac{V_{Ca} - V_{C1}}{L_a} \cdot DT_S - V_{C2} \cdot \sqrt{\frac{2 \cdot C_{\mathrm{OSS}}}{L_a}} \tag{7}$$

where C_{OSS} is the output capacitance of the switch.

Mode IV [t_3–t_4]: Switches S_1 and S_3 are turned OFF at t_3, and the n body diodes of S_1 and S_4 are turned ON. Inductor current i_{La} starts to decrease with the slope determined by (2). Note that S_4 could be turned ON under ZVS condition if the gate signal for S_4 is applied with appropriate dead-time before reversal of current i_{La}. This mode ends when the decreasing current i_{La} reaches 0 A.

Mode V [t_4–t_5]: When the increasing current i_{La} becomes greater than the decreasing current i_{Lf}, body diode of S_1 is turned OFF under ZCS condition. Then, after parasitic capacitors of S_1 and S_2 are completely charged and discharged, respectively, the body diode of S_2 is turned ON and inductor currents i_{La} and i_{Lf} start to decrease and increase, respectively, with slopes determined by (6) and (4), respectively. The negative

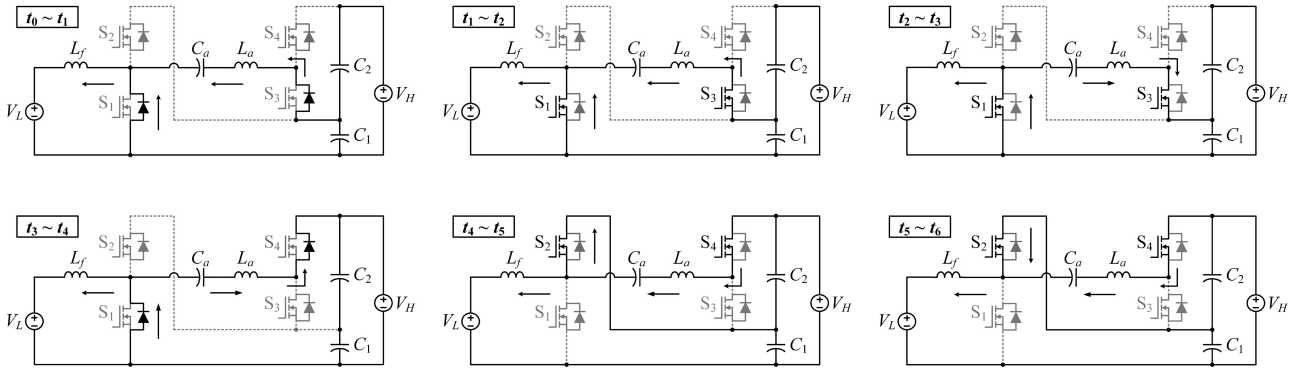

Fig. 5. Operation states of the proposed converter (buck operation).

peak value of i_{La} is determined by the following equation:

$$I_{La-} = I_{Lf} + \frac{\Delta I_{Lf}}{2} - \frac{V_{C1}}{\sqrt{L_a/(2 \cdot C_{\rm OSS})}} \tag{8}$$

where ΔI_{Lf} is current ripple of L_f. For ZVS turn on of S_2, the gate signal for S_2 should be applied before the decreasing current i_{La} becomes smaller than the increasing current i_{Lf}.

Mode VI [t_5–t_6]: At t_5 switch current i_{S2} is reversed. Inductor currents i_{La} and i_{Lf} keep decreasing and increasing with slopes determined by (6) and (4), respectively. At the end of this mode S_2 and S_4 are turned OFF. This is the end of one complete cycle.

B. Voltage Conversion Ratio

The HVS voltage is given by the following equation [18], [19]:

$$V_H = \frac{2}{1 - D_{\rm eff}} \cdot V_L \tag{9}$$

where the effective duty is defined as follows (see Fig. 2):

$$D_{\rm eff} = D - (d_3 + d_4) \tag{10}$$

where $d_3 + d_4$ means duty loss. The output voltage can also be expressed as follows:

$$V_H = \frac{2}{1 - D} \cdot V_L - \Delta V \tag{11}$$

where ΔV is the voltage drop caused by the duty loss. From (9), (10), and (11) the voltage drop ΔV can be obtained as follows:

$$\Delta V = \frac{2V_L(d_3 + d_4)}{(1 - D)(1 - D + d_3 + d_4)}. \tag{12}$$

Because the average current of both C_a and C_2 is zero, the average absolute currents of HVS switches can be expressed as follows:

$$\frac{1}{T_S}\int_0^{T_S} |i_{\rm S3}|dt = \frac{1}{T_S}\int_0^{T_S} |i_{\rm S4}|dt = I_H \tag{13}$$

where $I_H = V_H/R_H$. Assuming that the difference in duty losses d_3 and d_4 is much smaller than D, conduction times of HVS switches in the boost operation can be approximated as follows:

$$t_4 - t_2 \approx DT_S \tag{14}$$

$$t_6 - t_4 \approx (1 - D)T_S. \tag{15}$$

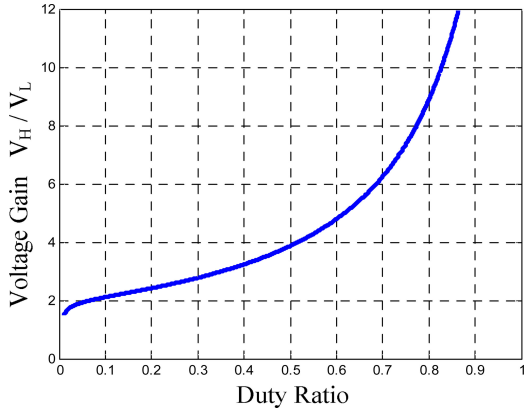

Fig. 6. Voltage gain of the proposed converter.

Then, the positive and negative peak values of i_{La} can be obtained as follows:

$$I_{La+} = \frac{2}{1 - D} \cdot \frac{V_H}{R_H} \tag{16}$$

$$I_{La-} = \frac{2}{D} \cdot \frac{V_H}{R_H}. \tag{17}$$

By applying volt-second principle to inductor L_a, we can obtain the duty losses by the following equations:

$$d_3 = \frac{2}{1 - D} \cdot \frac{V_H L_a}{R_H T_S V_{C1}} \tag{18}$$

$$d_4 = \frac{2}{D} \cdot \frac{V_H L_a}{R_H T_S V_{C1}} \tag{19}$$

where V_{C1} is the same as the output voltage of the general boost converter and can be expressed as follows:

$$V_{C1} = \frac{V_L}{1 - D}. \tag{20}$$

From (11), (12), (18), (19), and (20), the voltage gain can be obtained as follows:

$$\frac{V_H}{V_L} = \frac{\sqrt{\alpha^2(1 - D)^2 + 4\alpha\beta} - \alpha(1 - D)}{\beta} \tag{21}$$

where $\alpha = DR_H$, $\beta = 4L_a f_s$ and $f_s = 1/T_S$. Using (21), the voltage gain of the proposed converter is plotted as shown in Fig. 6.

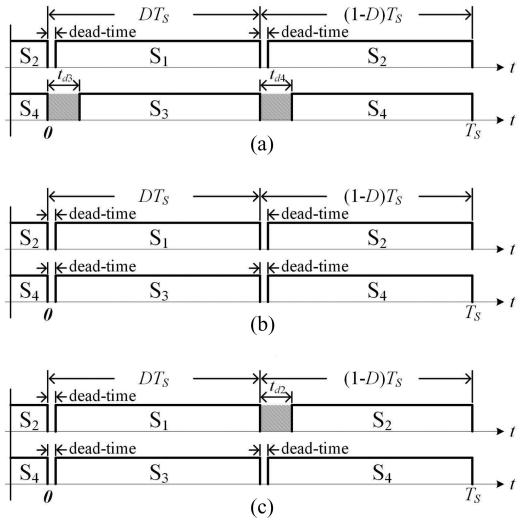

Fig. 7. Switching pattern for each operation. (a) Pattern 1 (boost operation). (b) Pattern 2 (intermediate operation). (c) Pattern 3 (buck operation).

C. Mode Change Strategy

In this section, a mode change strategy is proposed in order to carry out seamless transfer during mode change. Fig. 7 shows optimal switching patterns for each operation. The delay times for S_2, S_3, and S_4 are defined as t_{d2}, t_{d3}, and t_{d4}, respectively. The minimum delay time $t_{d2,\min}$ for ZVS turn on of S_2 is determined by the peak values of i_{Lf} and i_{La} as follows:

$$t_{d2,\min} = d_2 T_S = \frac{L_a(1-D)}{V_L} \cdot (I_{La+} - I_{Lf,\max}) \qquad (22)$$

where I_{La+} is the peak value of i_{La} in the buck operation. From (18), (19), and (20), the other minimum delay times are determined as follows:

$$t_{d3,\min} = d_3 T_S = \frac{2L_a V_H}{R_H V_L} \qquad (23)$$

$$t_{d4,\min} = d_4 T_S = \frac{1-D}{D} \cdot \frac{2L_a V_H}{R_H V_L}. \qquad (24)$$

If delay times of each switch are chosen to be smaller than their minimum delay times, ZVS cannot be guaranteed and RMS current of switches will be increased. The delay times are usually chosen to be the minimum delay times in order to minimize conduction time of a body diode of MOSFETs.

Although the switching patterns for boost and buck operations are different, seamless mode transition can be achieved by introducing an intermediate switching pattern, as shown in Fig. 8. The intermediate switching pattern is inserted between the two switching patterns for boost and buck operations. The switching sequence for transfer from forward mode to reverse mode is Pattern1 → Pattern2 → Pattern3. The switching sequence for transfer from reverse mode to forward mode is Pattern3 → Pattern2 → Pattern1. Figs. 8 and 9 show the switching sequence and control block diagram for the proposed BDC, respectively. The moment at which the switching pattern is changed is determined by comparing the instantaneous average value $I_{Lf,\text{avg}}$ of the inductor current to the preset values I_{upper} and I_{lower}, as shown

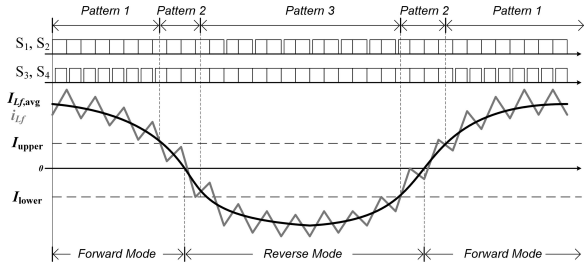

Fig. 8. Switching sequence for seamless mode change.

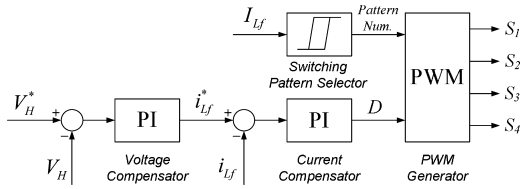

Fig. 9. Control block diagram of proposed converter for regulating HVS voltage under bidirectional operation.

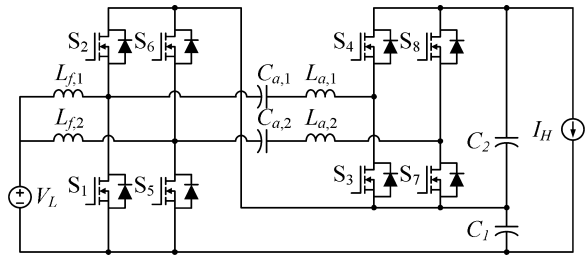

Fig. 10. Circuit diagram of the two-phase interleaved prototype converter.

in Fig. 8. If the band is too wide, ZVS may not be achieved under the light load condition. Whereas, if the band is too narrow, there will be bumping at the mode transition caused by a sudden change in switching pattern and be chattering problem under the light load condition. The maximum value of I_{upper} is determined by load condition that the minimum delay time of S_3 or S_4 becomes equal to dead-time T_{dead}. From (23) and (24), the maximum value of I_{upper} can be expressed as follows:

$$I_{\text{upper,max}} = \begin{cases} \dfrac{V_H T_{\text{dead}}}{2L_a}, & 0 < D \le 0.5 \\ \dfrac{D V_H T_{\text{dead}}}{(1-D)2L_a}, & 0.5 \le D \le 1. \end{cases} \qquad (25)$$

Similarly, the minimum value of I_{lower} is determined from (22) and as follows:

$$I_{\text{lower,min}} = \frac{\Delta I_{Lf}}{2} - \frac{V_L T_{\text{dead}}}{L_a(1-D)} - I_{La+} \qquad (26)$$

where ΔI_{Lf} is a current ripple of L_f, and I_{La+} is the peak value of i_{La} in the buck operation.

III. Experimental Results

The interleaving technique can be applied to reduce the size of passive components and current stresses. A 5-kW prototype of the two-phase interleaved version of the proposed converter shown in Fig. 10 was built according to the following

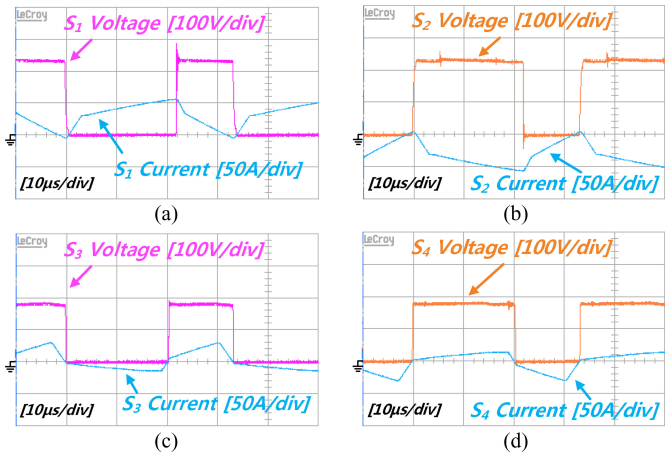

Fig. 11. Experimental waveforms of proposed converter in boost operation. (a) LVS bottom switch. (b) LVS top switch. (c) HVS bottom switch. (d) HVS top switch.

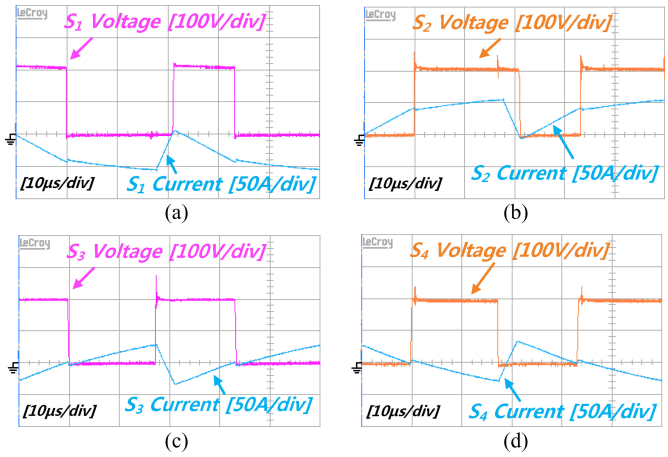

Fig. 12. Experimental waveforms of proposed converter in buck operation. (a) LVS bottom switch. (b) LVS top switch. (c) HVS bottom switch. (d) HVS top switch.

specification: $P_o = 5$ kW, $f_s = 30$ kHz, $V_H = 400$ V, $V_L = 72$–100 V, $L_f = 130$ μH, $L_a = 13$ μH, $C_a = 30$ μF, C_1=$C_2 = 470$ μF.

Both LVS and HVS switches are implemented with IXFN100N50P (500 V, 90 A, and 49 mΩ) MOSFET, and the filter and auxiliary inductor are implemented with powder cores CH610125 and CM330060, respectively, from Changsung. The nominal duty cycle of 0.64 was used to achieve voltage gain of 5.5 for the both buck and boost operations. The minimum delay times were calculated using (22), (23), and (24) under full load condition, the actual delay times t_{d2}, t_{d3}, and t_{d4} were chosen to be 3000, 3000, and 1200 ns, respectively, considering appropriate margin. The upper and lower values of the band for mode change were calculated using (25) and (26) and chosen to be $I_{\text{upper}} = 1.5$ A and $I_{\text{lower}} = -1$ A, respectively. Experimental waveforms of the proposed converter for boost and buck operations are shown in Figs. 11 and 12, respectively. Fig. 11(a) to (d) shows voltage and current waveforms of switches S_1 to S_4 in boost operation. Fig. 12(a) to (d) shows voltage and current waveforms of switches S_1 to S_4 in buck operation. It can be seen

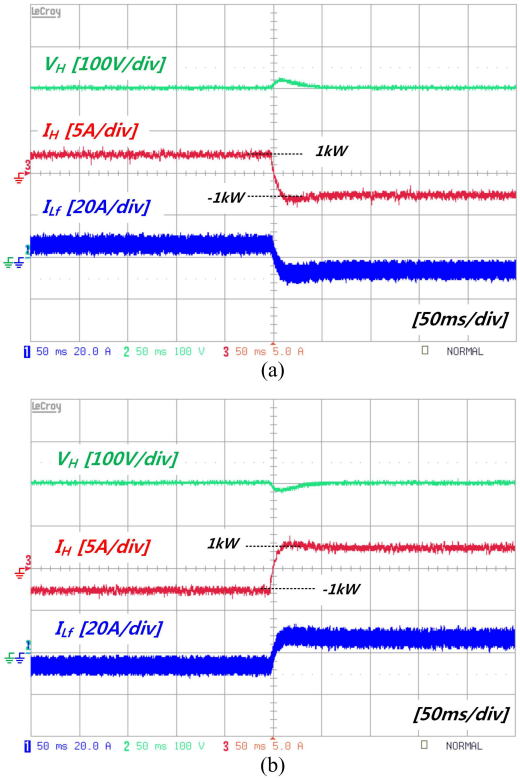

Fig. 13. Experimental waveforms of mode change. (a) From forward mode to reverse mode. (b) From reverse mode to forward mode.

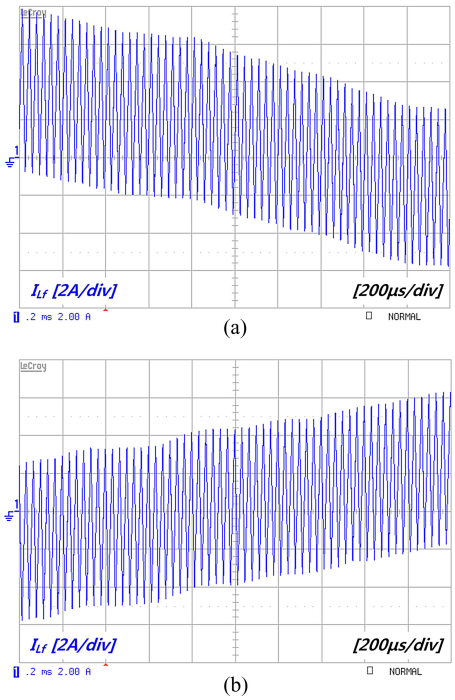

Fig. 14. Extended waveforms of the filter inductor current i_{Lf} in Fig. 13. (a) From forward mode to reverse mode. (b) From reverse mode to forward mode.

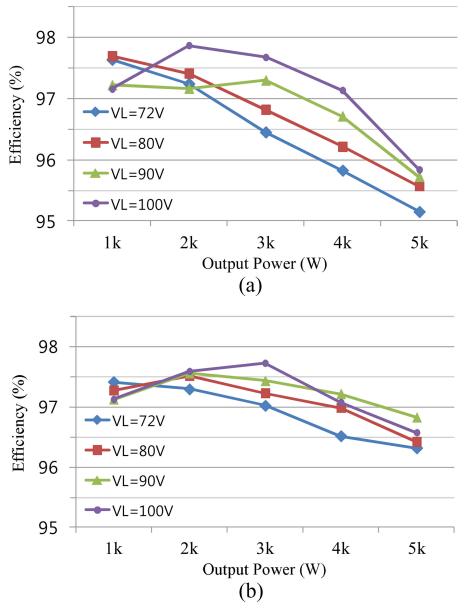

Fig. 15. Measured efficiency according to the variation of LVS voltage. (a) Forward mode. (b) Reverse mode.

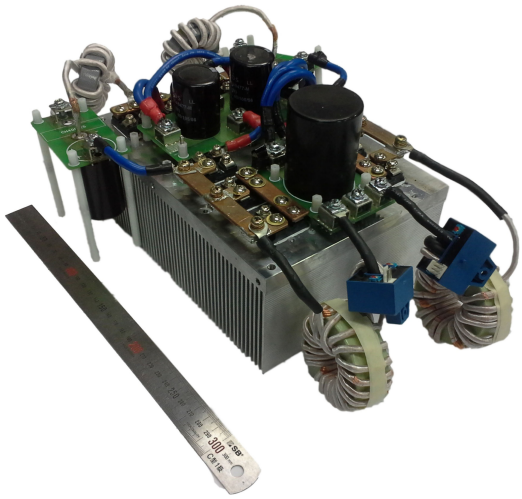

Fig. 16. Photograph of the proposed converter prototype.

that all switches are turned ON with ZVS in both operations. Experimental waveforms of mode change are shown in Fig. 13. Fig. 14 is the extended waveforms of the filter inductor current I_{Lf} in Fig. 13. It is seen that there are no transients caused by change of switching patterns during the mode change. The measured efficiencies under different LVS voltage conditions in forward and reverse modes are shown in Fig. 15. The efficiency was measured using Yokogawa WT3000. The maximum efficiencies in forward and reverse modes are 97.9% at 2 kW(V_L = 100 V) and 97.7% at 3 kW(V_L = 100 V), respectively. Fig. 16 shows the photograph of the proposed converter.

IV. Conclusion

In this paper, a nonisolated soft switching BDC has been proposed for high-voltage gain and high-power applications. The proposed converter can achieve ZVS turn on of all switches and ZCS turn off some switches in both boost and buck operations. An optimized switching sequence has been presented along with an intermediate switching pattern to carry out seamless mode change. A 5-kW prototype of the proposed converter has been built and tested to verify the validity of the proposed operation. A nominal duty cycle of 0.64 was used to achieve voltage gain of 5.5. The maximum efficiencies in forward and reverse modes are 97.9% and 97.7%, respectively. It has also been shown in the experiment that the mode change is seamless due to the proposed switching sequence.

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